A Space Vector Modulation Control Algorithm for VSI Multi-Level Converters

A. Cataliotti, F. Genduso, G. Ricco Galluzzo

Dipartimento di Ingegneria elettrica Università degli Studi di Palermo
Email: acataliotti@ieee.org; genduso@diepa.unipa.it; ricco@diepa.unipa.it
Tel. +390916566209, FAX +39091488452

Abstract. In this paper a novel modular digital control algorithm for multi level inverters is introduced and discussed. This algorithm is essentially based on the duty cycle expression and allows a great simplification, because of its modularity and its simple implementation. The algorithm is particularly suitable for the Multi Point Clamped (MPC) inverters with no constraint on the number of the voltage levels and results faster than the most recent solutions proposed in literature.
The modulation techniques considered in the paper are the sub oscillation PWM and, above all, the Space Vector Modulation (SVM), but the proposed algorithm may be employed for the main carrier based PWM control techniques including the "Zero sequence injection". Simulation of a MPC inverters, controlled with the proposed algorithm, have been made with the help of the MATLAB-SIMULINK® package. For these simulations a mathematical model already known in literature, but adapted to be used within the MATLAB-SIMULINK® environment, has been used. The simulation results show the effectiveness of the MPC model formulation and of the proposed control algorithm.

Keywords: Multilevel inverter; Space Vector Modulation; Digital modular control.

1. Introduction.

The recent progresses in the semiconductor technology made available fast commutating electronics power devices to be used with high voltages and currents, so extending the application field of Voltage Source Inverters (VSI). Actually, it is not still possible to employ traditional VSI in the high power range due to commutation difficulties and reverse recovery high voltages. Multilevel power converters are an interesting emerging technology for medium and high power applications including the fields of Renewable Energy Sources and power quality issues as active filtering and reactive power compensators (static VAR compensators).

The first multi level converter structures were the H bridge connected inverters with several different DC sources, whose main drawback is the requirement of a galvanic insulation among the DC sources. Towards the eighties Akagi Nabae et alt. introduced the Neutral point clamped (NPC) inverter [1]. This structure is able to realise an increased number of commutation states with the possibility to achieve output voltage higher than the traditional VSI, lower dv/dt, lower harmonic distortion and a reduced average switching frequency with a consequent reduction of the switching losses. NPC inverters have also been generalised introducing the structure of Multi Point Clamped Inverters (MPC) with a higher voltage level numbers than the NPC. Other important advantage of the MPC inverters is the uniform voltage sharing of the total DC Link voltage among the power devices of each leg. This correct voltage sharing is not fully assured in the traditional VSI inverter topologies with more devices connected in series. Multilevel inverters have been extensively investigated in literature showing their main advantages and drawbacks in the various application fields. [2]-[6].

In this paper, a novel digital modular PWM control algorithm, suitable for Multi Point Clamped inverters, is introduced and compared with the most recent solution proposed in literature [7], showing its greater flexibility and its possible use without limitation on the number of voltage levels and for all the main carrier based PWM techniques. This control algorithm has been verified and validated by means of simulations developed within the MATLAB-SIMULINK® programming environment. For the simulations, the mathematical model of a MPC inverter has been used, reformulating it into a particularly advantageous form suitable for the use within the MATLAB-SIMULINK® package. The inherent instability of the DC Link Capacitor voltages and its correction have been considered. A particular emphasis is given to the Space Vector Modulation Control.

2. The multi level MPC converters.

The schematic structure of a MPC inverter with power transistors is shown in fig.1

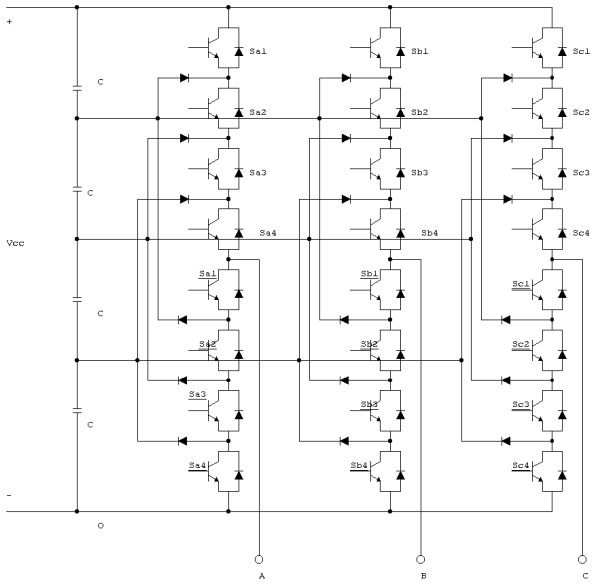

Fig. 1 Structure of the MPC converter.

In order to remind the MPC operation principle, it is convenient to introduce the switching functions S_k for the k-th device where S_k=1 in the ON state and S_k=0 in the OFF state. The output voltage V_{AO} values referred to the negative DC Bus O for all the allowed switching states are resumed in Table 1. In the same table an uniform voltage sharing of the total DC Link Voltage across the capacitors has been supposed.

In general, the expressions for the output voltages are:

$$\begin{aligned} V_{AO} &= \frac{V_{CC}}{n}(S_{A1} + S_{A2} + ... + S_{An}) \\ V_{BO} &= \frac{V_{CC}}{n}(S_{B1} + S_{B2} + ... + S_{Bn}) \\ V_{CO} &= \frac{V_{CC}}{n}(S_{C1} + S_{C2} + ... + S_{Cn}) \end{aligned} \quad (1)$$

The usual relations valid also for two level inverters express the phase voltages referred to the neutral point N of a star-connected balanced load:

$$\begin{pmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{pmatrix} = \begin{pmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{pmatrix} \cdot \begin{pmatrix} V_{AO} \\ V_{BO} \\ V_{CO} \end{pmatrix} \quad (2)$$

The generic expression of the output voltage space vector is then:

$$\underline{V} = \frac{V_{CC}}{n}\left(\sum_{k=1}^{n} S_{Ak} + \alpha \cdot \sum_{k=1}^{n} S_{Bk} + \alpha^2 \sum_{k=1}^{n} S_{Ck} \right) \quad (3)$$

where $\alpha = \exp(j2\pi/3)$

Equation (3) shows that for a n level inverter n^3 different combinations of the switching function are possible, but most of them correspond to the same voltage space vector. In particular, as the most external vectors are realisable with only one combination of the switching functions, the inner vectors are realisable in different redundant ways. This "redundancy" constitutes a difficulty in the inverter digital control. Fig.2 shows the voltage space vectors distribution in the complex plane for a four level MPC inverter.

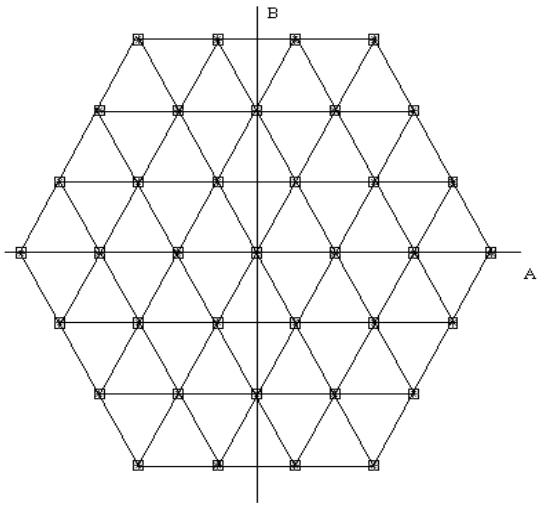

Fig. 2 Output voltage space vector of a four level MPC inverter

As it has been well investigated in the recent past [8]-[10], phenomena of inequality in voltages of the DC Link capacitors may occur because of their different average circulating currents. A difference of charge and consequently of voltage manifests during the operation of the MPC inverter for loads consuming both active and reactive power. Moreover the voltages of the different capacitor are generally unstable.

3. PWM control of MPC inverters.

Implementation of the sub-oscillation method is quite simple using multiple carrier signals, one for each voltage level, that are compared with the reference voltages given by the controller as shown in fig.3 The same figure is referred to a five level MPC inverter and exhibit the V_{AO} output voltage in p.u. of the total DC Link Voltage.

As the analog implementation does not present particular difficulties, it is rather different for digital implementation because each commutation state must be chosen on the basis of the previous state with the aim of reducing the number of switching at the least possible. This problem, already felt for the sub oscillation method, is more evident in the Space Vector Modulation (SVM) in which the complications are much higher.

Fig. 4 shows the principle of SVM in multi level converter. The reference voltage space vector is approximated applying a sequence of the adjacent voltage space vectors of the inverter V_x, V_y, V_z. The

S_{A1}	S_{A2}	S_{A3}	...	S_{An}	$\underline{S_{A1}}$	$\underline{S_{A2}}$	$\underline{S_{A3}}$	...	$\underline{S_{An}}$	V_{AO}
1	1	1	...	1	0	0	0	…	0	V_{CC}
0	1	1	…	1	1	0	0	…	0	$(n-1)V_{CC}/n$
0	0	1	…	1	1	1	0	…	0	$(n-2)V_{CC}/n$
…	…	…	…	…	…	…	…	…	…	…
0	0	0	…	1	1	1	1	…	0	V_{CC}/n
0	0	0	…	0	1	1	1	…	1	0

TABLE.1 Possible switching states in the phase A for a MPC inverter.

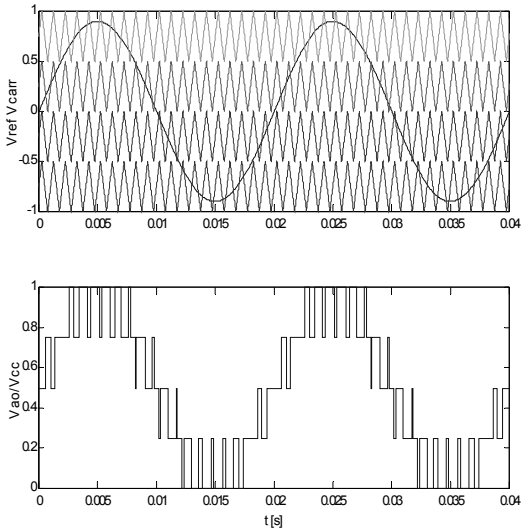

Fig. 3 Analog Sub Oscillation multi carrier method for MPC inverter (five level inverter)

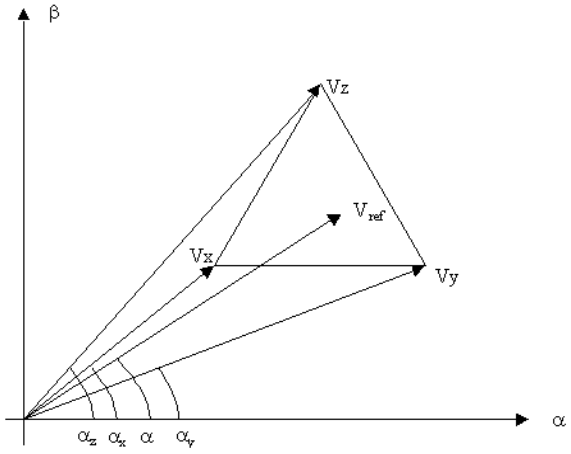

Fig.4 Principle of Space Vector Modulation in MPC inverter.

application times of these, i.e. T_x, T_y, T_z, are calculated solving the vector equation:

$$\underline{V_{ref}}\,T_{PWM} = \underline{V_x}T_x + \underline{V_y}T_y + \underline{V_z}T_z \qquad (4)$$

with the constraint $T_x+T_y+T_z=T_{PWM,}$ where T_{PWM} is the modulation period and $\underline{V_{ref}}$ is the reference voltage space vector.

Solving the vector equation (4) one obtain:

$$T_x = T_{PWM}\frac{V_{ref}V_y\sin(\alpha-\alpha_y) - V_{ref}V_z\sin(\alpha-\alpha_z) + V_yV_z\sin(\alpha_y-\alpha_z)}{(V_xV_y\sin(\alpha_x-\alpha_y) - V_xV_z\sin(\alpha_x-\alpha_z) + V_yV_z\sin(\alpha_y-\alpha_z))}$$
$$T_y = T_{PWM}\frac{V_{ref}V_x\sin(\alpha-\alpha_x) - V_{ref}V_z\sin(\alpha-\alpha_z) + V_xV_z\sin(\alpha_x-\alpha_z)}{(V_xV_y\sin(\alpha_x-\alpha_y) - V_xV_z\sin(\alpha_x-\alpha_z) + V_yV_z\sin(\alpha_y-\alpha_z))} \qquad (5)$$
$$T_z = T_{PWM}\frac{V_{ref}V_x\sin(\alpha-\alpha_x) - V_{ref}V_y\sin(\alpha-\alpha_y) + V_yV_x\sin(\alpha_x-\alpha_y)}{(V_xV_y\sin(\alpha_x-\alpha_y) - V_xV_z\sin(\alpha_x-\alpha_z) + V_yV_z\sin(\alpha_y-\alpha_z))}$$

in which α, α_x, α_y and α_z are, respectively, the phases of the voltage space vectors V_{ref}, V_x, V_y and V_z. The relations (5) may be made simpler using the α–β coordinates rather than the polar coordinates. In every case all the informations of the voltage space vectors (modulus and phase or cartesian coordinates) must be stored in a memory buffer and every possible correspondent binary switching configurations have to be associated with them.

Space vector modulation is quite more complex that in the case of two level inverters, as for the complexity of the expressions of T_x, T_y and T_z, as in consideration of the redundancy.

An efficient and fast SVM algorithm for MPC inverter presented in [7] is articulated in the following summarised procedures:

- determination of the three voltage space vectors adjacent to V_{ref};
- calculation of the duration time of the three nearest vectors before determined;
- determination of the switching pattern taking the redundancy into account, realising the condition of least ON-OFF commutation number and proper addressing of the register buffer.

Each of these procedures is articulated into various sub procedures whose details are exposed in the dissertation [7].

It is important to remark that the dimension of the memory buffer and the number of the instructions of the algorithm increase with the Voltage level number. In the following section a novel faster and simpler SVM algorithm for MPC that does not use any memory buffer and having a lower number of instructions, is introduced and discussed.

4. The proposed digital modular algorithm for MPC inverter.

In the carrier based PWM control techniques, when the reference voltage is sampled at the PWM carrier frequency, the ratio between the width of the switching pulse of every device, calculated by means of the intersection between the carrier and the modulating signal, and the modulation period T_{PWM} is equal to the duty cycle. If duty cycle expression is known “a priori” it may be implemented on a microprocessor in order to obtain directly the switching functions for the inverter control. It can be observed that considering multi carrier and single reference is equivalent to consider only one carrier and more reference voltages obtained adding positive or negative offsets to the main modulating signal. Fig. 5 shows as the modulation pattern, in both cases, will be the same.

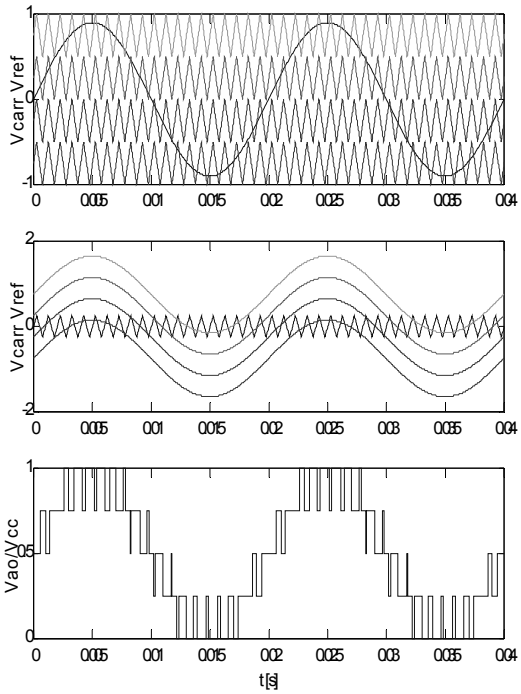

Fig. 5 Comparison between single reference multi-carriers and multi references single carrier for the determination of the switching pulse pattern.

Then a novel algorithm has been developed starting from the duty cycle expression. In the case of sub oscillation method the duty cycle for two level inverter is [11],[12]:

$$d_n = \frac{1}{2} + \frac{u_{n\_ref}}{V_{CC}} \tag{6}$$

in which u_{n_ref} is the phase modulating signal of the phase n and V_{CC} is the voltage on the DC Link Capacitor. Considering the offset added to the reference voltage in a MPC inverters, the duty cycle expression becomes:

$$d_n = \frac{1}{2} + \frac{u_{n\_ref}}{U_{CC}} \pm \frac{V_{offset}}{U_{CC}} \tag{7}$$

in which U_{CC} is the single capacitor voltage. The values of the offset voltage are integer multiples of U_{CC} for inverter with odd number of voltage levels and semi integers multiples of U_{CC} for inverter with even voltage level number. Positive offset values are applied to control the lower voltage level, while the negative values are applied to control the upper ones.

In the SVM technique the duty cycle is [11]-[12]:

$$d_n = \frac{1}{2} + \frac{u_{n\_ref} + U^*}{V_{CC}} \tag{8}$$

in which:

$$U^* = -\frac{1}{2}\{\max(u_{1ref}, u_{2ref}, u_{3ref}) + \max(u_{1ref}, u_{2ref}, u_{3ref})\} \tag{9}$$

In the SVM, the offset has to be added to the whole modulating signal $u_{n\_ref}+U^*$ and not only to the reference voltage because, with evidence of (8) and (9), the offset should vanish in the expression. In order to obtain the same result of the sub oscillation method, expression (8) must be modified as follows:

$$d_n = \frac{1}{2} + \frac{u_{n\_ref} + U^*}{U_{CC}} \pm \frac{V_{offset}}{U_{CC}} \tag{10}$$

In each control module of the algorithm the so modified duty cycle will be implemented with the suitable offset value.

Fig.10 shows the n-level block scheme of the modular algorithm generating the switching signal for each inverter leg. The modulator block that determines the modulation patterns may be realised by means of standard digital counters.

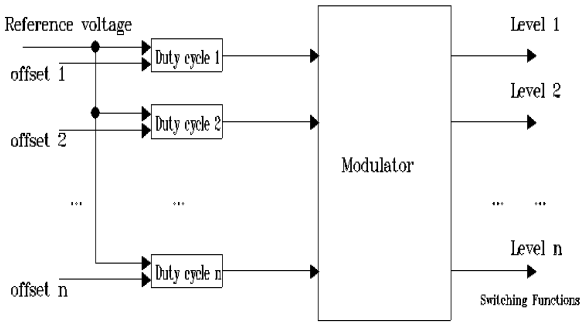

Fig. 6 Block scheme of the modular digital algorithm for n level MPC inverter

The greatest simplification is obtained for SVM technique due to the following reasons:

- employment of formulas with no trigonometric function with all the advantage of algebraic manipulation;
- identification of the three adjacent vectors is not necessary;
- the least switching number is automatically achieved by equivalence to the multi carrier analog method.

Other advantages of the proposed algorithm are:

- modular structure of the control algorithm that allows easy extension and application to each voltage level number;
- possibility of extension to all the Zero Sequence Injection PWM techniques because they have the

same duty cycle expression (8) except for the expression of the term U*;
- possibility of simple implementation on low cost microprocessors.
- low number of instruction to be loaded at every step.

The last advantage is of a particular importance for the fast execution of the algorithm. For a three level inverter the method presented in [7] requires in total 147 instructions as the algorithm here proposed requires only 34 instructions:

a. 26 instruction for the calculation of the duty cycles (16 instruction for the determination of the minimum maximum values of the reference sampled voltage and 10 instruction for the various sums and multiplications involved);
b. 8 instructions for the determination of the switching instants directly from the duty cycles.

5. Simulations.

A. Mathematical modelling of a MPC inverter

Simulations of the controller and of the converter have been made in the MATLAB SIMULINK® environment. In order to make simulations realist the inherent instability of the DC link voltages has been considered by including the equations of the DC Link Capacitors behaviour. The model of a multi level inverter has been presented in [7] for the case of a "three level" inverter. A more general form that considers the possibility of unequal voltage sharing across the DC Link Capacitors, using matrix notation, valid for all the voltage level number and suitable to be easily implemented in MATLAB-SIMULINK® environment, is (load model included):

$$\begin{aligned} \underline{i_c} &= i_o \underline{1} - \underline{S} \cdot \underline{i_L} \\ \underline{v_c} &= \frac{1}{C}\int_0^t \underline{i_c}\,dt \\ \underline{v_i} &= \underline{S}^t \cdot \underline{v_c} \\ T\underline{v_i} &= \underline{R}\underline{i_L} + \underline{L}\frac{d\underline{i_L}}{dt} \end{aligned} \qquad (11)$$

where:

$\underline{i_c}$ is the vector of the capacitor currents: $[i_{c1}\ i_{c2}\ \dots\ i_{cn}]^t$;
$\underline{1}$ is a vector whose elements are all ones: $[1\ 1\ \dots\ 1]^t$;
$\underline{i_L}$ is the vector of the load currents: $[i_A\ i_B\ i_C]$;
$\underline{v_c}$ is the vector of the capacitors voltages:
$[v_{c1}\ v_{c2}\ \dots\ v_{cn}]^t$;
$\underline{v_i}$ is the vector of the output voltages of the inverter referred to the negative DC bus: $[v_{AO}\ v_{BO}\ v_{CO}]^t$;
i_0 is the DC input current of the inverter;
$\underline{R}$ is the diagonal matrix of the load resistances;
$\underline{L}$ is the diagonal matrix of the load inductances;
$\underline{S}$ is the matrix whose elements are the switching functions:

$$S = \begin{pmatrix} S_{A1} & S_{B1} & S_{C1} \\ S_{A2} & S_{B2} & S_{C2} \\ \dots & \dots & \dots \\ S_{An} & S_{Bn} & S_{Cn} \end{pmatrix} \qquad (12)$$

T is the square matrix used in eq. (2);

The simulation program have been built interconnecting three different blocks: one for the converter model, one for the digital modular controller and one for the load.

Inside the simulation of the power converter a DC Link Voltages stabilisation system, shown in fig.7, has been considered. It is realised with a shunt resistor that allows the discharge of those capacitors whose voltage increases during operation. This discharge is allowed by a thyristor when over-voltage assumes a prefixed value. The balancing circuit has been modelled and then included in the block of the converter simulation.

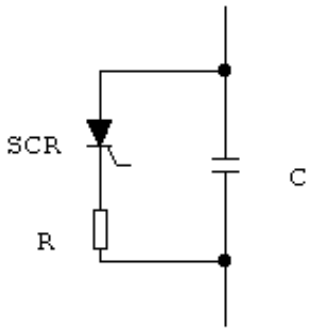

Fig. 7 Shunt resistance and SCR for the compensation of unequal voltage sharing in the DC Link Capacitors.

Fig.8 shows the graphical program used for the simulation of the converter and of its PWM controller.

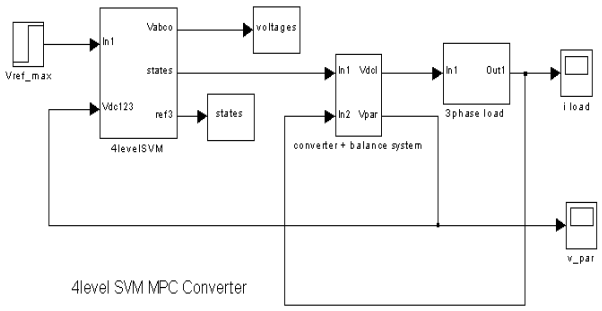

Fig. 8 MATLAB-SIMULINK® Graphical program for the simulation of an MPC inverter with SVM control.

The converter and load parameters used for the simulation are resumed in table 2:

Converter and Load Parameter used for the simulation	
DC link capacitors	500μF
Source inductance	4500μH
Switching frequency	2000 Hz
Rated Capacitor single voltage	560V
Discharge Capacitor shunt resistance	100 Ω
Output frequency	50 Hz
Load impedance	100 Ω
Load Power factor range	0-1

TABLE 2: Parameters of the simulated 4 level MPC converter and of the load.

B. Simulation results

Figure 9 shows the simulated phase output voltage for various values of the reference voltage. Figure 10 is a particular of figure 9 at the maximum value of the output voltage. The modulation technique used for the simulation is the Space Vector Modulation. Fig. 11 shows the shape of the load currents and of the input DC current simulated at steady state operation. The output current is practically sinusoidal because of the low harmonic content of the phase voltage even if the power factor is near unity.

Figure 12 finally shows the partial DC Link Voltages stabilised by means of the circuit shown in fig. 7. In the case study an tolerance of 10 V over-voltages is allowed for the external capacitors.

All the simulations show the effectiveness and the correctness of the proposed algorithm being in accordance with several experimental results reported in literature.

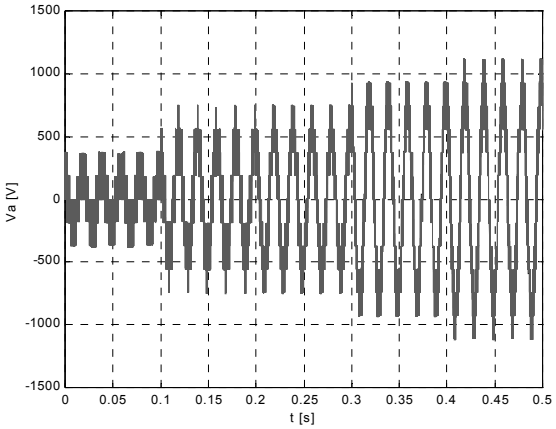

Fig. 9 Output phase voltage of the MPC converter for different reference voltage amplitudes.

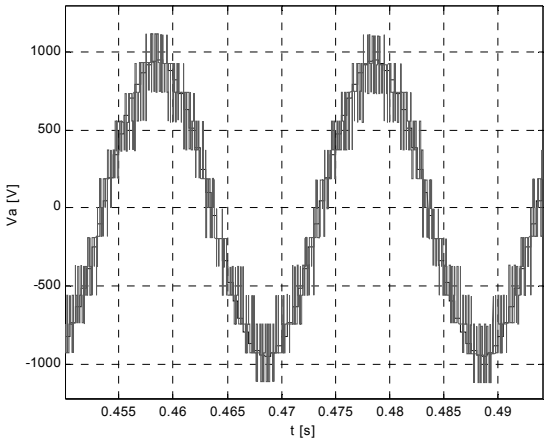

Fig. 10 Particular from fig. 8 (maximum output voltage)

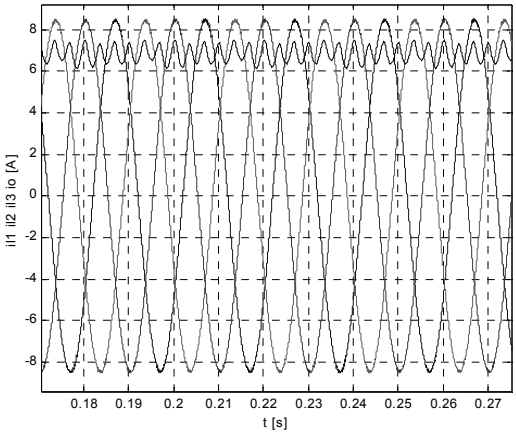

Fig. 11 Input and output (load) currents.

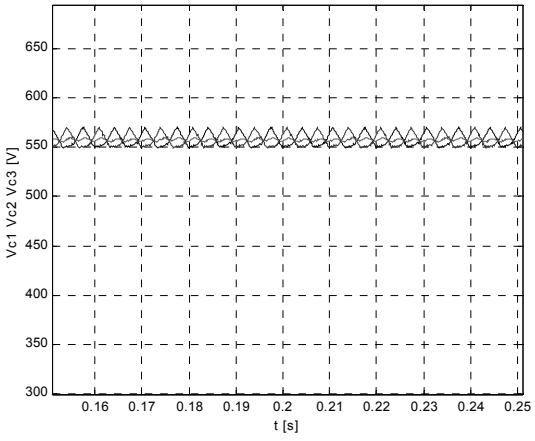

Fig. 12 Partial DC Voltage on each DC Link Capacitors with the balancing system operating.

6. Conclusions.

In this paper a novel modular digital control algorithm suitable for simple and immediate implementation of complex PWM control techniques, as for example Space Vector Modulation, has been presented. The advantages of the proposed algorithm compared with other solutions proposed in literature may be resumed as follows:

- reduced calculation amount respect to the other solutions by not using trigonometric complex expression, as in the case of standard classical SVM;
- automatic realisation of the least commutation number;
- modular structure for extension to arbitrary voltage level number;
- great flexibility in implementation of zero sequence injection PWM techniques in which duty cycle expression is available;
- simple implementation on low cost microprocessors;
- low number of instruction to be loaded at each step.

Extensive simulations in various conditions have been made with the help of the MATLAB-SIMULINK® programming environment, showing as the control algorithm works correctly. This algorithm may be considered particularly suitable in different conditions and for various employment of Multi point Clamped Converter as, for example, in renewable energy source conversion systems, Static VAR compensation, active filtering.

7. References.

[1] A. Nabae, I. Takahashi, H. Akagi. “A neutral-point clamped PWM inverter”, IEEE Trans. on I.A., Vol. IA-17, No. 5, 1981, pp. 518-523.

[2] M. Carpita, M. Fracchia. S. Tenconi. “A novel multilevel structure for voltage source inverter”, Proceedings of the 4th European Conf, on Power Electronics and Applications (EPE’91), Firenze, Italy, September 1991, pp.1-090/1-094.

[3] T. Ghiara, M. Marchesoni, L. Puglisi, G. Sciutto. “A modular approach to converter design for high power AC drives”, Proceedings of the 4th European Conf. on Power Electronics and Applications (EPE '91), Firenze, Italy, September 1991, pp. 4-477/4-482.

[4] Damiano A., M. Fracchia, M. Marchesoni, I. Marongiu. “A new approach in multilevel power conversion”, Proceedings of the 7th European Conference. on Power Electronics and Applications (EPE '97), Trondheim, Norway, September 1997, pp. 4.216-4.221.

[5] M. Fracchia, T. Ghiara, M. Marchesoni, M. Mazzucchelli. “Optimized modulation techniques for the generalized n-level converter”, PESC’92 Conference Record, Toledo, Spain, June/July 1992, pp.1205-1213.

[6] G. Sinha, T.A. Lipo, “A four level rectifier-inverter system for drive applications”, 31th IEEE IAS Annual Meeting Conf. Record, San Diego, California, October 1996, pp. 980-987.

[7] N. Celanovic “A Fast Space Vector modulation Algorithm for Multilevel converter". Dissertation for partial fulfillement of the Ph.D. degree in Electrical and computer engineering” Virginia polytechincal Institute Oct. 2000.

[8] F.Z. Peng, J.S. Lai, J. McKeever, J. Van Coevering. “A multilevel voltage-source converter system with balanced DC voltages”, Power Electronics Specialists Conference Proceedings, Atlanta, Georgia, June 1995, pp. 1144-1150.

[9] M. Marchesoni, M. Mazzucchelli, P. Tenca. “About the DC-link capacitors voltage balance in multi-point clamped converters”, Proceedings of the International 24th Annual Conference of the IEEE Industrial Electronics Society (IECON’98), Aachen, Germany, September 1998, pp. 548-553.

[10] M. Marchesoni, M. Mazzucchelli, F.V.P.Robinson, P. Tenca. “A Minimum-Energy-Based Capacitor Voltage Balancing Control Strategy For MPC Conversion Systems”, Proc. of IEEE-ISIE 99 Conference, Bled, Slovenia, July 1999, pp. 20-25.

[11] Cataliotti A, Genduso F, Ricco Galluzzo G. A New SVM Algorithm for VSI based electrical drive fed by Photovoltaic arrays” EERR (Electrical Engineering Research Report) Naples, April 2002;

[12] Cataliotti A, Genduso F, Ricco Galluzzo G. A New Over Modulation Strategy for High-Switching Frequency Space Vector PWM Voltage Source Inverters” Proceeding of the IEEE ISIE 2002, L’Aquila July 2002.