# A 270 – 330 GHz Vector Modulator Phase Shifter in 130nm SiGe BiCMOS

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***Abstract* — This paper presents a wideband vector modulator phase shifter measured at frequency bands reaching and ever surpassing the $f_t$ of the technology for 6G beamforming for extremely high data rate applications. The circuit is designed based on 130nm SiGe BiCMOS technology with $f_t$ / $f_{max}$ of 300/500 GHz. The chip occupies a die area of 0.53×0.48 mm$^2$ and offers a total 360° of phase variation with a pad-to-pad gain of -10dB over its 270 – 330 GHz operational ranges.**

***Keywords* — phased array, phase shifter, vector modulator, SiGe, HBT, BiCMOS, beamforming, 6G.**

## I. Introduction

Due to demands for extremely high data rates, upper mm-wave bands up to THz region have become an attractive range for recently discussed 6G wireless communications systems. The envisioned properties and performance requirements of the 6G systems impose much more burden on the electronics design as the physical limitations of some of the available technologies are at the edge of reasonable performance. Thus, it is increasingly difficult to design an integrated circuit solution to meet the stringent requirements. This is due to the intrinsic behavior of the semiconductors at frequencies higher than $f_t/10$ as the key performance characteristics of the active components are heavily impacted at the mentioned bands. Atmospheric absorption and attenuation along with high path loss and hence limited link budget also add to the problem. One approach to address the issues is the phased array antenna solution, i.e. beamforming [1] – [6].

Phase shifters (PS) are the key building blocks of the beamforming systems utilized in long range connectivity and multiple-user multiple-input-multi-output (MIMO) systems. Demand for higher data rate envisioned by 6G wireless communications systems, and the need for beamforming for mobility require spacial scanning systems. Thus, the design of phase shifters is of great importance.

Since the vector modulators are in favor of gain and smoother phase variation, directly proportional to the control mechanism e.g. number of bits in case of DAC controlled ones, they have been widely utilized in almost every frequency band [1] – [6]. Compact size has been achieved at the cost of DC power consumption compared to their passive counterparts [7] – [9].

In this respect, this paper presents a 20% fractional bandwidth phase shifter with a center carrier frequency of 300 GHz, i.e. $f_t$ of the technology. The rest of this paper is organized as follows. In section II, the designed vector modulator phase shifter (VMPS) circuitry is discussed. The measurement results are then shown in section III. The paper is concluded in section IV.

## II. Vector Modulator Phase Shifter Circuitry

The schematic of the implemented vector modulator is shown in Fig. 1. It is based on the concept in [10] wherein the simulated results were presented without implementation. The input signal is first decomposed into two namely in-phase (I) and quadrature (Q) signal components each of which is then weighted passing through a variable gain amplifier (VGA). The weighted I and Q signals are summed at the output node of the VGAs to form the phase shifted version of the input signal.

The circuit consists of two Marchand baluns, one coupled-transmission-line based quadrature hybrid coupler, two Gilbert cells, and two 5-bit current steering digital-to-analog converters (DAC) equipped with serial-to-parallel shift registers. The Marchand baluns are utilized to convert the single-ended signal to their differential counterpart and vice versa at the input and output sides, respectively.

Core of the circuit is designed inherently to be fully differential. Marchand baluns at the input and output facilitate single ended measurements at the desired frequency bands of 220 – 330 GHz corresponding to the available equipment. Each balun has simulated loss of ~1dB that is included in the total measured gain later in this paper. The quadrature hybrid coupler for initial 90° phase shift, which is comprised of two quarter wave coupled transmission lines shielded with ground walls on the sides, generates the differential I and Q signal components for the input of the VGAs. Gilbert cells are used to realize the VGA circuitry with I and Q signals applied to the tail transistors and gain controlling signals to the differential pairs. Due to the simplicity of the Gilbert cell circuitry, it has primarily been the candidate for such high frequencies [1] – [6]. The inductance $L_{cp}$ partly compensates the capacitances reside in the translinear loop [10]. The capacitance $C_b$ ensures only DC signals at the base nodes of the differential pairs in addition to guarantee total DC current through transistors $Q_{b1}$ – $Q_{b4}$. They also form a logarithmic operation to cancel out the antilog property of the base-emitters of the differential pairs. This yields more linear multiplication from digital control words to the output

constellation points over the frequency range. The weighting factors are determined by the two 5-bit current steering DACs in each branch. The weighed I and Q signals are then summed up at the output node of the Gilbert cells to form the phase shifted version of the input signal.

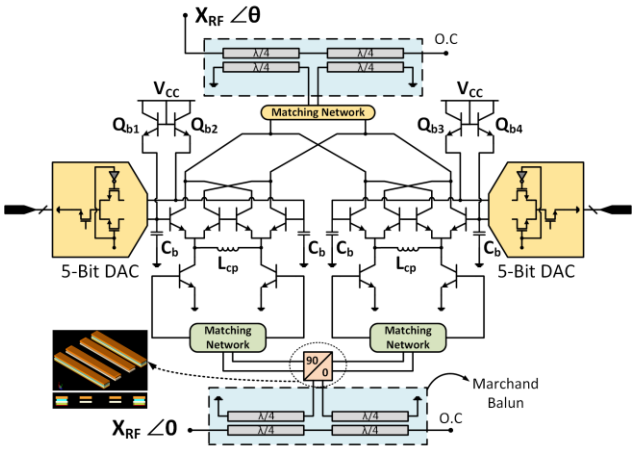



Fig. 1. Circuit schematic of the designed vector modulator phase shifter.

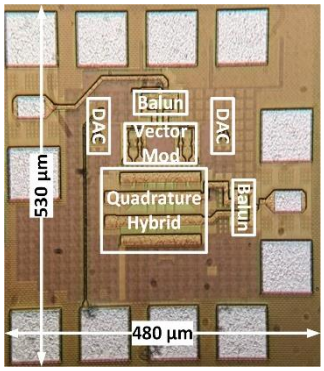



Fig. 2. Photograph of the designed vector modulator phase shifter.

## III. Measurement Results

The chip has been fabricated using 130nm SiGe BiCMOS process with $f_t$ / $f_{max}$ of 300/500 GHz. The microphotograph of the circuit is shown in Fig. 2. The chip dimensions are 0.53×0.48 mm$^2$, including the bias and signal pads. The active area of the phase shifter is only 0.179×0.13 mm$^2$. The chip draws 45 mA from 2.5 V of which 8 mA was burnt by the DACs, 7 mA burnt in the current mirror references, and 4 mA by the log/antilog circuitry. So, the net power consumed by the vector modulator phase shifter core is $2.5\ V \times 26\ mA = 65\ mW$.

The chip was measured on wafer using VDI WR3.4 extension kits connected to GSG infinity probes from Cascade Microtech. The probe tip short-open-load-thru (SOLT) calibration method on the P/N 138-357 calibration substrate was performed. An automatic measurement routine was developed based on MATLAB scripts consisting of the digital control codewords along with the commands for the Keysight PNA N5247B. The measurements were conducted in the time domain continues-wave (TDCW) mode. The schematic of the measurement setup is shown in Fig. 3.

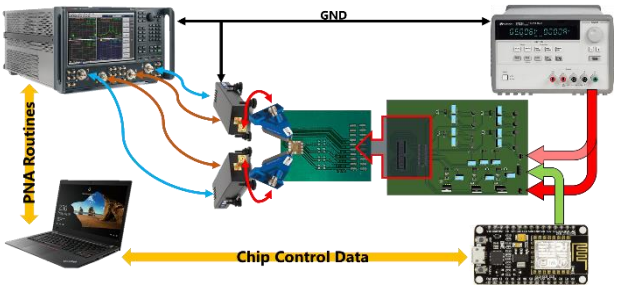
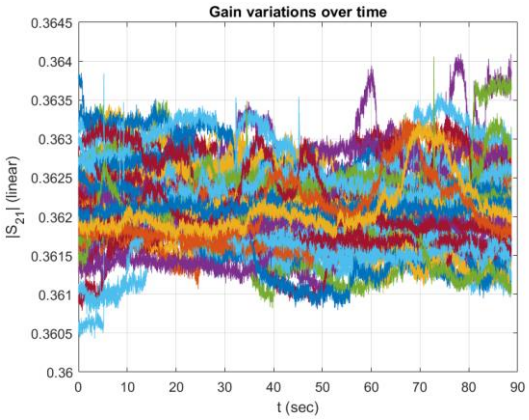
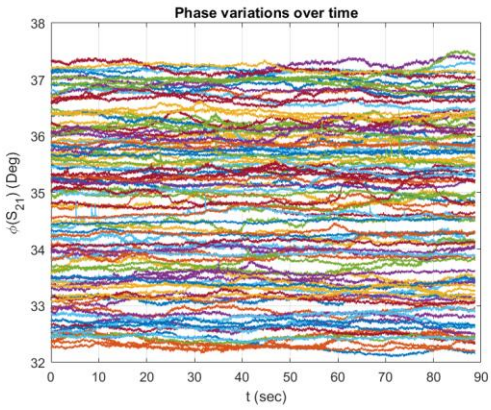



Fig. 3. Measurement setup block diagram.




(a)




(b)

Fig. 4. The variation of the reference point (a) amplitude and (b) phase over time.

To extract the constellation points the gain $S_{21}$ was measured in time domain. This is to prevent phase miss-locking in frequency domain. In other words, in frequency sweeping mode the internal/local oscillators of the PNA tend to lock to the reference frequency rather than phase. Therefore, the reference phase tends to vary randomly with each new frequency setting. To prevent this, for measurement purposes, the PNA was set to TDCW mode to ensure that the reference phase remain constant throughout the whole measurement sequence. Even in TDCW mode, the reference phase varies over the time due to time dependent variation of the measurement equipment systems properties. This also yields improper phase measurement. The variation of the reference point is shown in Fig. 4.

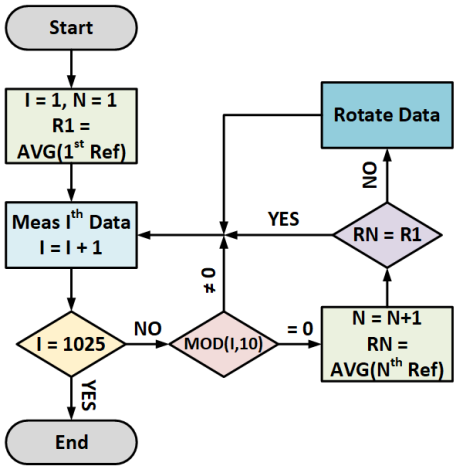



Fig. 5. The flowchart of the measurement routine.

To verify the measurement accuracy over time, the variation of the gain is shown in linear scale instead of logarithmic (Fig. 4(a)). Error seen from Fig. 4(a) the amplitude variation of the gain is quite negligible and limited close 0.5% on average. Hence, it can be ignored. Being on the order of $-2.5° \leq \Delta\phi \leq 2.5°$, the phase variation on the other hand varies in a larger scale with time (Fig. 4(b)). In phase shift measurements, a constellation point corresponding to the maximum gain was chosen as a reference, i.e. the code word was set to one of the outermost corners of the constellation diagram. Then, the automatic measurement routines were set to return to and measure the exact same reference point after every ten code words measurement sequence. The measured reference was then averaged. In case there existed a variation in the reference point, the phase of the measured group of gains were rotated accordingly. And then the rest of the measurement continued. This is shown in the flowchart diagram of Fig. 5.

Reference data point is defined in the measurements by averaging over 10001 samples and the rest of the constellation points were measured against that reference without averaging. Figs. 6 – 8 illustrate the measured constellation points at 270 GHz, 300 GHz, and 330 GHz, respectively. The presented circuit covers the whole plane, i.e. complete 360° of phase rotation for the whole band. In case of 330 GHz a hollow area was observed due to lack of points in origin. However, phase shifting was still operating properly.

Frequency response of the designed vector modulator phase shifter is shown in Fig. 9. The frequency response of the designed circuit is broad, i.e. ~100 GHz. Though, the constellation points start to be more distorted at frequencies below 260 GHz. Based on the plots, gain control in VMPS amplifiers tends to be more limited at some bands due to feedthrough. The more the gain can be controlled towards lower levels, i.e. more negative in dB scale, the more evenly constellation points are distributed towards the center of the constellation plane (Figs. 6 – 8). Limited gain range is clearly visible at 330GHZ in Fig. 8.

Table 1 summarizes recent papers on vector modulator phase shifters at frequencies above 100 GHz. It can be seen the presented vector modulator phase shifter offers the highest operating frequency with comparable performance. Furthermore, the presented circuit is also the first phase shifter that has been measured at frequency bands of $f_t$ and above.

Multistage cascade amplification has been utilized in [2], [3], and [6]. Therefore, the highest gain and dissipated DC power have been reported. The end resolution and phase error are directly proportional to the number of bits in the utilized DACs as well as calibration circuitry. Therefore, the higher the number of bits, the better the phase resolution and accuracy.

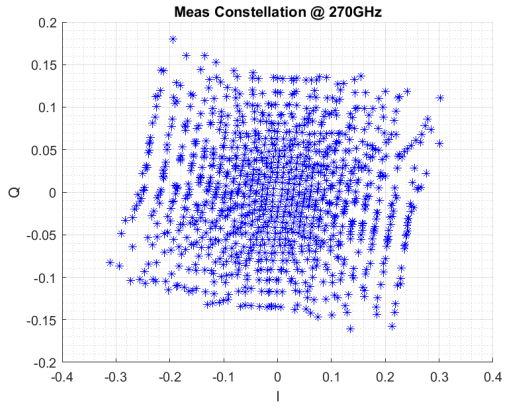



Fig. 6. Measured constellation points of the designed vector modulator phase shifter at 270 GHz.

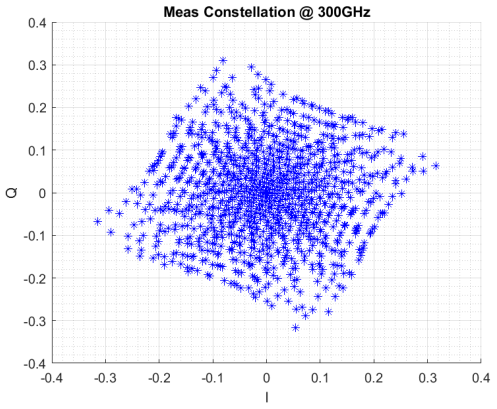



Fig. 7. Measured constellation points of the designed vector modulator phase shifter at 300 GHz.

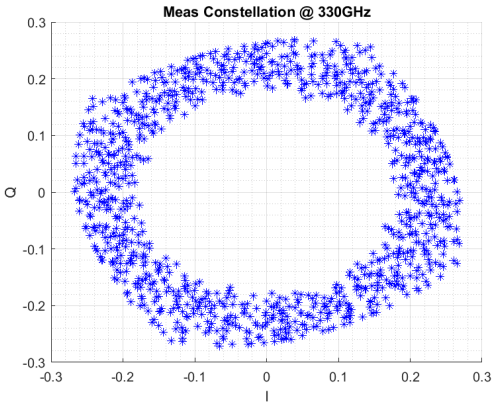



Fig. 8. Measured constellation points of the designed vector modulator phase shifter at 330 GHz.

Table 1. Comparison of the recently published vector modulator phase shifters

| Ref | [1] | [2][a] | [3][a] | [4] | [5] | [6][b] | This work |
|---|---|---|---|---|---|---|---|
| **Technology (nm)** | SiGe 130 | SiGe 130 | SiGe 130 | SiGe 120 | InP 250 | InP | SiGe 130 |
| **Frequency (GHz)** | 210 | 170 | 120-124 | 116-128 | 220-320 | 300 | 270-330 |
| **$f_t/f_{max}$** | 300/450 | 300/450 | 250/340 | 260/340 | 370/650 | 375/Nan | 300/500 |
| **Gain (dB)** | -9.5 | 16[c] | 15[c] | -5.8 | -10 | 10[c] | -10 |
| **Resolution (Deg)** | 15 | 5.625 | Analog Control | 11.25 | 22.5 | Nan | 11.25 |
| **RMS Phase Error (Deg)** | Nan | Nan | Analog Control | 2.2 | 10.2 | Nan | 0.98 |
| **Input $P_{1dB}$** | Nan | -6.2 | -9.3 | Nan | -0.7 | Nan | +1[d] |
| **DC $P_{Diss}$** | 30[e] | 330[f] | 225[f] | 30 | 42 | Nan | 65 |
| **Area ($mm^2$)** | 0.075 | 1.966[g] | 0.1 | 0.405[g] | 0.23[g] | 0.375[g] | 0.023 |

a) Only TX chain is reported here. Original paper reports both TX and RX. b) The design covers only the first quarter of the whole plane, i.e. maximum phase shift of 90°. c) Amplifier embedded front-end. d) Based on simulations. The available equipment did not offer enough drive for the chip to enter saturation. e) The authors defined a range from 0 mA to 012.5mA. f) PA power consumption is included. g) The given dimensions include all the passives, i.e. baluns, etc., pads, and/or extra amplifier circuits.

So, in case of analog control, i.e. [1] and [3], the phase resolution can be the best of all, and RMS phase error marginally approaches zero. In this paper the compression point is reported only based on simulation. This is because the utilized VDI frequency extender cannot provide enough power to compress the phase shifter. The saturated output power of the VDI WR3.4 is measured to be ~3 dBm [11]. Passing this through the ~6.5dB insertion loss probes, the authors managed to drive the chip with –3.5dBm signal power which is insufficient to compress.

## IV. Conclusion

A wideband vector modulator phase shifter with a 60 GHz (20% fractional) bandwidth was presented in this paper. The presented circuit was measured at frequencies 270 – 330 GHz. The circuit is the only vector modulator phase shifter which has been measured to be operational at frequencies above the unity current gain of the technology, i.e. 300 GHz. The designed circuit offers full 360° signal rotation with a –10 dB gain. Compensation technique for translinear loop improved the measured constellation of the phase shifter. To extract the constellation points a statistical processing was performed using multiple reference point scanning.

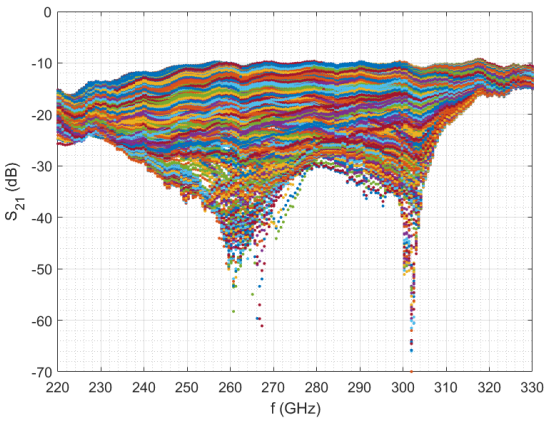



Fig. 9. Measured frequency response, i.e. $S_{21}$, of the designed vector modulator phase shifter at the band of 220 – 330 GHz.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