A Reconfigurable Dual-Mode Tracking SAR ADC without Analog Subtraction

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***Abstract*—In this contribution, it is proposed to limit the number of cycles needed for a successive approximation analog-to-digital converter to digitize a sample, through minimizing quantization search space by analytic derivation of maximum possible sample-to-sample variations. The presented example design of the proposed ADC is an 8-bit 1MS/s ADC with SAR logic customized to incorporate this priori information while no modification has been required to the analog circuitry. In comparison to conventional SAR conversion, the proposed tracking approach yields significant reduction in total power consumption in oversampling mode. The power savings are due to the reduced number of SAR cycles, and voltage variation minimization across DAC capacitors. The design is reconfigurable both to conventional SAR sampling and the proposed tracking scheme. The approach is attractive for SAR ADCs embedded in very low power micro-controllers.**

***Index Terms*—Analog-to-digital converter, SAR ADC, Over-sampling.**

I. Introduction

Most Micro-Controller Units (MCU) incorporate an Analog-to-Digital Converter (ADC) [1]. Thanks to their high power efficiency and flexible sampling rate, Successive-Approximation-Register (SAR) ADCs are popular with low power MCUs, but their bit precision tends to be limited to 12 bits due to linearity issues. Consequently, the MCU vendors provide developers, ADCs with oversampling option to improve the resolution [2]. In its simplest form, the resolution enhancement is achieved through oversampling the signal by factor M (over Nyquist-rate), followed by, e.g. Hogenauer structure and simple FIR filters [3]. However, the flip-side can be a substantial increase of power dissipation [4]. Moreover, in sensor readout interfaces, reconfigurable ADCs that provide different sampling and resolution options, are especially useful, where the ADC is time-multiplexed to digitize different types of input signal with different bandwidth and resolution requirements [5].

A modified oversampling scheme that reduces the power dissipation of the quantization process through cutting number of cycles for each conversion during oversampling, is proposed. The method is based on the observation that in oversampling mode, maximum sample-to-sample variation is constant and deterministic. In an attempt to take advantage of this observation, a tracking ADC is introduced to save power through constraining quantization levels that need to be resolved. The scheme can be an alternative for the commonly used oversampling techniques in conventional ADCs. Our design also supports regular Nyquist-rate sampling and can be reconfigured to various digitization schemes.

Previous designs generally attempt to reduce conversion cycles by quantizing only sample-to-sample variation which necessitate some form of analog subtraction, e.g. authors of [6] propose a modification to the Digital-to-Analog-Convertor (DAC) in order to derive sample-to-sample variations, but this modification prevents employment of bottom plate sampling (and consequently facing charge injection problem). The proposed method in this work uses prior knowledge to limit quantization search space, hence reducing number of cycles required to resolve each sample. In this contribution, contrary to previous works, e.g. Noise Shaping SAR, the idea is not to use the ADC to digitize the difference between the current sample and previous converted value, but instead track the signal through adjust DAC value. In other words. the current conversion is held and is used to resolved the next sample, through minor modifications.

II. Theoretical Concept

The purpose of the following is to derive an analytic expression for determining the maximum change between two consecutive samples, when the input signal has been low pass filtered and is oversampled by a factor of M. Assuming there is a front-end anti-aliasing filter before ADC (which practically is accessible), it is guaranteed that the input signal is low-passed. The fastest changing band-limited and bounded (i.e. amplitude-limited) signal would be a sinusoid with maximum frequency and full dynamic range. Let us assume the Nyquist-rate sampling rate to be f_s , oversampling factor M, and oversampling rate f_{os}. When the highest frequency component in the signal is f_{max}, the sampling rate f_s must be more than $2f_{max}$, but for our purpose in the calculations, one can safely be assume $f_s = 2f_{max}$, leading to over-sampling rate of $f_{os} = 2Mf_{max}$. The signal to be sampled can therefore be expressed as,

$$x(t) = Acos(2\pi f_{max}t + \phi) \tag{1}$$

where A is the amplitude, t is time and ϕ is the phase. The oversampled signal is

$$x[n] = Acos(\frac{\pi n}{M} + \phi) \tag{2}$$

and the difference between two adjacent samples is defined by,

$$D[n] = x[n] - x[n-1] \tag{3}$$

To find the maximum value for the difference (3) in the oversampled signal, the first derivative of the difference is set equal to zero, then using backward differentiation one can solve for n:

$$\frac{\partial D}{\partial n} = \frac{(D[n] - D[n-1])}{1} \tag{4}$$

$$\frac{\partial D}{\partial n} = Acos(\frac{\pi n}{M}) - 2Acos(\frac{\pi(n-1)}{M}) + Acos(\frac{\pi(n-2)}{M}) \tag{5}$$

Setting the above equal to zero ($\frac{\partial D}{\partial n} = 0$) gives,

$$Acos(\frac{\pi n}{M}+\phi) - 2Acos(\frac{\pi(n-1)}{M}+\phi) + Acos(\frac{\pi(n-2)}{M}+\phi) = 0 \tag{6}$$

To simplify the notation, let $x = \frac{\pi n}{M}$ and $b = \frac{\pi}{M}$, and using angle sum and difference identities, we get

$$\begin{aligned} &Acos(x+\phi) - 2Acos(x+\phi)cos(b) - 2Asin(x+\phi)(b) \\ &\quad + Acos(x+\phi)(2b) + Asin(x+\phi)(2b) = 0 \end{aligned} \tag{7}$$

Let assume $M \gg \pi$ (which regularly is the case, in our experiments $M \geq 32$), $b \approx 0$ and using Small Angle Approximation the following is resulted,

$$\begin{aligned} &Acos(x+\phi) - 2Acos(x+\phi)(1-b^2/2) - 2Asin(x+\phi)(b) \\ &\quad + Acos(x+\phi)(1-2b^2) + Asin(x+\phi)(2b) = 0 \end{aligned} \tag{8}$$

Most of the terms in the above expression cancel out each other, leaving

$$-(b^2)Acos(x+\phi) = 0 \tag{9}$$

from which solving for x yields

$$x = \frac{k\pi}{2} - \frac{M\phi}{\pi}, k \in \mathbb{Z} \tag{10}$$

Therefore, D_{max} for $n = \frac{k\pi}{2} - \frac{M\phi}{\pi}$ becomes

$$D_{max} = \pm Asin(\pi/M) \tag{11}$$

Small angle approximation can be applied again and hence the maximum range is approximated as $\pm\frac{A\pi}{M}$. Having the current sample $x(nT_s)$ and its quantized equivalent, the next sample would be in the range limited to $\pm\frac{A\pi}{M}$,

$$x[(n+1)T_s] = x[nT_s] \pm \frac{A\pi}{M} \tag{12}$$

Hence, the search space of the ADC can safely be limited to the range of $\pm\frac{A\pi}{M}$. This can be exploited to reduce power consumption of ADCs embedded in MCUs.

In the above analysis the signal was assumed to be perfectly low-passed, whereas in read world scenarios higher intrusive signals might be present. As it is shown in following, the ADC algorithm can get back on track once such sudden inferences occurs.

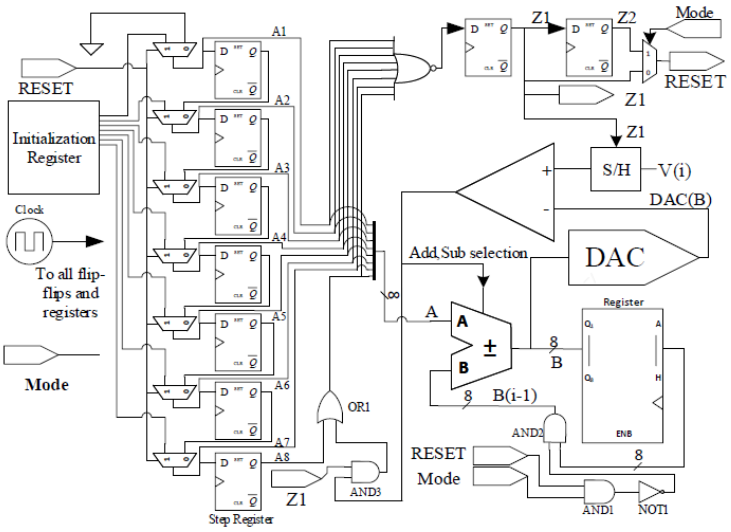

Fig. 1. Digital logic for realization of the proposed dual-mode SAR ADC.

III. Proposed ADC

A. General Description

Figure 1 shows the circuit diagram of the proposed ADC. As shown, the main building blocks of the ADC consist of an 8-bit shift register, Z1 and Z2 delay generation unit, arithmetic unit and a successive approximation converter (ADC core). The ADC core itself is implemented by a binary weighted capacitor array that perform digital to analog conversion (DAC), a comparator and a passive sample-and-hold circuit. The details and considerations of the unit capacitor in the DAC capacitor array as well as the comparator are similar to [7]; but the unit capacitor is 15fF in this design. Also, the arithmetic unit is composed of an 8-bit adder/subtract, an 8-bit delay cell and few digital logic gates for control and mode selection. Based on the mode pin status, the ADC operates in regular mode or oversampling mode. The functionality of the proposed ADC is described in the next subsection.

B. Sampling Modes

As explained earlier, the proposed ADC digitizes the analog value in successive approximation manner, but instead of conventional logic, its range and steps are adjusted based on mode of operation. Algorithm 1 and Algorithm 2, present detailed procedural description of each mode. Also, in Fig. 2, the sampling in tracking mode is depicted to help understanding of the concept.

In regular SAR mode similar to conventional logic, the DAC value is set to zero at the end of each conversion but in tracking mode the DAC value is maintained. For regular SAR mode the user must set the initial value of the shift registers to "1000000" (for 8-bit ADC). For proposed tracking mode the initial value depends on the calculated maximum sample to sample variation:

$$IntitialValue \geq \lceil \frac{D_{max}(DynamicRange)}{(2^N - 1)} \rceil$$
$$= \lceil \frac{2Asin(\frac{\pi}{M})}{2A}(2^N - 1) \rceil = \lceil sin(\frac{\pi}{M})(2^N - 1) \rceil \quad (13)$$

Where N is number of bits. For example, in case of an 8-bit ADC operating with oversampling rate of 64 the shift register initialization value is "00001000". This means, in this example, only five cycles are required for conversion of each sample. The use of fewer cycles results in saving of energy required for each conversion. In addition, for most of code transitions the DAC does not need to be reset, which results in avoiding the discharge of MSB capacitors. This leads to extra power savings at DAC. Operation of the scheme is illustrated in Fig. 1 where the ADC is configured to function in regular SAR mode or in the proposed tracking SAR mode via setting the Mode bit '1' or '0', respectively. In Fig. 1, Algorithm 1 and Algorithm 2, B represents digital output, $B(i-1)$ denotes digital output from previous cycle, the Mode bit is set by user while RESET, Z1 and Z2 are generated within the circuit.

The RESET signal is used to initialize the step shift register in both regular mode and in tracking mode, the signal from Z2 (multiplexed to RESET) is used to delay the initialization of the shift register by an additional clock cycle to let the comparator to compare the current analog sample with the quantized version of the previous sample. The design enables exploitation of sample to sample adjacency in oversampling mode, while maintaining the option to use the ADC also as a regular SAR. In both operation modes the delay flip-flop Z1 is used to indicate end of conversion.

Algorithm 1: SAR ADC regular mode algorithm

Result: Digital version of the input analog sample, B.
Initialization Register (IR) is set by user; Mode is selected by user; B is binary output; DAC(B) is analog equivalent of B; *IR* ← "10000000"
Step 1. Take sample, S/H ← V(in)
Step 2. StepRegister ← *IR*
B(i-1)← "00000000"
B ← B(i-1)+$StepRegister$
Step 3. if *StepRegister* $\neq 0$ **then**
  StepRegister ← StepRegister $\gg 1$;
  if *V(in)>DAC(B)* **then**
    B ← B(i-1)+ StepRegister;
  else
    B ← B(i-1)-StepRegister;
  end
  jump to **Step.3**;
end
if *not(V(in)>DAC(B))* **then**
  B ← B(i-1)-1;
end

In the regular mode the quantized value of a previous sample is ignored, while in the tracking mode the previous value on the DAC is held. In Fig. 1 blocks AND1, NOT1 and AND2 are used for this selection. The control signals are automatically generated using data in the shift register. At each clock cycle, data in the shift register is moved one bit to the right, generating a step value to be added or subtracted. An 8-bit asynchronous ripple-carry adder–subtracter is connected to the output of shift register (A1 being the MSB), and one clock cycle delayed version of quantized output, $B(i-1)$. The comparator's output controls the addition/subtraction mode selection of the adder-subtracter. In addition, since in the last cycle all bits in the shift register have already been shifted out, Z1 is used as LSB (AND3 and OR1). Note, for applications that only require implementation of the tracking mode the circuit can significantly be simplified.

Algorithm 2: Tracking mode algorithm

Result: Digital version of the input analog sample, B.
Initialization step is as described in Algorithm 1 but for tracking mode, $IR \leftarrow \lceil sin(\pi/M)(2^N - 1) \rceil$
Step 1. Take sample, S/H ← V(in)
StepRegister ← *IR*
(note that the DAC value and the output, B, are held from previous conversion)
B ← B(i-1)+$StepRegister$
Step 2. if *StepRegister* $\neq 0$ **then**
  if *V(in)>DAC(B)* **then**
    B ← B(i-1)+ StepRegister;
  else
    B ← B(i-1)-StepRegister;
  end
  jump to **Step.2**;
end
if *not(V(in)>DAC(B))* **then**
  B ← B(i-1)-1;
end

IV. Results and Discussion

Initially, a behavioral simulation using MATLAB was carried out to verify the functionality of the proposed ADC. Subsequently, a transistor level circuit simulation in 90 nm CMOS process with an HSPICE model was carried out to investigate the power consumption in both regular and proposed oversampling mode with different oversampling ratios. Specifications of the design is presented in Table I. The power consumption for different oversampling ratios were estimated through simulations. The summaries of the findings are in Table II which shows energy consumption per sample reduces proportionally to the oversampling ratio. Figure 2 shows the power spectral density of the proposed ADC architecture in tracking mode for $OSR = 64$.

The proposed architecture serves as an example on exploiting sample-to-sample variation without having to carry out analog subtraction. Although similar ideas have been investigated before [6][8], to the best knowledge of authors, general approach of the previous works was to quantize the

TABLE I
PROPERTIES SUMMARY OF THE SAMPLE SAR ADC.

Specification	Value
Technology	90nm CMOS
Resolution	8
ENOB*	7.4
Supply Voltage	1V
Max. Sampling Rate	1 MS/s
Power Consumption	12.9 μW

*Regualar mode, Nyquist rate.

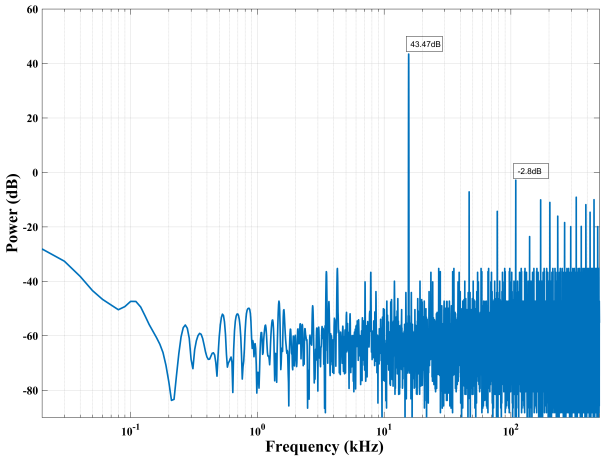

Fig. 2. Power Spectrum of the ADC in proposed oversampling mode with oversampling ratio of 64 (SFDR=46.3dB)

analog difference of two consecutive samples while in this work the search space is adjusted digitally. Analog subtraction requires extra analog circuitry, which introduces more design constraints. In addition, the proposed approach can be reconfigured to conventional SAR logic mode (either for Nyquist-rate sampling or oversampling). Furthermore, though the digital complexity of the design is slightly higher that conventional SAR logic, the power saving can compensate this to a large degree. Moreover, low power digital design techniques can be employed without having to compromise the performance, to further reduce power consumption.
Although, the presented implementation of the design does not achieve the best FoM in Table III, where comparison with similar works including Noise-Shaping (NS) SAR ADCs, is provided. However, as indicated before, we aimed at a reconfigurable architecture that can function as a regular SAR with more efficient oversampling mode via taking advantage of limited sampling-to-sample change. Please note, as it is presented in Table II, in the proposed design, the power dissipation per sample scales down with increasing the sampling frequency. Furthermore due to large logic section, further power lessening through voltage scaling can be envisioned.

V. CONCLUSION

Taking advantage of how sample-to-sample variation is limited can provide for substantial energy efficiency improvements for SAR ADCs. Our contribution shows how this can be accomplished by modifying only the digital parts of the conversion logic, and minimum restriction is imposed on analog circuits. The digital section can enjoy power reduction techniques such as voltage scaling without having to compromise circuit functionality. The presented digital logic supports both regular SAR and proposed tracking mode of operations. The method is useful in multi-channel ADCs used in embedded micro-controllers.

TABLE II
ESTIMATED POWER CONSUMPTION WITH RESPECT TO OSRS

OS Mode	OSR*	Variation	Initial	Cycles	pW/S
Regular	Any	Max.	10000000	9	12.8
Tracking	32	25	00100000	7	8.03
Tracking	64	12.5	00001000	5	6.33
Tracking	246	3.1	00000100	4	5.53

* master clock was kept constant and the input frequency was scaled down.

TABLE III
COMPARISON WITH THE RELATED WORKS

	Ref. [9] (Sim.)	Ref. [10] (Chip)	Ref. [3] (Chip)	This Work (Sim.)
Bandwidth	60 KHz	20 MHz	11 MHz	2-500 KHz
ENOB	9.55	9.8	10	7.4
Power	2.97 μW	1.8mW	806 μW	13 μW
Technology	180 nm	180 nm	65 nm	90 nm
FoM	36.9 f	70.2 f	35.8 f	76.9 f
Architecture	SAR	Reconfigurable	NS-SAR	Tracking SAR
FOM	$\frac{Power}{B.W \times 2^{ENOB}}$			

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