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Speed Up Technique by Pre-charging Load Capacitor in SC Residue Circuit

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***Abstract*— A novel passive charge re-distribution technique for switched capacitor residue circuits used in pipeline analog to digital converters is presented. It is based on pre-charging the load capacitor to the proper voltage during the previous phase, connecting the pre-charged load capacitor to the output of the Operational Trans-conductance Amplifiers (OTA) during the evaluation phase, and hence pulling the charge so that the initial voltage step in the OTA input is instantaneously minimized. The OTA therefore skips the slew region, and enters into the linear settling region, leaving just a minor charge to be moved by the OTA. A double sampling, OTA sharing SC residue with 1.5-bit MDAC is designed using 90-nm generic CMOS PDK with 1.2-V supply voltage. Simulation results of a 10-bit, 100 MS/s SC residue with proposed technique show that the conversion rate can be increased over 30% compared to the conventional SC residue circuit.**

***Index Terms*—pre-charge, initial input voltage, pre-charged load capacitor, settling time reduction, switched capacitor, pipeline ADC.**

I. Introduction

For high resolution and high speed applications, the pipeline analog to digital converter (ADC) represents the most suitable architecture, and a switched-capacitor (SC) residue amplifier is a basic building-block in the most pipeline ADCs. One of the main design bottlenecks in high speed ADC is to obtain a very precise and fast settling by the end of the evaluation period with minimal power consumption. Numerous ways of either enhancing the class AB operation of the OTA or making its bias current signal or time-dependent can be found in the literature [1-6]. Dominantly they affect the internal design and dimensioning of the OTA itself.

SC circuits use Operational Trans-conductance Amplifiers (OTAs) to transfer charge, and there will be large transient voltage spikes Vi0 in the inputs of the OTAs. If the initial step exceeds the linear input range Vlin of the OTA, it drives the OTA into slewing, where the OTA output current gets limited to Imax. The time spent in slewing is taken away from the linear settling time, causing highly non-linear settling error. In this paper a passive capacitive pulling technique is proposed where a properly charged load capacitance is used to pull the charge so that the initial step of OTA is instantaneously minimized close to the final steady-state. This technique is completely outside the OTA structure and hence it does not affect its dimensioning, offset properties, and cause any new internal time constants. This approach can be compared to split-CLS technique [7], which uses two different OTAs for the estimation and level shifting phases, improving the overall performance in terms of power, speed and accuracy. In CLS the size of the level shifting capacitor influences both the feedback factor and the total charging capacitance of the structure.

Section II describes the concept of charge redistribution in a double sampling OTA sharing SC residue circuit of a pipeline ADC. Section III introduces various implementations of charge redistribution speed-up technique. Section IV presents the circuit implementation of the selected method. Section V shows simulated results, Section VI gives the conclusions.

II. Charge Redistribution of a Traditional SC Residue Circuit

A. Conventional Structure of SC Residue Circuit in a Pipeline ADC

Fig. 1 shows a double sampling, OTA sharing SC residue circuit that is used in pipeline ADCs at the present time. The residue OTA has two sets of capacitor banks (bank A and bank B). When the input signal is being sampled by one capacitor bank, the other capacitor bank is connected to the OTA for the evaluating phase.

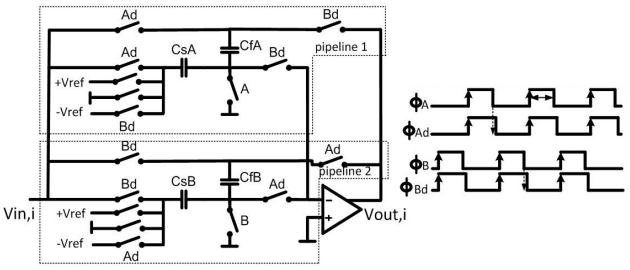

Fig. 1. Double sampling, OTA sharing SC residue circuit used in pipeline ADC.

B. Charge Redistribution Equations

Fig. 2 shows the capacitor connection of the 1st and the following stage at the end of sampling phase ϕA and at the beginning of evaluation phase ϕB. At the very beginning of ϕB phase, the OTA itself is assumed that it has no effect yet, and the total charges are almost instantaneously and passively redistributed. The instantaneous charge redistribution results into the initial values at the input and the output of the OTA. V_{i0}

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and V_{o0} are the initial points at the input and output of the first OTA respectively, and $V_{i0,i+1}$ and $V_{o0,i+1}$ are the following stage initial points. These voltages are the initial points where the OTA starts settling from. Since the total charge in the node A1 or B1 has no path to move in the beginning of ϕB, the total charge in these nodes in the beginning of the evaluation phase is the same as at the end of ϕA. The charge redistribution equations in the SC residue circuit are shown in (1), from which the initial voltages Vi0 and Vo0 can be calculated. V_1 represents the previous output voltage of next stage (Vo,pre,i+1) in the double sampling, OTA sharing SC residue circuit. V_2 represents the next stage reference voltage of previous evaluation phase (Vref,pre,i+1). V_1 and V_2 depend on the previous state of the following residue stage.

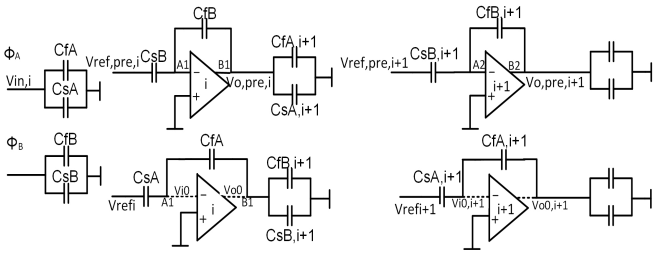

Fig. 2. Charge redistribution in a double sampling OTA sharing SC residue circuit used in pipeline AD converter.

$$\begin{aligned} &A1: CsA\times\left(V_{i0}-V_{refi}\right)+CfA\times\left(V_{i0}-V_{o0}\right)=CsA\times\left(0-V_{in,i}\right)+CfA\times\left(0-V_{in,i}\right)\\ &B1: CfA\times\left(V_{o0}-V_{i0}\right)+V_{o0}\times\left(C_{fB,i+1}+C_{sB,i+1}\right)=CfA\times V_{in,i}+V_1\times C_{fB,i+1}+V_2\times C_{sB,i+1}\end{aligned} \quad (1)$$

When Vi0 is smaller than the linear input range Vlin of the OTA, the SC circuit operates fully linearly and the charge-transfer error is proportional to the initial input Vi0. When Vi0 is large, slewing of the OTA results in an exponential increase of the error, which is a major cause of non-linear distortion. Hence Vi0 is the key factor which determines the amount of distortion.

III. Charge Redistribution Speed-up Technique

A. Overview of Charge Redistribution Speed-up Technique

The main idea of charge redistribution technique is to add an appropriate amount of pre-calculated charge Qpre at the output of the OTA at the beginning of the evaluation period. The injected Qpre helps to move the charge and forces Vi0 close to zero, so that the OTA has very little linear correction to accomplish, and the output voltage reaches desired value quickly as well.

B. Various Ways to Inject a Pre-calculated Charge Qpre

One technique is to inject a dynamically controlled pumping current pulse Ipump=Qpre/Δt with a fixed short pulse Δt into the output of the OTA at the beginning of the evaluation phase. If the load capacitor is emptied before the evaluation phase, the charge redistribution equations get the form shown in (2). This current pumping idea will be studied in a future paper.

$$\begin{aligned} &A1: CsA\times\left(V_{i0}-V_{refi}\right)+CfA\times\left(V_{i0}-V_{o0}\right)=CsA\times\left(0-V_{in,i}\right)+CfA\times\left(0-V_{in,i}\right)\\ &B1: CfA\times\left(V_{o0}-V_{i0}\right)+V_{o0}\times\left(C_{fB,i+1}+C_{sB,i+1}\right)=CfA\times V_{in,i}+Ipump\times\Delta t\\ &\Longrightarrow Ipump=\frac{5V_{in,i}\times CsA-3V_{refi}\times CfA}{\Delta t}\end{aligned} \quad (2)$$

In this paper the pulling is implemented by pre-charging the load capacitor CL (the sampling capacitor of the next stage) to the proper amount Qpre=Vpre×CL before connecting it to the output of the OTA. The charge redistribution equations of this pre-charging load capacitor method are shown in (3).

$$\begin{aligned} &A1: CsA\times\left(V_{i0}-V_{refi}\right)+CfA\times\left(V_{i0}-V_{o0}\right)=CsA\times\left(0-V_{in,i}\right)+CfA\times\left(0-V_{in,i}\right)\\ &B1: CfA\times\left(V_{o0}-V_{i0}\right)+V_{o0}\times\left(C_{fB,i+1}+C_{sB,i+1}\right)=CfA\times V_{in,i}+V_{pre}\times\left(C_{fB,i+1}+C_{sB,i+1}\right)\\ &\Longrightarrow Vpre=2.5\times Vin,i-1.5\times V_{refi}\end{aligned} \quad (3)$$

If all the capacitors are equal, a simple expression for Vpre is derived from (3) by forcing Vi0 to zero. As shown in (3), Vpre does not depend on the previous states, but is only affected by the sampled voltage Vin,i and reference voltage Vrefi.

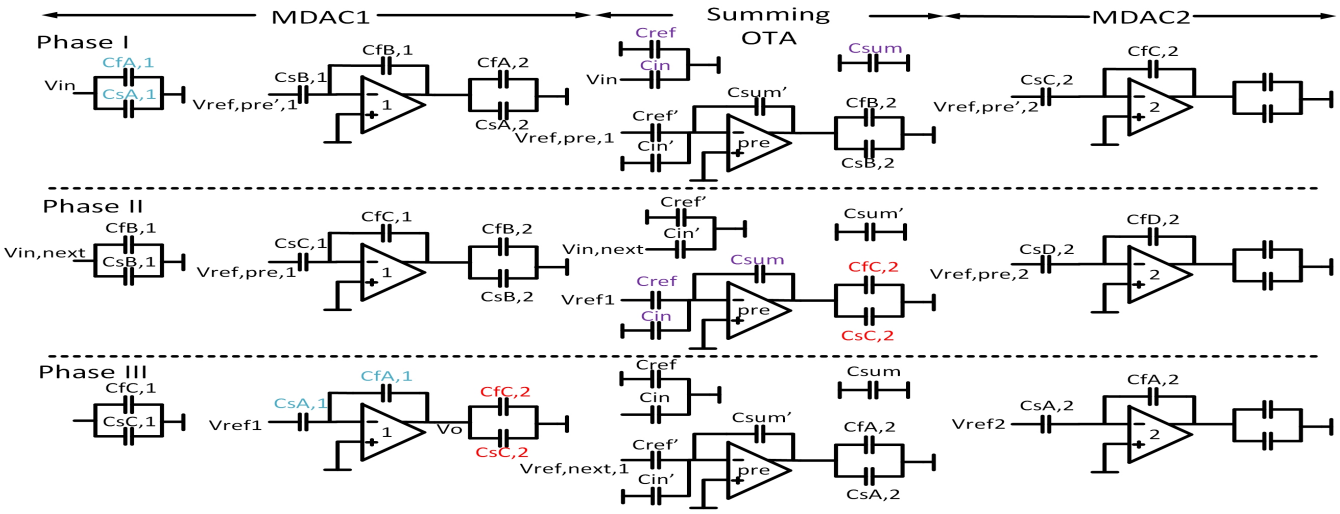

Fig. 3. Pre-charge load capacitor speed-up technique.

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IV. Circuit Implementation of Pre-charge Load Capacitor Speed-up Technique

A. Architecture

To pre-charge the load capacitors CL of a residue OTA stage to Vpre given in (3): Vpre=2.5×Vin,i-1.5×Vrefi, a circuitry is needed for calculating Vpre and sample it into CL. For this purpose, a separate summing SC stage (pre-charging block) is added between the 1st and 2nd multiplying Digital-to-Analog Converter MDAC (i.e., the residue stage) as illustrated in Fig. 3. Asingle-ended configuration is shown here for simplicity, but the actual implementation is fully differential. As usual, the residue voltage of MDAC1 is generated and sampled onto the sampling capacitors of MDAC2.

To allocate enough time for pre-charging the load capacitor of the 1st stage, it is necessary to introduce one full sample time delay for the processing. This means that in the double-sampling 1st stage three capacitor banks are required instead of two; In the 2nd stage, where the sampling caps will be also pre-charged, four capacitor banks are required. The sampling frequency is still fs, but the use of the capacitor banks rotates at fs/3 in the 1st and fs/4 in the 2nd stage, as shown in Table I.

TABLE I
CAPACITOR BANK ARRANGEMENT OF EACH PHASE

		phase I	II	III	IV
MDAC1	CsA,1 CfA,1	Sampling	------	Evaluation	Sampling
	CsB,1 CfB,1	Evaluation	Sampling	------	Evaluation
	CsC,1 CfC,1	------	Evaluation	Sampling	------
MDAC2	CsA,2 CfA,2	Sampling	------	Evaluation	Pre-charged as CL
	CsB,2 CfB,2	Pre-charge as CL	Sampling	------	Evaluation
	CsC,2 CfC,2	Evaluation	**Pre-charged as CL**	Sampling	------
	CsD,2 CfD,2	------	Evaluation	Pre-charge as CL	Sampling
Summing OTA	Cin	Sampling	Pre-charge CL	Sampling	Pre-charge CL
	Cref Csum	Empty Charge		Empty Charge	
	Cin'	Pre-charge CL	Sampling	Pre-charge CL	Sampling
	Cref' Csum'		Empty Charge		Empty Charge

The three capacitor banks of the MDAC1 alternate in order A→B→C→A. After the input is sampled onto the capacitor bank A during the phase I, the sampled signal is held in the capacitor bank A during the phase II, during which time the pre-charge voltage Vpre is calculated into the load capacitor (bank C of MDAC2) of the 1st stage. Then in phase III the capacitor bank A is connected as feedback around MDAC1 and the pre-charged load capacitor (bank C of MDAC2) is connected its output for pulling and sampling.

In MDAC2 two sets of sampling capacitors are necessary, the one being pre-charged and the other one being sampling. Hence, the four capacitor banks are rotating in order of A→B→C→D→A. While the bank A is sampling during the phase I, bank B is being pre-charged, bank C is in the evaluation operation and D is not used.

During the phase I shown in Table I, while the input voltage Vin,i is sampled onto CsA and CfA of MDAC1, Vin,i is also sampled by Cin of summing OTA shown in Fig. 4 by clock ctrla. Clocks ctrlap and ctrlA go down simultaneously to make sure that the same input value Vin,i is sampled by CsA and CfA and Cin of the summing OTA. At the end of phase I, the reference voltage Vref1 is selected by a 1.5-bit ADC and a reference selector. Then Vref1 is held during the building the pre-charge voltage and further during phase III for evaluation operation of MDAC1. After entering phase II, the summing OTA pre-charges sampling capacitors CsC and CfC of MDAC2 to Vpre. During phase III the pre-charged CsC and CfC of MDAC2 are connected to the output of MDAC1 as the load capacitor, and CfA and CsA are connected to the feedback path of MDAC1. Note that the first stage needs 3T to finish processing one input sample, determining the bits, and passing the residue to the 2nd stage, and each successive stage needs 2T to finish processing the sample and propagate to the next stage. Hence the total data latency is 3T+8×2T=19T which is larger than in normal pipeline structure. The proposed technique is implemented only for pre-charging the load capacitor of the first stage, so that the 1st stage requires one and the 2nd stage two additional capacitor banks, while the other eight stages of 10-b ADC keep the same as the original structure. Therefore, the extra area cost of these additional capacitors with respect to the total area of the original ADC is only approximately 10%.

B. Calculating the Pre-charge Voltage Using a Summing Amplifier

The proposed technique requires that the proper pre-charged value is calculated and then pre-charged into the load capacitors of the summing amplifier. This is implemented by the summing amplifier shown in Fig. 4. The parallel time-interleaved switched capacitor summing OTA has two capacitor banks working in opposite clock phases to implement the pre-charge equation (4).

$$Vpre = 2.5 \times Vin,i - 1.5 \times V_{refi} = \frac{Cin}{Csum} \times Vin,i - \frac{Cref}{Csum} \times Vrefi \quad (4)$$

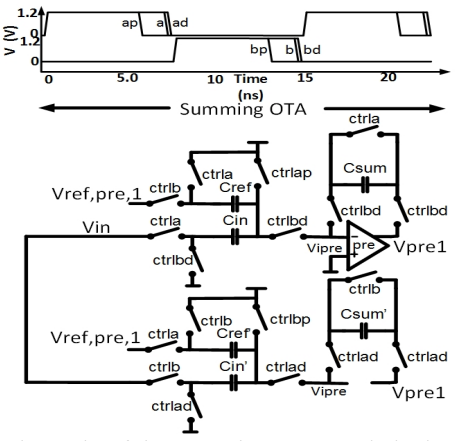

Fig 4. Schematic of the summing OTA and clock phases

V. Simulation Results

To validate the proposed settling time reduction technique, a double sampling, OTA sharing SC residue circuit based on a SHA-less architecture with 1.5-bit MDAC was designed using 90-nm generic CMOS PDK and 1.2-V supply voltage. The

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input signal frequency fin is 25.37MHz, and sampling frequency of the conventional structure is 100MHz. A two-stage folded cascaded OTA with a Miller capacitor is used as the main OTA in both the original and the proposed architecture. A simple single stage telescopic OTA is used for the summing OTA in the pre-charge circuit block since the accuracy of the pre-charge is relaxed. The OTAs, digital logic circuit and switches were implemented at transistor level, and the comparators were modelled by Verilog-A. The same on-resistance of switch was used in both the original and proposed structure. The Spectre tolerance parameters of simulations were gmin=1e-14, reltol=50e-06, Vabstol=0.6e-6, iabstol=1e-15, maxtimestep=156.6ns, errpreset=conservative. Fig. 5 depicts the initial input voltage Vi0 of the OTA versus input voltage without and with the proposed speed-up technique. Vi0original1,2,3 were collected by several combinations of Vo,pre,i+1, Vref,pre,i+1 and Vref1 which all affect the initial input voltage under normal operation. The maximum Vi0 of original initial input voltage can reach 246mV, while the pre-charging method reduces Vi0 approximately to +/- 30mV.

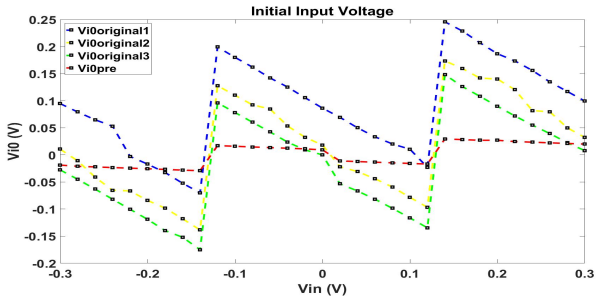

Fig. 5. Vi0 versus varies input voltages with the speed-up technique.

A. Settling Transient Response

Fig. 6 illustrates the settling transient responses of the SC residue circuit without and with the proposed pre-charge technique. Vi,original and Vo,original of Fig. 6 (a) are the input and output transient voltages of the OTA during the evaluation phase without the proposed technique. Vi,pre and Vo,pre of Fig. 6 (b) are the corresponding input and output transient voltages with the proposed technique. In the original structure, the biggest initial input voltage happens when the input signal Vin,i is around ±1/4Vref. Here Vi,original peaks to 246 mV when Vin,i = 140mV. Since Vi0 is larger than Vlin, OTA enters in the slew rate region first, causing a signal-dependent delay before the final linear settling. By using the pre-charging technique, the initial input voltage drops to 29.5mV which makes the OTA to skip the slew rate region, and enter in the linear settling region immediately. The settling accuracy is presented by the base-10 logarithm value of the absolute value of the difference between the real output voltage (Voreal) and ideal output voltage (Voideal): $\log_{10}|\text{Voreal-Voideal}|$.

For the example in Fig. 6 $\log_{10}|\text{Voreal-Voideal}|<-3.96$ means that the output voltage of the evaluation phase meets the accuracy requirement of 10 bits. As shown in Fig. 6 the proposed SC residue circuit reaches the required accuracy in 5.5ns, while the original structure needs 8ns.

With the proposed pre-charged technique, the initial input voltage range of the MDAC1 OTA is reduced and is within the Vlin voltage range, as seen in Fig. 5. Hence, we can lower the slew rate specification of the main OTA to get the same resolution as the original structure, and subsequently the power consumption of the main OTA is lower. The switched capacitor summing OTA does consume additional power, but the total power consumption of the main and summing OTA remains the same – so we achieve 30% higher sampling rate with the same power consumption.

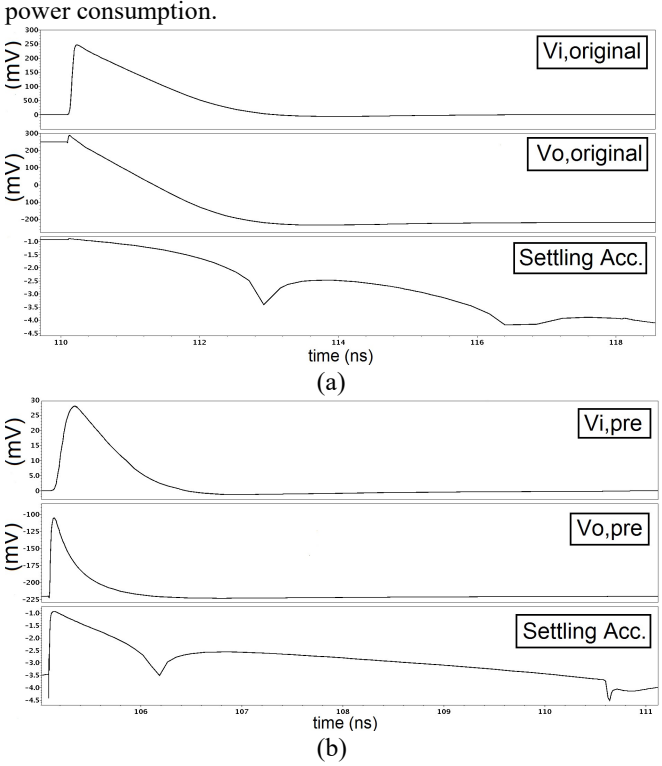

Fig. 6. (a) Simulated settling transient responses without the pre-charged technique (b) with the pre-charged technique

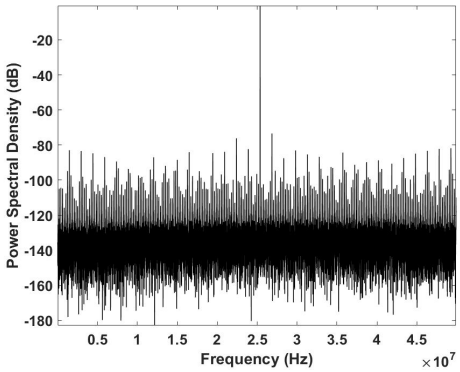

Fig. 7 (a) FFT spectrum of conventional SC residue circuit with fs=100MHz

Fig. 7 (a) shows the simulated 65536-point FFT output spectrum obtained from circuit simulation for the conventional structure with sampling frequency fs=100MHz and Fig. 7 (b) shows the output spectrum with the proposed pre-charged method with fs increased to 133MHz. Table II summarizes the FFT performance comparison of the two SC residue circuits. The spurious-free dynamic range SFDR and the signal-to-noise

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and distortion ratio SNDR of the conventional structure with fs=100MHz were 73.4 and 67.6dB respectively, resulting in effective number of bits ENOB of 10.94 bit. The SFDR and the SNDR of the pre-charge speed-up structure with fs=133MHz were 73.6 and 67.2 dB, resulting in the ENOB of 10.87 bit. With the proposed pre-charged method, the sampling rate is increased about 30% with the power consumption remained the same, but still can achieve the same performance as the conventional structure.

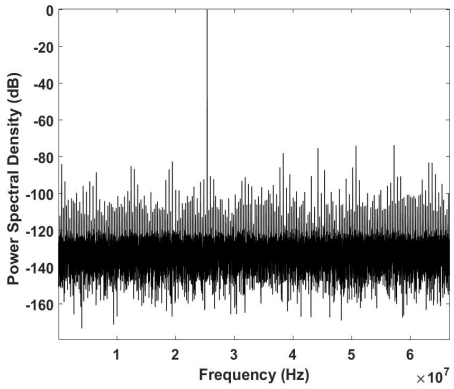

Fig. 7 (b) FFT spectra of proposed pre-charged technique with fs=133MHz

TABLE II
PERFORMANCE COMPARISON OF SC RESIDUE CIRCUIT WITH/WITHOUT PRE-CHARGE TECHNIQUE

	SC residue circuit	
	original circuit	*pre-charge Method*
Sampling frequency	100 MHz	133 MHz
SNDR	67.6 dB	67.2 dB
SFDR	73.4dB	73.6dB
Supply voltage	1.2 V	
Technology	90 nm	
ENOB	10.94bits	10.87 bits

Table III compares the main characteristics of the OTAs used in the original and pre-charge structure. The total power consumption of the SC residue circuit is dominated by the main OTA and summing OTA of pre-charge circuit block. The total static current consumption of 1016uA with the original OTA and without the proposed method results in static power dissipation of 1.22mW. With the realaxed main OTA and pre-charge summing OTA the total static current consumption is 897uA (465uA+432uA) resulting in static power dissipation of 1.08mW. Despite the slightly smaller power dissipation, the sampling frequency can be increased from 100MHz to 133MHz due to faster settling. The additional dynamic power of the proposed circuit is due to pre-charging the load capacitor to Vpre. The worst case is when the load capacitor is pre-charged to the maximum voltage (Vpre,max) of Vpre, then completely discharged to 0V during every clock cycle. The estimation of the worst additional dynamic power (Pdynamic,worst) is equal to $C\times(Vpre,max)^2\times fs,pre$ = 0.01776mW where C is the sampling capacitor of the next stage and fs,pre is the sampling frequency of the proposed structure. Compared to the static power dissipation, the additional dynamic power can be ignored.

The complexity of the pipeline stage is increased, more switches and clock phases are needed. . Also, the pre-charge circuit block does consume some power. However, due to the power saving of the relaxed main OTA, the total power consumption including the increased complexity remains almost the same as the conventional structure, but the sampling frequency can be increased by 30% while still achieving the same dynamic specifications as compared to the conventional SC residue circuit.

TABLE III
OTA PERFORMANCE COMPARISON

OTA	**Original main OTA in SC Without Pre-charged method**	**Relaxed main OTA in SC with Method 2**	**pre-charge summing OTA**
Accuracy	10b	10b	3%
OTA structure	two stage folded cascode OTA with Cc	two stage folded cascade OTA with Cc	one stage telescopic OTA
PhaseMargin	55 degree	71 degree	75 degree
Gain	71dB	71dB	300
Unit Gain Bandwidth	520 MHz	540 MHz	560MHz
Slew Rate	248V/us	62.4 V/us	266V/us
Load capacitor	2.375pF	2.375pF	------
Cs,Cf	0.75p	0.75p	------
Cc	0.5pF	0.5pF	------
Total Static Current	1016uA	465uA	432uA
Total settling time	8ns	5.5ns	7.1ns

VI. CONCLUSION

A double sampling, OTA sharing SC residue circuit based on a SHA-less architecture with 1.5 bits MDAC is designed using 90-nm standard process with 1.2-V supply voltage. An additional one-sample delay and one additional time-interleaved capacitor bank is introduced to pre-charge the load capacitors of the first stage so that its initial input step is minimized. As the 1st OTA skips the slew rate region it settles more quickly, and in this case, it was possible to increase the sampling frequency by 30 %. In addition to the one-sample delay, the pre-charging logic requires one additional summing amplifier, but the relaxed accuracy requirements allow for implementation with simpler and power efficient circuity.

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