

# Designing at Millimeter-Wave: Lessons from a Triple Coil Variable Transformer

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**Abstract**—This paper presents a triple coil variable transformer that can be used to design RF blocks for millimeter-wave 5G transceivers. By employing a third coil with a varying capacitive load in a two coil transformer, simultaneous dual band or a wide-band response can be achieved ranging from 20 GHz to 50 GHz. The idea is validated using simulations and fabricated using 45 nm CMOS SOI technology. In addition, reasons for mismatch between the simulated and measured results are studied. Furthermore, a modified switching configuration is proposed to alleviate the problems with the original design.

**Index Terms**—CMOS, transformer, millimeter-wave, switch, 5G.

## I. INTRODUCTION

To cope with the massive bandwidth requirements for 5G, wide-band systems operating at centimeter or millimeter-wave (mmWave) frequencies are required [1]. 3rd generation partnership project (3GPP) new radio (NR) FR2 standard has allocated several new mmWave frequency bands ranging from 24 GHz to 40 GHz [2], for example, bands n258 (24.25 GHz to 27.5 GHz), n257 (26.5 GHz to 29.5 GHz), n260 (37 GHz to 40 GHz), and n261 (27.5 GHz to 28.35 GHz) propose 3 GHz wide frequency bands. Hence, 3GPP NR FR2 compatible circuits should inherently be wide-band or preferably dual band.

In this paper, we propose a triple coil variable transformer structure compatible for 3GPP NR FR2 circuit blocks. At the core of the triple coil variable transformer is a two coil transformer to which a third overlapping coil with a switchable capacitive load is added. As a result, the behavior of the transformer can be modified to either produce a very wide-band response or provide simultaneous dual band response. Furthermore, the vertical positioning of the third coil can also be included in the design variable space.

In order to verify the idea, a test circuit was designed and manufactured using GLOBALFOUNDRIES 45 nm CMOS SOI process. Due to the experimental nature of the circuit, previously designed inductors and switches were used to build the prototype. The measured results show that, unfortunately, the fabricated circuit does not completely match the simulated operation, therefore, in this paper we also studied the reasons behind the discrepancy between simulated and measured results. Furthermore, we propose improvements to rectify the issues.

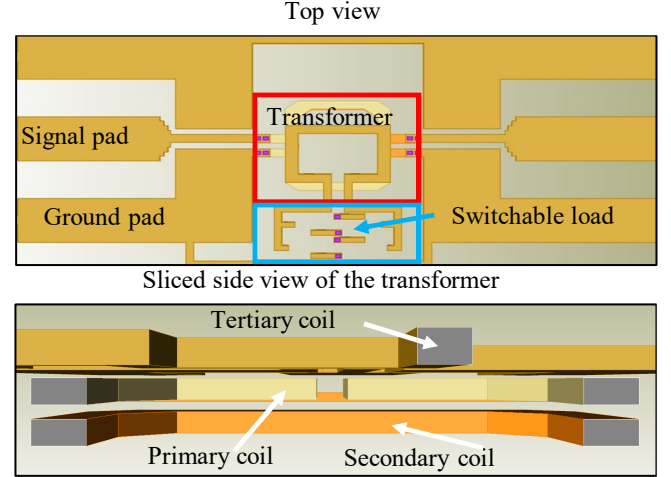


Fig. 1. Top and side view of the triple coil variable transformer.

The organization of the paper is as follows, in Section II, the fabricated circuit is described, followed by the results in Section III. In Section IV, the measured results are analyzed along with simulated data. The circuit improvements are proposed in Section V. Conclusions are drawn in Section VI.

## II. CIRCUIT DESIGN

The top and side view of the complete test structure is shown in Fig. 1, with the transformer part outlined in red. The top most metal, which is aluminum in this case, is used for making the tertiary coil. Beneath that, are the primary and secondary coils, both made out of thick copper. All the metal coils are on top of each other, giving them maximum coupling. The area of the tertiary coil is approx. 0.6 times the area of the primary and secondary coils, which have the same area. Below the transformer, are the capacitors and transistors, which form the switchable load for the tertiary coil.

Schematic of the whole circuit is shown in Fig. 2. The parts outlined in the red colored rectangle in Fig. 2 correspond to the triple coil transformer and are simulated using Momentum [3], a 2.5D Electro Magnetic (EM) simulator. Resistive, Capacitive and Cross Capacitive (R-C-CC) parasitic extraction is done for the parts of the schematic outlined in the blue colored rectangle.  $L_1$ ,  $L_2$ , and  $L_3$  represent the primary, secondary, and the tertiary coils, respectively.

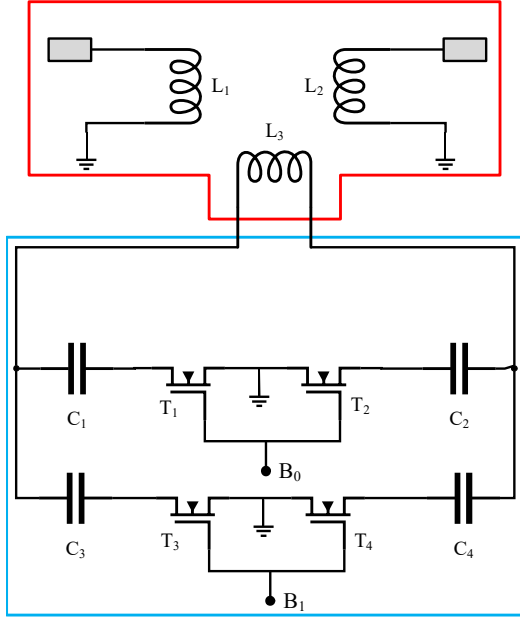


Fig. 2. Schematic of the triple coil variable transformer.

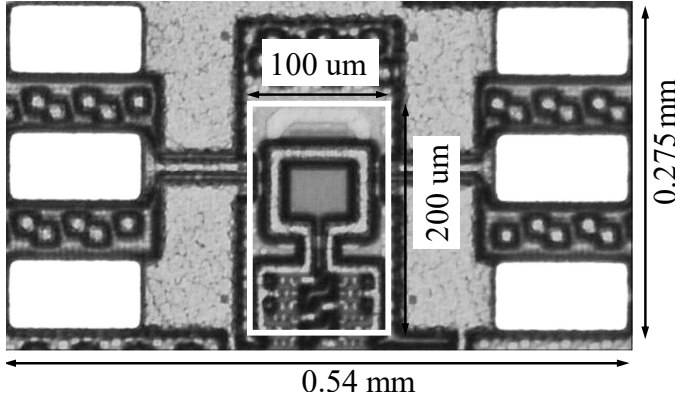


Fig. 3. Chip photograph of the fabricated structure.

A two bit control is implemented using  $T_{1-4}$  to modify the frequency response of the transformer.  $T_1$  and  $T_2$  are controlled together and correspond to bit  $B_0$ . Similarly,  $T_3$  and  $T_4$  are controlled together and correspond to bit  $B_1$ . By turning  $T_{1-4}$  on or off, capacitive loading on  $L_3$  is changed. All transistors are  $100\mu\text{m}$  wide and  $45\text{nm}$  in length. This large width was chosen to keep the ON resistance to a minimum. High density metal-insulator-metal (MIM) capacitors were used for implementing  $C_{1-4}$ .  $C_1$  and  $C_2$  are the same size and have a value of the order of  $200\text{fF}$  and  $C_3$  and  $C_4$  have a value of around  $300\text{fF}$ .

### III. RESULTS

The structure is fabricated using  $45\text{nm}$  CMOS SOI technology and its micrograph is shown in Fig. 3. The dimensions, including the input and output pads, are  $0.54\text{mm} \times 0.275\text{mm}$ . The core area is  $0.02\text{mm}^2$  and is enclosed by a white rectangle in Fig. 3.

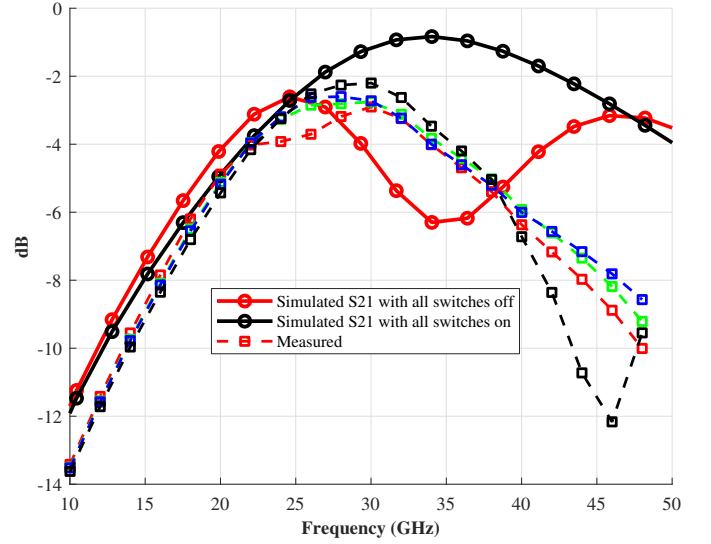


Fig. 4. Simulated vs measured small signal frequency response (S21).

The measurements were performed with Keysight PNA-X N5242A vector network analyzer. Cascade Microtech probe station along with its Infinity series 67 GHz GSG probes were used for probing. The calibration plane was set at the end of the probe tips using the Cascade calibration substrate P/N 101-190.

The simulated and measured small signal frequency response is shown in Fig. 4. The impact of the varying capacitive load can be seen clearly from the simulated results. By changing the capacitive loading, S21 can either show a wide-band response or a simultaneous dual band response. In case of a wide-band response, the center frequency is around  $34\text{GHz}$  with a  $3\text{dB}$  bandwidth of  $26\text{GHz}$ . In case of a dual band response, the two bands appear at  $25\text{GHz}$  and  $46\text{GHz}$ , with an individual bandwidth of around  $14.5\text{GHz}$ .

However, even though the measured results follow a similar trend as the simulated data, the impact of change in loading is marginal compared to the simulated data. Similar discrepancy between the simulated and measured data is seen in S11 too, as shown in Fig. 5. The simulated results clearly depict the impact of changing the loading on the tertiary coil as evident from the one deep notch or two distinct notches in the S11 data, whereas measured results depict almost no change.

### IV. DEBUGGING

For the differences between simulated and measured behavior of S21 and S11, there seem to be two possible culprits, namely

- inability to modify the capacitive load for the tertiary coil,
- unaccounted parasitics.

An NMOS device is used as a switch to modify the capacitive load. A lack of isolation in it will manifest as a static load. As a separate test structure of the NMOS transistors in the switch configuration was available, the debugging was started by studying their measured performance. The test structure

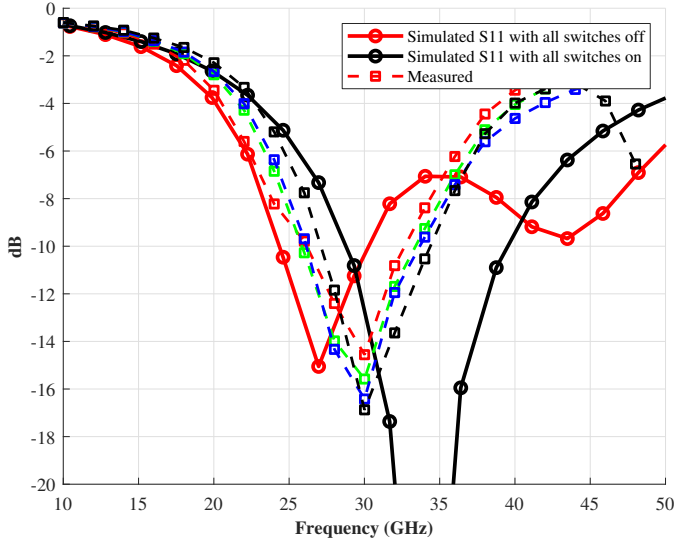


Fig. 5. Simulated vs measured input matching (S11).

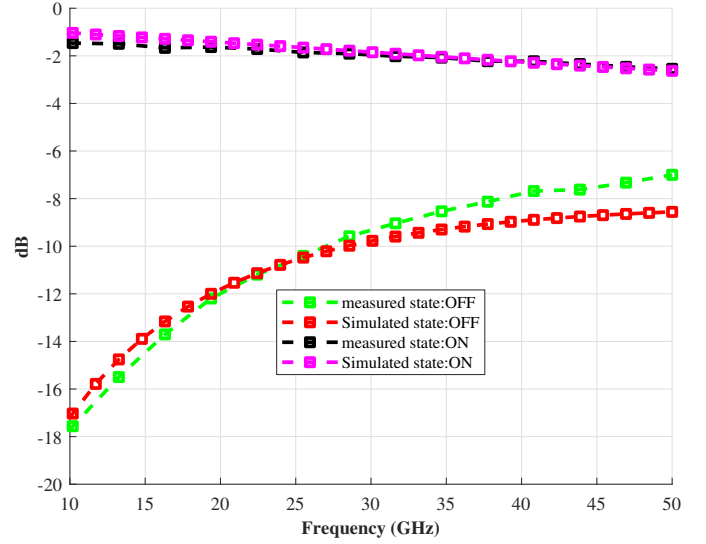


Fig. 7. Simulated vs measured S21 for a 80 $\mu$ m wide NMOS as a function of frequency.

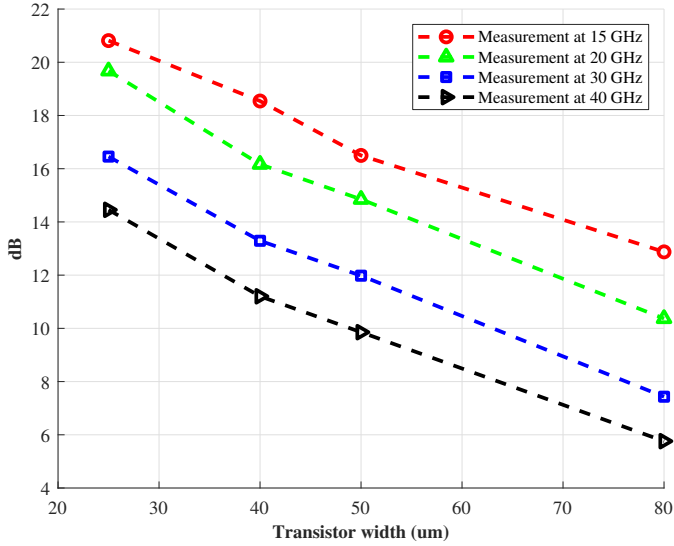


Fig. 6. Measured difference in S21 between ON and OFF state at different frequencies as a function of the transistor width.

included four NMOS devices with their width varying from 25  $\mu$ m to 80  $\mu$ m. Fig. 6 shows the measured difference in the S21 data of the transistor between the ON state and OFF state, as a function of the transistor width. For a 80  $\mu$ m wide device, the difference between the ON state and OFF state is around 8 dB at 30 GHz.

To rule out any modeling or R-C-CC extraction issues with only the transistor, for a 80  $\mu$ m wide device the measured S21 data was compared with the simulated data. As shown in Fig. 7, for the ON state, the measured and simulated data match well. In case of the OFF state, there is a decent match between them till 30 GHz after which they start to diverge, with a difference of around 1 dB at 40 GHz and increasing.

As the NMOS used in the circuit has a width of 100  $\mu$ m, the isolation will be smaller than 8 dB at 30 GHz and will degrade

further as the frequency increases. However, this observation is not enough to match the measured results with the simulated one.

The MIM capacitors, which form the load of the tertiary coil, are around 70  $\mu$ m away from the connecting point of the coil. These 70  $\mu$ m long connections are made using the top aluminum metal. While modeling, these lines were part of the R-C-CC extraction model and not the EM model. As the length of these connections is not negligible compared to the dimensions of the tertiary coil, they were re-simulated as part of the EM model instead of R-C-CC model. This modeling change seems to be the final piece of the puzzle as after taking these two changes into account, the new simulated data matched perfectly with the measured data.

## V. RE-DESIGNING THE CIRCUIT

Coming back to the triple coil variable transformer idea, to operate, it requires a switchable capacitive load. Besides the extra inductance of the length of the connecting routing, the weak point of the design was the use of NMOS transistor in the original configuration. To alleviate this lack of isolation, there exists traveling wave switches [4] and other type of  $\lambda/4$  based switches [5], which can provide isolation in excess of 25 dB at higher frequencies. However, they are too big to implement in this frequency range and have a limited bandwidth. To circumvent these issues, the original capacitive load circuit is modified as shown in Fig. 8. Here, the  $C_1$  is the original capacitive load, however, instead of having the NMOS in series, it is connected in parallel. When the switch is off, its  $c_{ds}$  comes in parallel with  $C_1$  and can be absorbed as part of the total required capacitance. In the ON state, the switch shorts out the capacitive load with a low  $r_{on}$ , thus providing a switchable capacitive load. The bootstrapping resistor  $R_3$  helps with the depth of the notch between the two bands.  $R_1$  and  $R_2$  are for biasing. The transistor is sized based on the tolerable

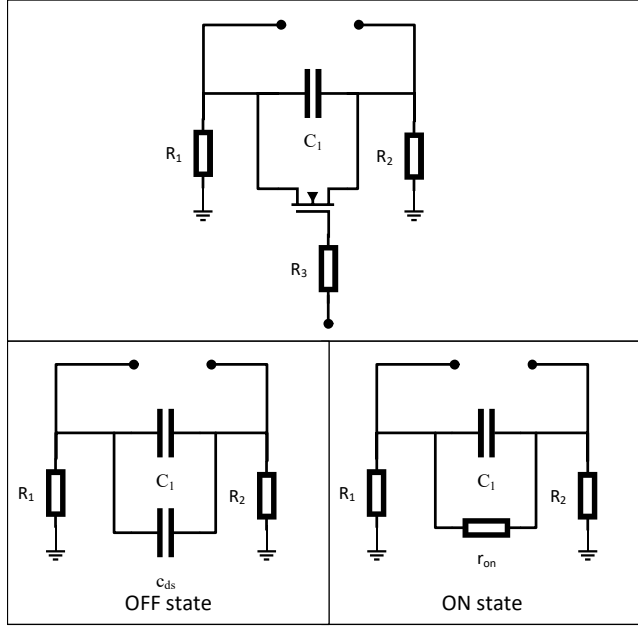


Fig. 8. Modified switching control.

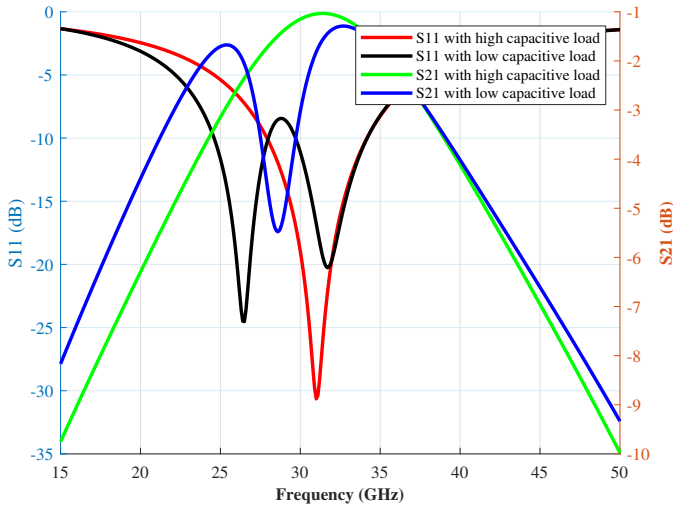


Fig. 9. Simulated data with the modified switching control.

level of  $r_{on}$ . It has to be noted that with this arrangement the control mechanism is different, as the capacitance is either there, or bypassed. This implies that the we can only provide a single bit of control.

After replacing the original switching circuit with this new proposed version, the behavior of the triple coil variable transformer is verified again via the circuit simulations. As seen from Fig. 9, a similar switch from single to dual bands can be achieved with similar losses as in the initial design. Furthermore, here the switch capacitance can be fully absorbed in to the capacitive load.

## VI. CONCLUSION

This work demonstrates a triple coil variable transformer that can provide either a simultaneous dual band or a wide-band response. Though the idea worked in simulations, it was not supported by the measured data. The differences between the measured and simulated results were traced back to a lack of isolation in the switch and unaccounted parasitics. To alleviate the lack of isolation of the switch, a new configuration for the switch was proposed, which could make the original idea of triple coil variable transformer viable. The verification was done using circuit simulations.

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