Optimizing Inductorless Static CML Frequency Dividers up to 23GHz Output Using 45nm CMOS PD-SOI

Mikko Hietanen
Centre for Wireless Communications
University of Oulu
Oulu, Finland
mikko.hietanen@oulu.fi

Janne Aikio
Circuits and Systems
University of Oulu
Oulu Finland
janne.aikio@oulu.fi

Alok Sethi
Centre for Wireless Communications
University of Oulu
Oulu, Finland
alok.sethi@oulu.fi

Rehman Akbar
Centre for Wireless Communications
University of Oulu
Oulu, Finland
rehman.akbar@oulu.fi

Timo Rahkonen
Circuits and Systems
University of Oulu
Oulu, Finland
timo.rahkonen@oulu.fi

Aarno Pärssinen
Centre for Wireless Communications
University of Oulu
Oulu, Finland
aarno.parssinen@oulu.fi

***Abstract*—Two mmWave frequency dividers were designed, manufactured and measured using static current mode logic divider topology on 45nm CMOS PD-SOI technology. Dividers differ by flip-flop load, first divider uses resistive loads and second divider active PMOS loads. Achieved output referred frequency ranges cover 13-22GHz on the first divider and 8-23GHz on the second divider. Both dividers occupy small areas of 0.002mm², and 0.0017mm², respectively and dissipate only 10.3mW and 11mW from 1V supply. The broad tuning range, moderate speed, small area and I/Q output phases make this divider architecture an attractive option for sliding-IF transceiver topologies operating up to 69GHz carrier frequency and enable operation of PLL's up to 46GHz.**

Keywords—CML, CMOS, Static Flip-flop, Frequency Divider, mmWave, SOI

I. Introduction

Growing market demand of broadband and high data rate communication systems are driving circuit design for millimeter wave (mmWave) radios. High losses on mmWave frequencies force designers to use phased arrays and beamforming at system level and utilize inductive peaking techniques at circuit level. Inductive peaking resonates out parasitic capacitances out and saves power at the cost of area. Unfortunately, the utilization of resonator structures make phased array systems not only large, but also induce extra losses in transmission lines between the resonator structures. Even though resonators help to reduce current consumption and enable operating at frequencies closer to f_{max} of the process, inductorless structures are handy in places where there are multiple signals for example mixing stage with input, output and local oscillator ports. For example, in sliding IF topology, dividers can split local oscillator signal as I and Q for the second mixing stage (Fig 1b) [1]. Also, in phase locked loops, a frequency divider is an essential component, which in fact is often the fastest operating circuit in a transceiver design, since it has to cover voltage controlled oscillator frequency range with an ample margin.

Frequency dividers operating in mmWave frequencies can be split into three major categories: static and dynamic logic dividers and injection locked frequency dividers. First type, which is used in this paper, has moderate speed and power dissipation but wide tuning range and very small area. Dynamic logic dividers provide high speed and low power but suffer from narrow bandwidth. Injection locked frequency dividers are much like dynamic dividers but their frequency division is fundamentally different and always occupy large area since they utilize resonators. Static dividers are attractive option for their wideband operation and for their ability to provide differential I/Q phases in outputs. Wideband I/Q generation enables efficient sliding IF topologies because generating I/Q phases with dedicated circuits like polyphase filters require large area and significant power for loss compensating buffers [2]. [3],[4].

This paper presents two static current mode logic (CML) dividers operating at mmWave frequencies. Dividers differ by the load type. First divider (FD1) uses resistive load as a reference to benchmark this technology and second divider (FD2) uses active PMOS load to test wideband tuning capability.

II. Frequency Divider Circuit Design

Schematic of the designed circuits is presented in Fig. 1a. It consists of two differential flip-flops in cascade and feedback configuration. Input signal steers current between differential pair branch (M1, M2 & M5) and latch branch (M3, M4 & M6). Differential pair captures flip-flop inputs during the first half period of the input signal and latch transistors hold the value on the second half period. Having two flip-flops in cascade and clocking them in antiphase results in frequency division by two with I/Q output phases.

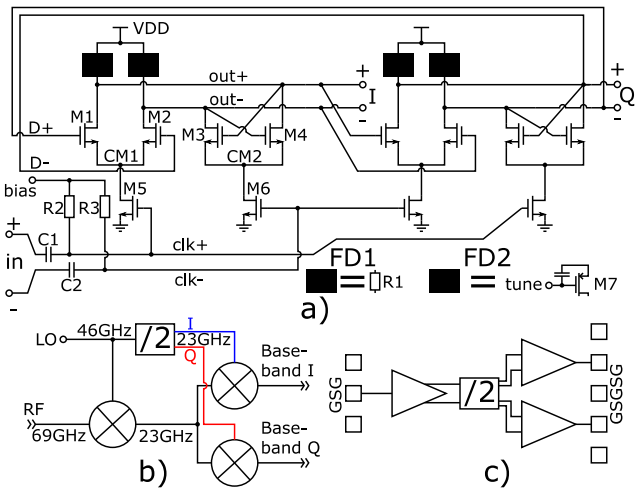

Fig. 1. Static CML frequency divider schematic (a), example of divider in sliding IF system (b) and full block diagram of the divider test structure (c). FD1 uses resistive loads (R1) and FD2 active PMOS loads (M7).

Typically, in mmWave circuits the center frequency is determined by resonators. Here, there are no resonators and the speed is maximized for given process and then controlled down to desired frequency by dimensioning of the components and bias current. Converting resistive load to active load was done by setting the width of the M7 transistors to match the voltage drop of the resistive load. All transistors use minimum length of 40nm and widths are 30µm, 24µm and 26µm for M1/M2, M3/M4 and M5/M6, respectively. M7 in FD2 is 8µm. Resistive loads are 100Ω polysilicon resistors with sufficient width to carry nominal bias current of 4mA with margin. Input capacitors C1 and C2 are 200fF vertical natural capacitors made with all digital routing metal layers except lowest one to reduce signal leakage to substrate. Detailed analysis and design of this topology is presented in many publications such as [3], [4] and [5]. In this paper, we focus mostly on critical aspects of the layout design.

Maximum speed of the dividers is mainly limited by the parasitic capacitances, resistances and the f_T of the transistors. In FD2, speed can be tuned by adjusting M7 gate voltage. Zero volts at the gate provides minimum load impedance and therefore maximum speed. Lower speeds (center frequencies) are achieved with higher gate voltage. To maximize the speed, layout parasitics sensitivity was investigated by simulating self-oscillation frequency (f_{so}) and output amplitude with extra parasitic components in relevant circuit nodes and branches. Results are presented in Fig. 2 and the core layout with these parasitics is illustrated in Fig. 3. Time constant formed by the output node wiring resistance and capacitive components have the biggest impact on the speed of divider. Therefore, it has to be minimized at the cost of other parasitics. For example, M5 and M6 transistors are placed rather far away from M1-M4 transistors to minimize output capacitance, which increases routing lengths of nodes CM1 and CM2, thus increasing their capacitance. However, as it can be seen from Fig 2b, the effect of extra capacitance from CM1 and CM2 wiring is marginal. The wiring of output nodes is also done with higher and thicker metal layer to reduce substrate coupling and wiring resistance.

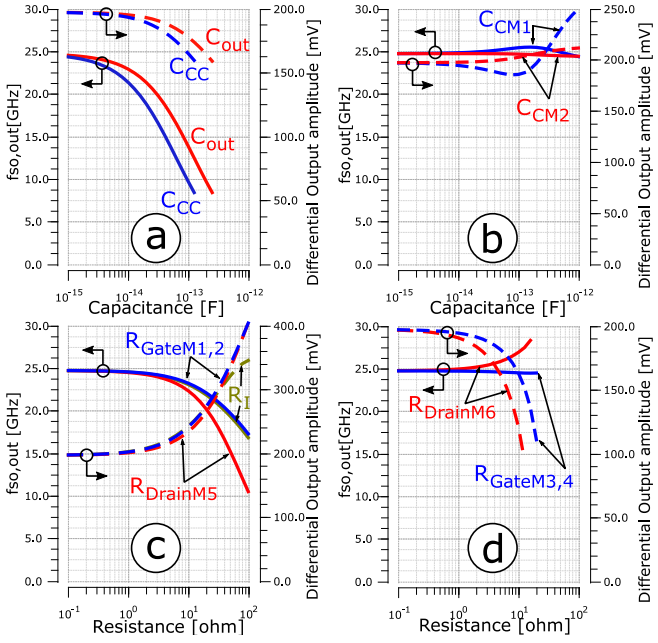

Fig. 2. Divider flip-flop parasitics study sweeps. In a) and b) parasitic capacitances are swept and in c) and d) parasitic resistances are swept. C_{cc} is the capacitance between output nodes.

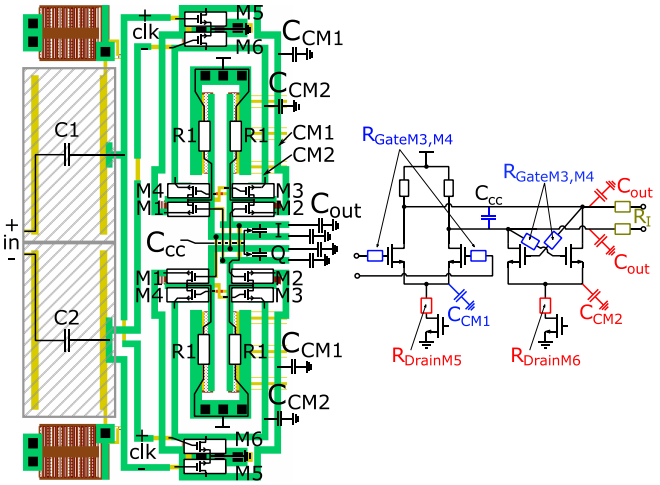

Fig. 3. Divider core (FD1) layout with some parasitic capacitances and circuit nodes illustrated. Brown areas in left corners are additional filtering capacitors for bias.

Fig 2c and Fig 2d indicate that, transistor gate and drain resistances should be kept well below 10Ω, and in most cases below 1Ω range. Excessive drain resistance reduces gain of the differential pair transistors (M1-M2) and limit current driving capability of the latch transistors (M3-M4), which is seen from f_{so} (Fig 2b) and output amplitude behavior (Fig 2c). Resistances are minimized by stacking lower metals in close interconnections of flip-flop transistors while avoiding lowest metal.

Aside from speed optimization, divider outputs are routed to keep phase and amplitude imbalances at minimum by designing symmetrical environments for both I and Q outputs. Final extracted parasitic load of optimized layout is 29.6fF for C_{out} of which 6.6fF is C_{cc}. C_{CM1} and C_{CM2} are 27fF and 24fF. The interconnecting resistance between flip-flops (R_I) is 3.3Ω whereas transistor resistances are $R_{GateM1,2}$= $R_{GateM3,4}$=7.6Ω and $R_{DrainM5}$=$R_{DrainM6}$=3.2Ω. Resistances are comfortably low but output capacitances are on the edges of steep slopes in Fig 2a making any extra capacitance increase detrimental. This emphasizes the need for very careful layout optimization of output node in the design phase.

To measure the divider, a wideband active balun was used to convert single-ended input signal to differential and divider output was buffered with pseudo-differential pair followed by 2-stage common source buffers to drive 50Ω measurement equipment (Fig 1c).

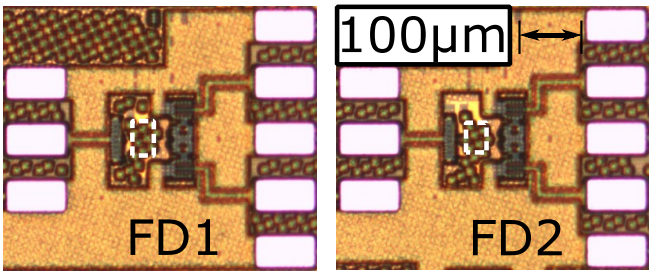

Fig. 4. Micrographs of frequency dividers. Core areas highlighted.

III. MEASUREMENTS

Dividers were measured on-wafer with Cascade Microtech Infinity Probes: 40GHz GSG probe for input and 67GHz GSGSG probe for output. Input signal was generated with Keysight N5242A PNA-X 67GHz vector network analyzer in order to calibrate input power to probe tip. Output signal was measured using Keysight E4446A 44GHz spectrum analyzer with phase noise option. Supply voltage is nominally 1V for this process. Micrographs of both dividers are shown in Fig 4.

Measured bandwidth and input power relation i.e. sensitivity curves for FD1 are presented in Fig. 5. Divider is biased with a 6-bit digital-to-analog converter providing voltages from 160mV to 850mV. Minimum bias for self-oscillation is 490mV. Little higher bias allows slightly faster and more wideband operation. Self-oscillation frequency saturates to 19.36GHz with maximum bias, but the bandwidth is narrow due to heavily saturated M5 and M6 transistors. With all bias values, the achievable bandwidth is 13.2 – 22GHz with 0dBm input signal. We observe only a minor tuning characteristic as a function of biasing.

Sensitivity curves of FD2 are shown in Fig. 6. FD2 required slightly higher bias of 522mV to self-oscillate. Another 6-bit digital-to-analog converter was used to tune gate voltages of load transistors from 0mV to 811mV. The f_{so} is tunable from 20GHz down to 0.2GHz. However, lower frequency is limited by the input coupling capacitors. Hence, the divider could only lock to signals above 7.6GHz. At low frequency values, tail bias has to be boosted for self-oscillation because higher drain-to-source resistance on higher gate voltage of the M7 is limiting bias current flow and gain.

Spurious components in spectrum were observed carefully in measurements to make sure there that interior of the sensitivity curve is spur-free. With FD2, locking to input signal was successful with the same power levels as with FD1, but FD2 required 10dB more input power i.e. >-20dBm to generate spur-free output spectrum. Presence of spurs is difficult to predict with simulations and therefore making a separate test structure of a frequency divider is important before implementing it as part of a larger system.

Phase noise of the dividers were measured at multiple frequencies and tuning values and are shown in Fig 7a and b. Ideally, a noiseless divide-by-2 operation would improve the phase noise by $20 \cdot \log_{10}(2) = 6$dB. The measurements agree with this very well. However, a trend of increasing phase noise degradation with increasing frequency can be observed from Fig 7c.

Different types of state-of-the-art of frequency dividers are compared in Table I. There are not many published CMOS static inductorless frequency dividers reaching mmWave range. FD1 and FD2 use only a fraction of the power while having roughly same the frequency range. Reported dynamic dividers have excellent area, power and bandwidth properties, but no I/Q output possibility. Therefore, they are suitable as PLL prescalers. Narrowband nature of dynamic dividers have been countered with tuning techniques. Static dividers with inductive loads have small power dissipation and when using inductive loads with well-designed inductance and resistance ratio, the bandwidth is actually increased as described in [13]. However, going to higher frequency requires LC-load, which result in narrowband operation. Moreover, design of compact high inductance loads, for example in [10], is much more

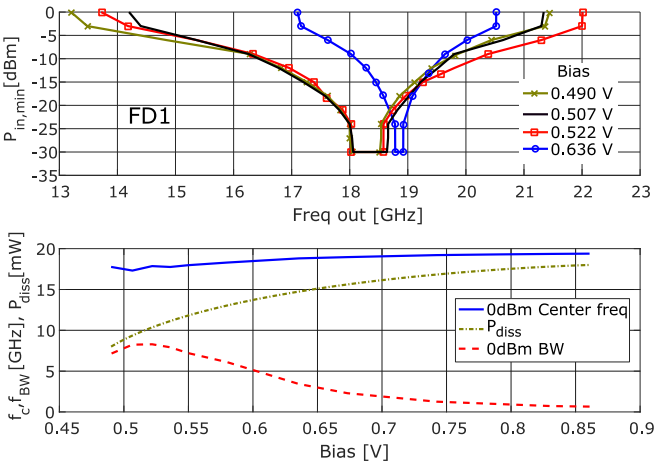

Fig. 5. Frequency divider 1 measured sensitivity curves with multiple biases (top) and bandwidth, center frequency relation and divider core power dissipation (bottom).

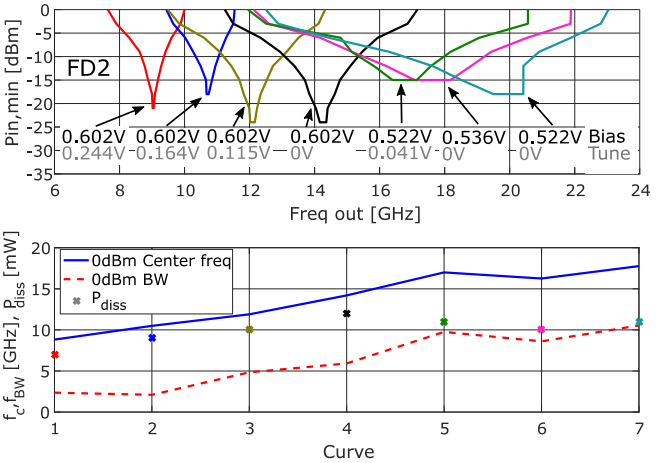

Fig. 6. Frequency divider 2 sensitivity curves (top) and center frequency and bandwidths of each curve (bottom).

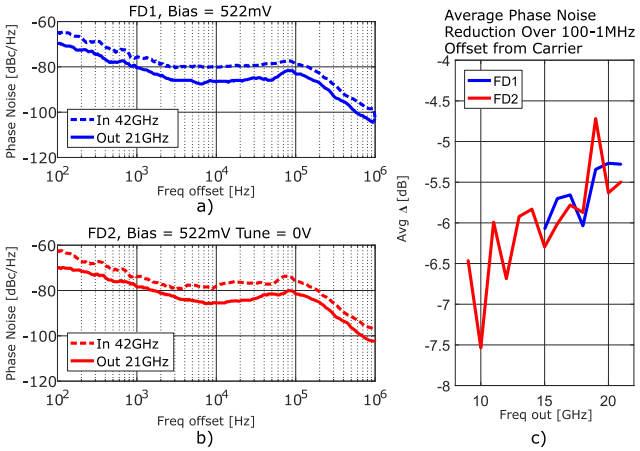

Fig. 7. Phase noise plots of FD1 (a) and FD2 (b) at 21GHz and average phase noise differences over frequency (c).

complex than resistive or active loads due to extensive EM-modeling and layout iteration not to mention potential cross-talk issues. Injection locked frequency divider in [11] uses a transformer to get wide bandwidth. Lastly, a SiGe divider is also included to give more complete view of all reported dividers.

Figure of merit used in the table uses relative bandwidth, division ratio, input power and power dissipation. Because this FoM favours low power and wideband dividers, [10] and [11] stand out in the table. Nevertheless, FD1 and FD2 are

TABLE I. DIVIDER COMPARISON. FREQUENCIES ARE OUTPUT REFERRED.

	FD1*	FD2*	[3]	[6]	[7]	[8]	[4]	[9]	[10]*	[11]	[12]
Type	Static inductorless					Dynamic		Static with inductors		Inj. Lock.	Static SiGe
Load	Amp	Amp	N/A	Amp	Div	Div	Div	Amp	Amp	Amp	Div
DivN	2	2	2	2	2	2	2	2	2	2	2
f_{max} [GHz]	22	23	42.5	27	18	52.5	35	30	22	61.9	26
f_{min} [GHz]	13.2	7.6	16	2	0.4	12.5	6	0.5	1	32.3	1
f_{so} [GHz]	18	0.2-20	32-42	24	11	1-30	13-34	30	15.5	~47	23
LR [%]	51	101	91	172	191	123	141	193	183	63	185
P_{diss} [mW]	10.3	11	35.2	39.7	39.6	5.6	4.8	9.6	3.2	1.2	4
P_{in} [mW]	1	1	1	1	1	1	1	1	1	1	1
Area [mm²]	0.002	0.0017	0.0016	0.02	0.014	<0.001	0.001	0.01	0.0012	0.07	0.018
Process	45nm	45nm	65nm	90nm	55nm	28nm	32nm	45nm	80nm	65nm	120nm SiGe
FoM	9.7	18.3	5.2	8.7	9.7	44	58.9	40.3	114	104.7	82.8

FoM = DivN · LR[%] / (Pin[mW] · Pdiss[mW]), LR = 2 · 100% · ($f_{high} - f_{low}$) / ($f_{high} + f_{low}$) *I/Q outputs implemented

excellent technology node benchmarks showing the effect of downscaling to improve the performance with the same circuit topology. Low frequency bandwidth limitation is irrelevant due to ac-coupled input. With sliding-IF example given in introduction, FD2 suits mmWave bands from 22.8GHz to 69GHz which cover mmWave frequency range of 3GPP/5G New Radio standard (24.25GHz – 52.6GHz) [14].

IV. CONCLUSIONS

Two frequency dividers for mmWave range were designed with focus on layout and speed optimization and implementation of I/Q outputs using static CML topology. FD1 uses simple resistive loads in flip-flops that provides wide bandwidth of 13-22GHz. In FD2, these loads are replaced with PMOS transistors, which enable frequency tuning from DC to 23GHz whilst input capacitors limit minimum frequency to 8GHz in this implementation. Compact areas of 0.002mm² (FD1) and 0.0017mm² (FD2) make these dividers attractive alternatives against dividers using large inductors. High frequency and moderate power consumption of 10.3mW (FD1) and 11mW (FD2) prove good progress in CMOS technology and outperform previous inductorless static dividers.

ACKNOWLEDGMENT

This research has been financially supported by Academy of Finland 6Genesis Flagship (grant 318927) and Nokia Corporation Ltd. Global Foudries is acknowledged for silicon fabrication and technical support.

REFERENCES

[1] M. Chen, K. Wang, D. Zhao, L. Dai, Z. Soe and P. Rogers. "A CMOS Bluetooth radio transceiver using a sliding-IF architecture" in Proceedings of the IEEE 2003 Custom Integrated Circuits Conference, 2003, pp. 455-458.

[2] F. Piri, M. Bassi, N. Lacaita, A. Mazzanti and F. Svelto, "A >40dB IRR, 44% fractional-bandwidth ultra-wideband mm-wave quadrature LO generator for 5G networks in 55nm CMOS" in 2018 IEEE Int. Solid State Circuits Conference, San Francisco, CA.

[3] D. Kim, C. Cho, J. Kim and J. Plouchart, "Wideband mmWave CML static divider in 65nm SOI CMOS technology" in 2008 IEEE Custom Integrated Circuits Conference, San Jose, CA.

[4] A. Ghilioni, A. Mazzanti and F. Svelto, "Analysis and Design of mm-Wave Frequency Dividers Based on Dynamic Latches With Load Modulation" in IEEE Journal of Solid-State Circuits, Vol. 48, Issue 8, pp. 1842-1850, 2013.

[5] U. Singh and M. Green, "Dynamics of High-Frequency CMOS Dividers" in 2002 IEEE International Symposium on Circuits and Systems. Proceedings, Phoenix-Scottsdale, AZ, USA.

[6] J. Chang and S. Liu, "A 4-54GHz Static Frequency Divider with Back-Gate Coupling" in International Symposium on VLSI Design, Automation and Test, 2007, pp. 1-4.

[7] R. Zeng, R. Zhang, C. Shi, Z. Zhang, N. Zhong, "Analytical and Experimental Study of Wide-Range CMOS Static Frequency Divider for 5G mm-Wave Applications" in 2018 14th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Qingdayo, China.

[8] M. Vigilante and P. Reynaert, "A 25-102GHz 2.81-5.64mW Tunable Divide-by-4 in 28nm CMOS" in 2015 IEEE Asian Solid-State Circuits Conference, Xiamen, China.

[9] S. Rehman, A. Ferchichi, M. Khafaji, C. Carta and F. Ellinger, "A 1–60 GHz 9.6 mW 0.18 V Output-Swing Static Clock Divider Circuit in 45-nm SOI CMOS" in 2018 25th IEEE International Conference on Electronics, Circuits and Systems (ICECS)

[10] C. Kromer, G. Büren, G. Sialm, T. Morf, F. Ellinger and H. Jäckel, "A 40-GHz Static Frequency Divider With Quadrature Outputs in 80-nm CMOS" in IEEE Microwave and Wireless Components Letters, vol 16, issue 10, 2006.

[11] J. Zhang, Y. Cheng, C. Zhao, Y. Wu and K. Kang, "Analysis and design of ultra-wideband mm-wave injection-locked frequency dividers using transformer-based high-order resonators" in 2018 IEEE Journal of Solid-State Circuits, pp. 1-13.

[12] H. Knapp, M. Wurzer, J. Böck and T. Meister, "62-GHz 24-mW Static SiGe Frequency Divider" in 2004 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, Atlanta, USA.

[13] S. Mohan, M. Hershenson, S. Boyd and T. Lee, "Bandwidth Extension in CMOS with Optimized On-Chip Inductors" in IEEE Journal of Solid-State Circuits, Vol. 35, Issue 3, March 2000.

[14] 3rd Generation Partnership Project. "3GPP TS 38.104 Base Station (BS) radio transmission and reception (release 15)". April 2019.