An 80 × 25 Pixel CMOS Single-Photon Sensor With Flexible On-Chip Time Gating of 40 Subarrays for Solid-State 3-D Range Imaging

Henna Ruokamo, Lauri W. Hallman, and Juha Kostamovaara, *Senior Member, IEEE*

***Abstract*— A CMOS solid-state 3-D range imager that uses short (∼110 ps) laser pulses and a novel flexible time gating scheme for a single-photon avalanche diode (SPAD) array is presented. The array is divided into 40 subarrays for which a narrow (<0.8 ns) time gating position can be set and scanned independently. The imager can be set to measure multiple regions of interest by means of the flexible time gating of the subarrays. The time gating for each of the subarrays is selected separately with an on-chip delay-locked loop (DLL) block that has 240 outputs and a delay grid of ∼100 ps. The prototype has 80 × 25 pixels overall with 10 × 5 pixel subarrays. The fill factor of the sensor area is 32%. A 3-D range image is demonstrated at ∼10 frames/s with centimeter-level precision in the case of passive targets within a range of ∼4 m and a field of view of 18° × 28°, requiring an average active illumination power of only 0.1 mW.**

***Index Terms*— 3-D imager, single-photon avalanche diode (SPAD), SPAD array, time gating, time-of-flight (TOF).**

I. Introduction

A 3-D range imager is a measurement device that can measure the spatial coordinates (x, y, z) of objects within its field of view (FOV). Thus, contrary to a conventional camera, which measures only the intensity of the radiant excitation of points within a 2-D object surface, a 3-D imager can determine the distance of each point on the surface with a certain spatial resolution. A 3-D range imager is typically realized with a laser scanner that measures distances from objects on one or more horizontal planes, while the measurement beam (or several beams on different horizontal planes) is rotating vertically around the measurement scene. Laser scanners of this kind have traditionally been used in geodesy, civil engineering, architecture, inspection, quality control, and quality assurance, for example. The development of an autonomous or "driverless" car is an attractive example of an application that obviously calls for high-speed environment-sensing techniques [1].

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The authors are with the Circuits and Systems Research Unit, Faculty of Information Technology and Electrical Engineering, University of Oulu, 90014 Oulu, Finland (e-mail: henna.ruokamo@oulu.fi).

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There is, however, a growing interest in applications of 3-D range imaging techniques to areas beyond the traditional ones mentioned above, for example, in robotics and automation, security, "smart homes," gesture control, and collision avoidance systems for unmanned aerial vehicles [2]. These areas can be roughly categorized into long-range (100 m–1 km), midrange (10 m–100 m) and near-range (1 m–10 m) applications. Although the precision and measurement range required to depend greatly on the application, a frame rate (FR) of 10 frames/s (fps) or higher is preferred in most cases. A measurement precision of ∼10 cm is often acceptable in long-range applications, but in some near-range cases such as face recognition, millimeter-level precision is required. In addition, especially in new, emerging applications, a solid-state approach to scanning, i.e., an architecture requiring no mechanically moving parts, is preferred. This kind of realization would simplify the system and pave the way for miniaturization, low-power consumption, low cost, and high reliability.

There are currently several techniques that have been suggested for solid-state 3-D range imaging. Our interest in this paper is mostly in near-range (5 m), medium precision (<5 cm) applications such as gesture control, for which several groups have suggested and studied time-of-flight (TOF) techniques [3]–[8]. These are techniques in which the FOV of the system is illuminated with an intensity-modulated signal in the form of a pulse train or series of short pulses, for example. The receiver then consists of a 2-D array of detectors located at the focal plane of a positive lens. In this system, distance assessment is based on the measurement of the transit time of an optical signal from the transmitter to the target and back to the receiver (TOF). Since each of the 2-D detector array elements points in a distinct direction within the FOV of the system, as determined by its position within the array, a 3-D range image can be produced.

There are basically two approaches for measuring the transit time of the photons. In one of these, a continuous-wave (CW) modulated laser transmitter is used and the per-pixel distance from the target is deduced from the phase of the received signal using some kind of a CMOS active pixel sensor (APS) [6]–[13]. This technology gives a high image pixel resolution (x, y pixel count) but calls for high average power from the optical transmitter (≥100 mW) even for short-range or midrange applications. In the other approach, the phase shift of the CW-modulated signal trans-

mitted and received is detected with a CMOS single-photon avalanche diode (SPAD) array [14], [15]. The phase shift can alternatively be measured from long laser pulses instead of a CW-modulated signal, as in the pulsed indirect TOF (PL-iTOF) technique [5], [16]. Short laser pulses can also be used, in which case a direct transit time measurement is needed instead of a phase measurement [4], [17]–[21]. The approaches based on single-photon detection techniques potentially require a lower average transmitter power due to the inherent high sensitivity of these breakdown-based techniques. On the other hand, the receiver is highly complex, especially in the pulsed TOF method, due to the need for accurate time-to-digital converters (TDCs) for recording the transit times. Background radiation is also an issue, especially in outdoor applications, since random detections due to background light produce noise in the measurements and may even block the receiver under very high-illumination conditions [22].

In the work described here, an attempt was made to address the challenges of single-photon detection-based 3-D range imaging techniques, especially from the point of view of receiver complexity and tolerance of background illumination. The proposed 3-D range imaging architecture uses the pulsed TOF principle, in which short, intensive laser pulses illuminate the FOV of the system (e.g., 40°). In this case, however, contrary to the nanosecond-scale laser pulses which are typically used in long-range LiDAR applications, see, for example [23] and the references therein, sub-nanosecond laser pulses are used. They are produced with a gain-switched laser diode [24]. The receiver electronics consist of a 2-D array of CMOS SPAD detectors, but contrary to the situation in conventional pixel-based time interval measurement systems, the system proposed here adopts a gating approach to distance determination, as used in [25] and [26], for example. In this approach, the SPADs are switched ON for only a short time and this window is then scanned over the measurement range (with respect to the emitted laser pulse). This means that an object at a certain distance produces detections when the time window coincides with the travel time of photons from the transmitter to the target and back to the receiver. The advantage of this method is its resistance to background illumination, since only photons occurring during the time window can trigger the SPAD. Also, since the result is basically 1 bit only (a detection or no detection) the amount of data produced per laser pulse emitted is much lower than in TDC-based measurements, thus allowing for a higher pulsing rate in the transmitter. On the other hand, the measurement rate is relatively low, since only a fraction of the measurement range (the time window) is measured per laser pulse emitted.

In order to speed up the measurements, the receiver used here represents a novel partial scanning approach in which scanning of the time window occurs only around a selected distance, see Fig. 1. The idea is that after the surface of the target has been found [by an initial scan search over the whole measurement range, the "global" region of interest (ROI)], it is enough to scan the time window around that surface distance with a limited scan depth (within the local ROI). Any movement of the surface can be detected from these results and the scan range (depth and position) updated accordingly.

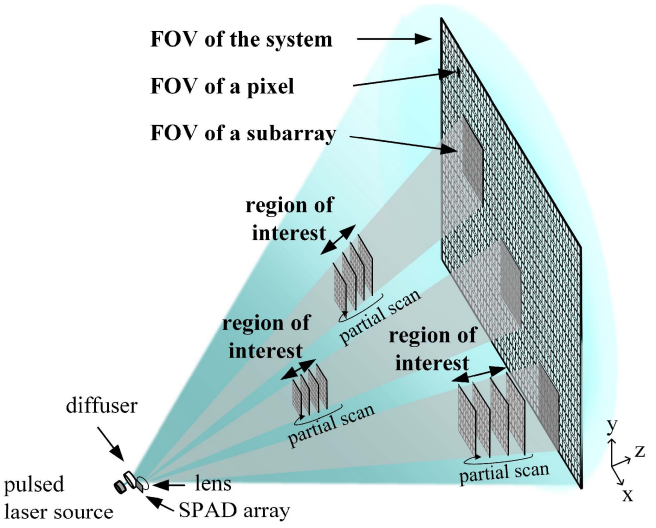

Fig. 1. 3-D range imager system based on a diffused laser pulse transmitter, a 2-D SPAD array, and ROI-based scanning.

This arrangement speeds up the measurement considerably. Moreover, the 2-D detector matrix of the receiver with 80 × 25 pixels is divided into 40 subarrays of 10 × 5 SPAD elements, the scanning depths and positions of which can be set separately and independently of each other. In this way, the receiver can adapt itself to varying target distances within the FOV of the 3-D range imager and the resulting system can produce accurate centimeter-level 3-D range image results with 80 × 25 pixels within a measurement range of several meters with non-cooperative targets at a FR of >10 fps using a transmitter power of only ∼0.1 mW.

The proposed imager topology has been presented briefly in [27], but now its design and characterization will be presented in detail. The operation of the proposed 3-D range imager will be explained in more detail in Section II, the architecture of the sensor chip will be presented in Section III, and the generation of the timing signals in section IV, together with some results characterizing the performance of the device. The pixel electronics will be presented in Section V and the digital signal processing in Section VI. Finally, experimental results for the 3-D range imager will be given in Section VII, a discussion is presented in Section VIII, and the conclusions will be set out in Section IX.

II. Operating Principle of the Imager

The imager prototype uses a pulsed laser diode source as an active illuminator to produce short [∼110-ps full-width at half-maximum (FWHM)], high-energy (>1 nJ) laser pulses with a linewidth of 6.7-nm centered at 864 nm at a pulsing rate of 100 kHz. The scene is illuminated homogeneously by spreading the energy of the laser pulse with a diffuser, see Fig. 1. A SPAD array is used as a detector for the laser pulse echoes. The distances d from the targets are calculated from the TOFs Δt of the received laser pulse photons that trigger the SPADs ($d = c \times \Delta t/2$, where c = speed of light).

The TOFs of the photons are captured by time gating, which is defined here as a period from the activation of the SPADs,

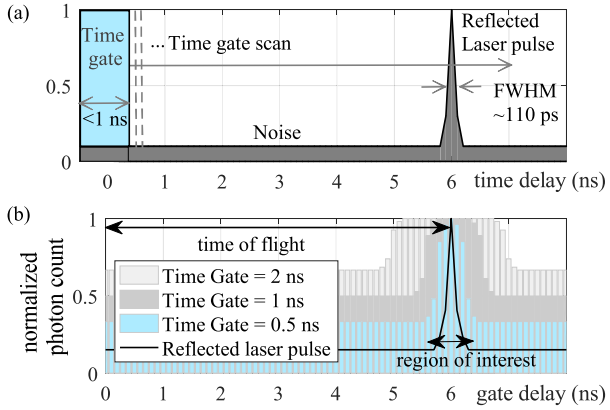

Fig. 2. Histogram creation with shifting of the time gate in 100-ps steps.

ending at the sampling moment when the state of the SPAD is captured. The state is either "1" if the SPAD has detected a photon, or "0" if not. These time gates are delayed in time with respect to the emitted laser pulse (scanning in the z-dimension) to obtain the TOFs of the spread laser pulse. The depth resolution is defined by the time gate width and by the step by which the time gate position is changed with respect to the laser pulses emitted in successive measurements.

In this paper, the time gate is typically short (<1 ns) and can be delayed in ~100-ps steps (see Fig. 2). The time gate scans the scene in the z-dimension and accumulates the detected photons into a histogram, the peak of which provides a basis for calculating the flight time of the laser pulse [see Fig. 2(b)]. The figure shows histograms of the number of photons detected when sampled with ideal time gate widths of 0.5, 1, and 2 ns shifted in 100-ps steps. As can be seen, the width of the time gate should obviously be matched with the laser pulsewidth in order to calculate the delay of the laser pulse precisely and to achieve maximum background suppression.

To increase the FR of the system, the depth scan can be restricted to cover only an ROI, e.g., around the surface of a target as seen by the imager. Moreover, the FOV of the system is split into multiple sub-FOVs by dividing the detector array into 40 subarrays, each of which has its own FOV. The scanning depth and position can then be set separately and independently in each of these subarrays. To achieve 3-D image FRs > 10 Hz for moving targets, the depth scanning can be set to continuously follow the movement of target surfaces. This was implemented in the prototype by starting the partial scan of each subarray one-time gate step before the location of the nearest surface measured in the previous measurement cycle within this particular sub-FOV. In this way, the measurement range for the other pixels within a certain subarray was maximized while retaining a relatively small scanning depth to provide a higher FR. If there were no signal detections in a previous frame in a subarray (no target found or a new target blocks the signal from the previously measured target), the predetermined maximum range is fully scanned to find the distance of a new target that has arrived into the scene.

Although the scanning range position, scanning depth, and step size could be set by software for each of the subarrays,

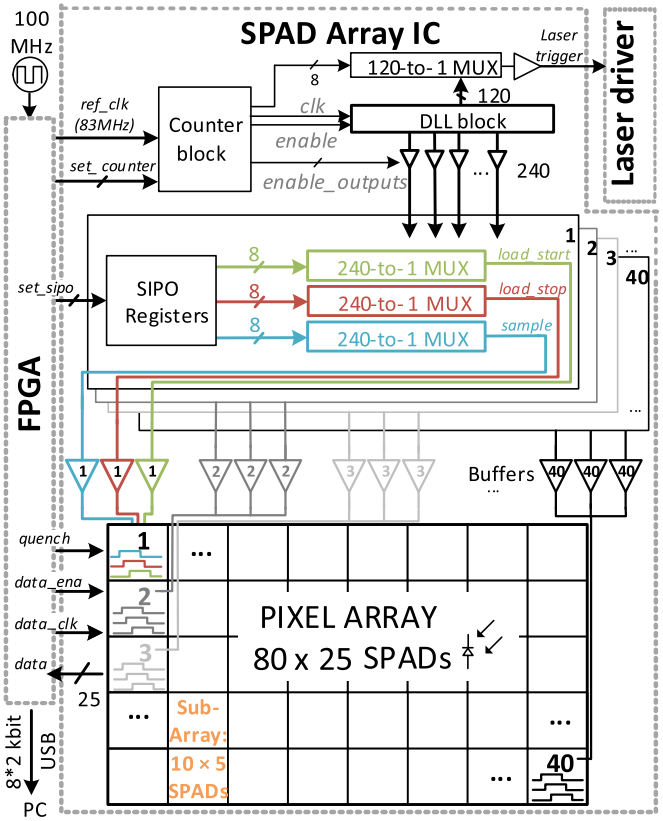

Fig. 3. Block-level representation of the sensor chip.

an algorithm that follows the movement of the surface was implemented in the FPGA of the prototype system. The range settings of the scan in the prototype FPGA were limited to 1.4, 2, 4, or 24 ns (corresponding to 21, 30, 60 cm, and 3.6 m) and the time gate step could be set to either 100 or 200 ps (1.5 or 3 cm). The scanning system for the subarrays described earlier was implemented digitally in the FPGA controller, which enables fast signal processing and 3-D image FRs as high as 100 fps.

The time measurement precision of the 3-D range imager depends on the SPAD timing jitter (typically 50–100 ps), the time gating precision, the laser driver circuitry jitter and the shape of the laser pulse. In the prototype, the laser pulse jitter and the time gating jitter were both ~150 ps, resulting in a total system precision of about ~200 ps.

III. Architecture of the Imager

The imager system consists of an integrated SPAD array circuit, an FPGA control board with a 100-MHz oscillator and circuitry for the pulsed laser source. The receiver part of the imager will be presented here in detail. The core of the receiver is a SPAD array chip that includes 2000 SPADs and a global delay-locked loop (DLL) block that produces the time gating signals for the SPADs (see Fig. 3). The pixel array has been divided into 40 subarrays of 10 × 5 SPADs. The time gating signals of each subarray are selected from the 240 outputs of the global DLL block with 240-to-1 multiplexers (MUXs).

The timing diagram of the flight time measurement is presented in Fig. 4. An on-chip counter block divides an

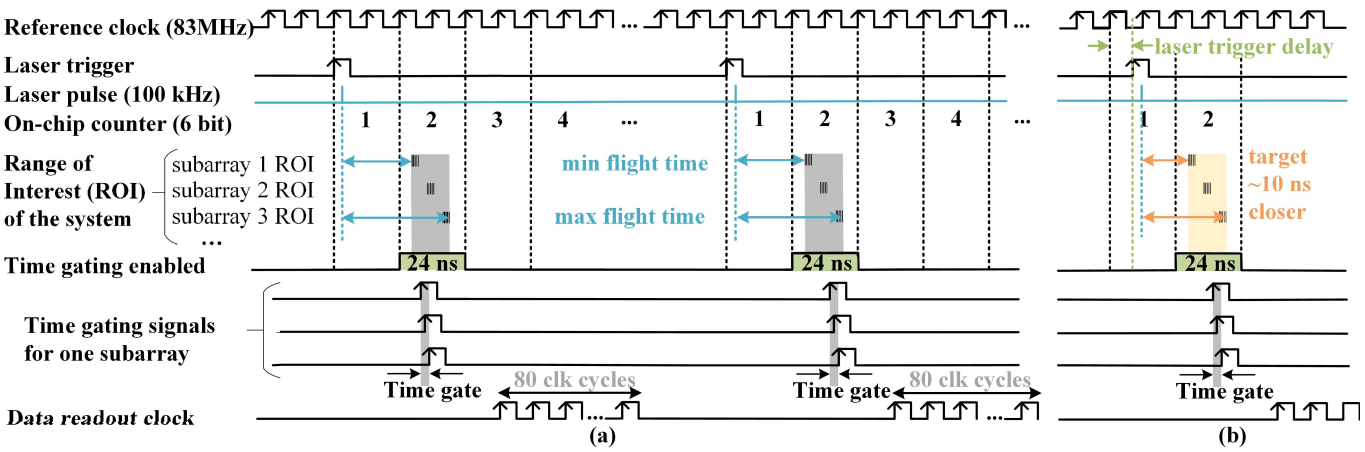

Fig. 4. (a) Timing diagram of the operation of the device. (b) Timing when the laser trigger is delayed to make the range of interest overlap with the DLL period.

83.33-MHz reference clock by two and counts the resulting 24-ns periods from the laser trigger. The time gating can be enabled within any of these 24-ns periods by setting the counter block registers, which enable the DLL block outputs at a specific counter value. For short range applications (<10 m), a 2-bit counter would be enough, but in the imager prototype, a 6-bit counter is implemented to enable measurements for longer ranges in the future systems with higher laser transmitter power. The delay and width of the time gates can be selected for all the subarrays within one 24-ns time window from the DLL block's 240 outputs.

A trigger for the laser is sent from the sensor chip, and an adjustable delay of 0–24 ns is also implemented for this signal in order to allow the "global" ROI (desired range) to overlap with the 24-ns time slot of the DLL [see Fig. 4(b)]. However, if the desired total measurement range is more than 24 ns, multiple measurements are needed since the "global" ROI would then not fit within a single counter value.

A prototype of the sensor IC was fabricated in a cost-effective standard 0.35-μm high-voltage CMOS technology. This approach was chosen since it provides satisfactory SPAD performance for the targeted application in a standard technology [28], and it also provides adequate time precision and resolution for the time gating signals (100 ps), corresponding to the laser pulsewidth (FWHM ~110 ps). A more advanced technology node would provide more design freedom in the digital part of the sensor chip, with increased metal layers, faster speed and a decrease in the area enabling the time gating of individual pixels or a higher fill factor, for example, although using the same time gating for subgroups of pixels reduces the complexity of the system. The detector array size is 80 × 25 pixels in the prototype, but the layout was designed so that an 80 × 50 or even 160 × 50 array could be implemented by copying the design, pipelining the registers and rearranging the power supply pins. A microscope picture of the chip and one subarray of pixels are presented in Fig. 5.

In the prototype, the state of the SPAD array at the trailing edge of the time gate is sampled and all 2000 bits are read out from the sensor IC to the FPGA by connecting in-pixel registers in series of 80 bits. With a 100-MHz readout clock

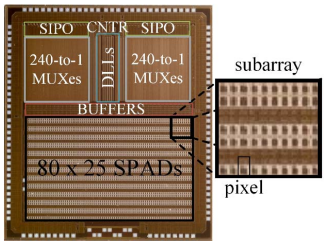

Fig. 5. Picture of the chip and placement of the main blocks.

and 3 cycles reserved for data acquisition, an FR of up to 1.2 MHz can be achieved for these 2 kbits of data. However, since the 2-D binary image FR is limited in the prototype by the laser pulsing frequency (100 kHz), a reference clock frequency of 83.33 MHz can also be used for readout purposes. All the signal processing is done by the FPGA, which is beneficial for imager system prototyping and also enables the necessary digital design to take advantage of the most advanced process nodes. The FPGA controls the time gating by selecting time gating signals from the DLL outputs by setting the serial-in parallel-out (SIPO) registers that control the 240-to-1 MUXs. The counter block that enables the DLL outputs at a set time delay from the triggering of the laser pulse is also controlled by the FPGA, which provides the DLL reference clock and readout clock.

The power consumption of the SPAD array IC is accounted for mainly by the DLL block, the drivers for the time gating signals and the data readout. The DLL clock in the prototype is gated and enabled 1 μs before enabling the time gating, resulting in an average current consumption of 5 mA from a 3.3-V power supply for the DLL block and other time gating circuitry if both DLLs of the DLL block are on, and 3 mA if only one DLL is on. The average power consumption of setting up the SIPO registers is negligible since these have to be written only when the time gate positions change. The average current consumption of the readout circuitry in the prototype is 15 mA from a 3.3-V power supply, resulting in a total measured current consumption of 18 or 20 mA depending on whether one or two DLLs are activated. The average current consumption from the high-voltage supply is

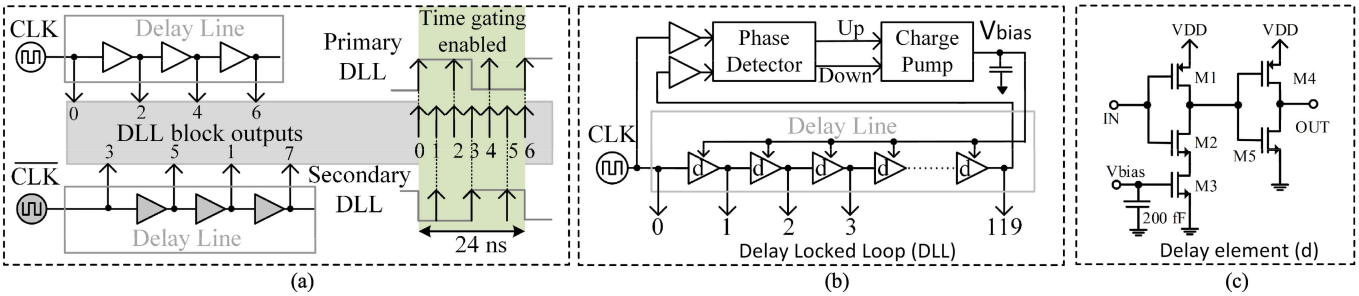

Fig. 6. (a) Principle of mapping the primary and secondary delay line outputs to DLL block outputs, shown with three elements in the delay line (119 delay elements in one DLL in the prototype). (b) Block diagram of one DLL. (c) Schematic of a delay element that has been implemented on the prototype chip.

small since SPADs are loaded only once for each measurement cycle (post layout simulations show 70-μA average current consumption for loading all the SPADs at a pulsing rate of 100 kHz).

IV. Generation of the Time Gating Signals

A. Delay-Locked Loop

The DLL block consists of two separate DLLs: a primary DLL, which is used to generate the time gating signals and to set a delay to trigger the laser source. The primary DLL has 120 outputs in a timing grid of ~200 ps when locked to the 24 ns reference clock, and the secondary DLL can be turned on to increase the timing resolution of the time gating signals to ~100 ps. The delay lines are driven by orthogonal clock phases derived from the outputs of dividers (by 2), ensuring an accurate duty cycle of 50%. Since both delay lines consist of an odd number of elements, it is possible to generate a delay grid of ~100 ps; for the grid generation principle, see Fig. 6.

One DLL consists of a phase detector, a charge pump and a voltage-controlled delay line that has 119 delay elements, see Fig. 6(b). A current-starved buffer is used as a delay element to produce a nominal 202-ps delay when the delay line is locked from the ends to the 24-ns period (24 ns / 119 = 202 ps), see Fig. 6. Since the delay line is locked to the reference clock, the delay grid is tolerant of process variations and power supply voltage and temperature changes.

B. Linearity of the Time Gating Signals

The linearity of the time gating signals depends on that of the delay lines of the DLL block and on the MUX chains. First, the linearity of shifting the scanning range (24 ns) to overlap the ROI was measured. This shift is achieved by delaying the laser trigger and selecting the appropriate counter value to match the min and max flight times of the "global" ROI to the time gate scan, as in Fig. 4(b). The linearity of this shifting was assessed by measuring the delay from the laser trigger to the leading edge of the first possible rise time of the time gate (min flight time) at counter values of 1–4 using the time interval measurement property of a high-speed real-time oscilloscope, see Fig. 7.

If the laser triggering is not delayed and the counter value is set to 4, the laser triggering appears ~76 ns before the first possible time gate signal. In the linearity measurement, the laser triggering was delayed from this position with all

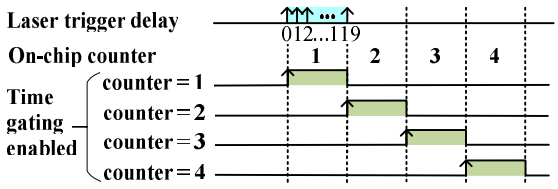

Fig. 7. Signals for measuring delay and linearity in the laser trigger delay as compared with the first possible time gate signal with counter values 1–4.

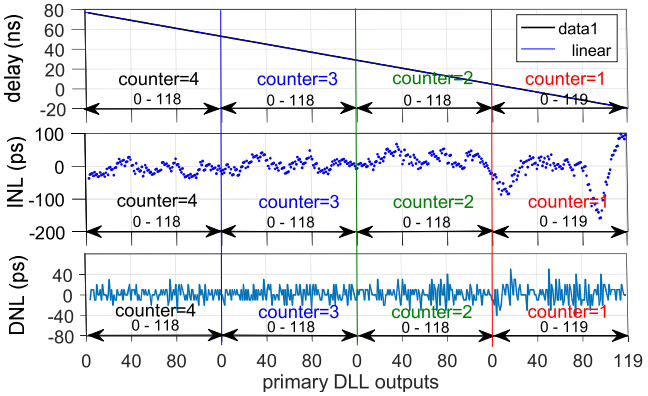

Fig. 8. Delay and linearity of the leading edge of the laser trigger signal compared with the leading edge of the time gate at counter values 1–4, measured by delaying the laser triggering signal.

the 119 primary DLL delay settings, resulting in the laser trigger approaching the time gate position both when the laser trigger was delayed and when the counter value was reduced (total range 4 × 24 ns, i.e., −20–76 ns). The linearity of the delay grid is calculated by fitting a linear line to the delay measurements and taking the difference between the fit curve and the measured one.

The measurement result shows a non-linearity of <70 ps for the laser trigger signal delay at counter values of 2–4, see Fig. 8. This linearity is assumed to continue in a similar manner with larger counter values, since the linearity depends on the delay line and the MUX chain and not on the counter. When the counter is set to 1, the time gate position can be set to small delay values or even before the laser triggering signal (i.e., −20–4 ns), see Fig. 8. When the counter is set to 1, the buffering for the time gating is also enabled at the same time, as seen in Fig. 7, which affects the linearity of the laser triggering signal due to the effects of parasitics in the power supply line on the delay line behavior when enabling the DLL outputs for time gating.

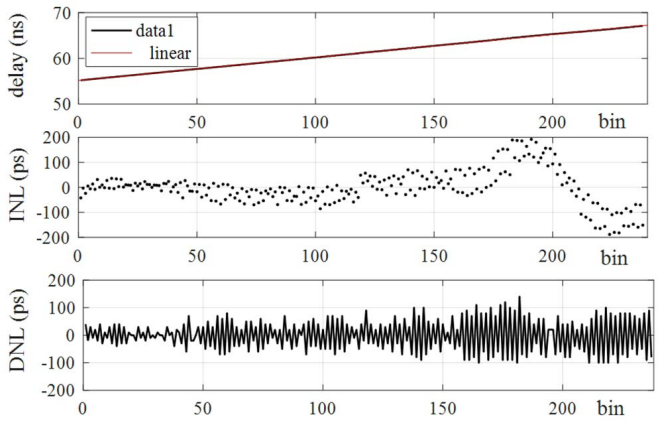

Fig. 9. Delay and linearity of the time gate scan upon delaying the time gate signal by setting the delay from DLL block at 240 outputs (counter = 3).

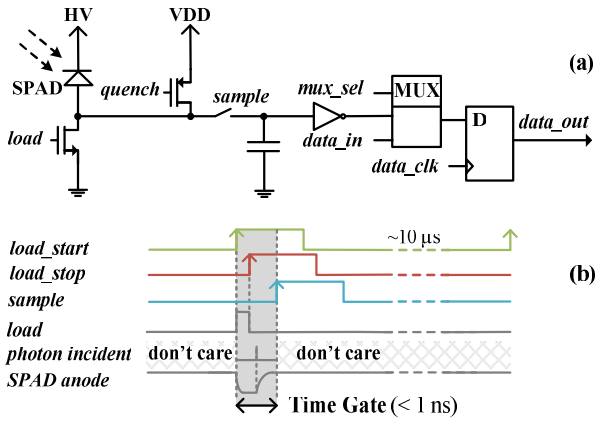

Fig. 10. (a) Simplified schematic of the pixel electronics. (b) Timing diagram of the pixel electronics.

The time gating for measuring the flight time of the laser pulse is nevertheless needed only after the laser pulse has been triggered (delay $>$ 0), in which region the measured integral non-linearity (INL) is less than 100 ps. The differential non-linearity (DNL) at counter values of 1–4 is less than 50 ps, see Fig. 8.

The linearity of the actual time gate scan, which can differ from one subarray to another, is measured by turning on both DLLs and setting the rising edge of the laser trigger as the reference signal (start). The delay for the laser trigger was set to 2 ns, and the time position of the leading edge of the time gate was measured at different settings. A delay of 50–74 ns was measured with a counter setting of 3, and the measured INL is less than $\pm$100 ps from bin 0 to bin 187 and increases to $\pm$200 ps after that (see Fig. 9). The increase in the non-linearity rises in the latter part of the delay line due to the parasitic inductance in the power supply line and can be reduced by decreasing the parasitics or the number of simultaneous digital events. In principle, it is also possible to correct the non-linearity by calibration. The corresponding DNL of the time gate scan is presented in Fig. 9.

V. Pixel Design

Each pixel includes one SPAD, switches for biasing the SPAD, a sampling switch and a 1-bit data storage element, see Fig. 10. The cathode of the SPAD is initially connected to a high voltage (HV $\sim$ 22 V) and when the operation starts, the SPAD is first quenched by connecting its anode to 3.3 V with the *quench* signal, bringing the SPAD voltage slightly below the breakdown voltage V_{br}. The diode is then biased with an excess bias voltage V_{ex} above V_{br} by connecting its anode to the ground with the *load* signal. When the voltage across the SPAD exceeds the breakdown voltage, the SPAD is activated and is ready to detect photons. The anode is loaded to the ground for only a short period of time ($\sim$200 ps), after which the anode voltage rises as a photon reaches the active area of the SPAD and a breakdown event occurs. Load is constructed from two rising edges locally at every pixel, to make a short electrical pulse possible even when trace lengths are over 2.5 mm, as in this prototype circuit. The time gate is defined to begin at the rising edge of the load signal and to end when the SPAD state is sampled by opening the sampling switch at the rising edge of the *sample* signal. The SPAD is activated once for every laser pulse (100 kHz), thus the effect of afterpulsing is negligible.

The active area of the SPAD is between p+ diffusion and the deep n-well and it is surrounded by the p-well guard rings, as in [29]. The size of one pixel is 50 μm $\times$ 100 μm, of which the active area of the diode is 36 μm $\times$ 44 μm. This results in an average fill factor of $\sim$32% for the sensor part of the chip.

VI. Digital Signal Processing

In the prototype, the state of the SPADs at the end of each time gate is transferred directly from the sensor IC to the FPGA due to the flexibility of the digital design when an FPGA is included and the possibility for using advanced process nodes (28 nm) for the digital part. The FPGA produces a 2-D distance array from the target, the distance is calculated by creating a histogram from the photons detected for each pixel and calculating the TOF by first filtering the histogram and then finding the maximum intensity.

The data rate from the FPGA to the PC was minimized by sending only the peaks of filtered TOF histograms to the PC. Thus, the amount of data to be sent in the prototype is 8 bits per histogram of 240 bins, leading to a total amount of data equivalent to the number of pixels (2000) multiplied by 8 bits for every depth range of $\sim$3.5 m, an amount that can easily be sent through a USB connection. Therefore, when the signal processing is done in the FPGA, the data rates on the route from the FPGA to the PC are small (16 kbits/frame) and real-time operation can be achieved.

The data rate from the PC to the FPGA was minimized by implementing an algorithm in the FPGA which sets the scanning range at the surface of the nearest target. Similarly, the scanning depth, position, and step size could also be controlled by software. To set three time gating parameters each of 8 bits, the data rate from the PC to the FPGA would have to be 24 bits per subarray for every frame (96 kbits/s for an FR of 100 fps in the prototype).

VII. Experimental Results

A. Time Gate Uniformity

The actual, effective width of the time gate (SPAD active time) across the array was measured with time gate width

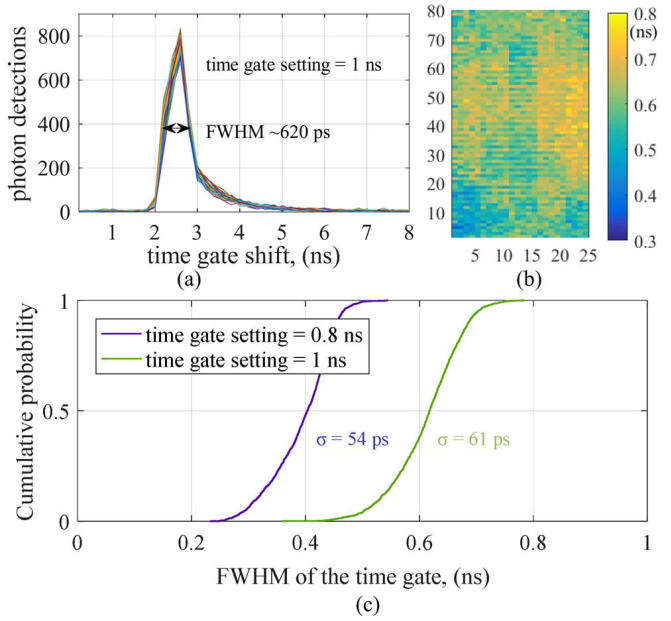

Fig. 11. (a) Photon detections of a sub-array of 50 SPADs in the middle of the array when time gate (1 ns) is shifted in 200-ps steps. (b) FWHM (nanoseconds) across the pixel array when time gate is set to 1 ns. (c) Cumulative probability of the FWHM of the SPAD active time for the 2000 pixels.

settings of 0.8 and 1 ns. The measurement was made by placing a piece of white paper 1.25 m away from the imager as a target and detecting photons from multiple laser pulses. The laser pulses were the same as used in the normal operation of the imager prototype (FWHM ∼110 ps, energy ∼1 nJ, wavelength 864 nm and pulsing rate of 100 kHz). Histograms of the reflected signals for all the pixels were accumulated while shifting the time gate position in 200 ps steps, and the FWHMs were calculated from the histograms, see Fig. 11(a) and (b). The measurements of the detected photons with two time gate settings for the whole array show a median FWHM of 400 ps for the time gate setting of 800 and 620 ps for 1 ns, see Fig. 11(c). The nominal time gate values were ∼400 ps larger than the FWHM values, mainly due to the slow rising and falling edges of the time gates. The spatial uniformity of the time gate widths in the array when the time gates are set to 1 ns can be seen in Fig. 11(b). The figure shows that the actual time gate widths are smaller at the corners and that the subarrays in the middle of the x-axis have somewhat smaller time gates. The main reason for the different time gating widths in the array is routing skews.

B. SPAD Array Noise

A median dark count rate (DCR) of 200 kHz was measured for the SPAD array at room temperature, see Fig. 12. However, when the FOV is 18° × 28°, for example, the ambient lighting usually dominates the noise, as in the sample measurement result also shown in Fig. 12, which was measured under background illumination conditions of 200 lux measured in front of the detector. The uniformity of the DCR of the pixel array can be seen in Fig. 13. The median measured DCRs and a decrease in photon detection effectivity (PDE) when the cathode voltage is reduced are shown in Fig. 13. Photon

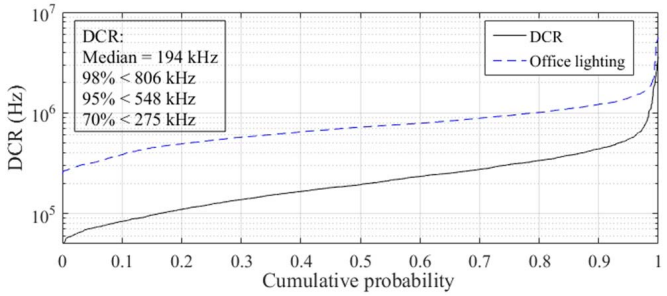

Fig. 12. Cumulative probability of the DCR and an example of random photon counts in 200-lux office lighting with a cathode voltage of HV = 22 V with a white paper as a target.

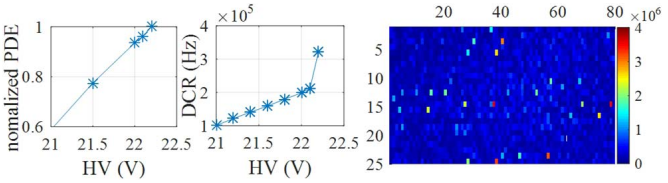

Fig. 13. Normalized PDE and median DCR at different cathode voltages (HV), and DCR (Hz) of the pixel array (HV = 22 V) at room temperature.

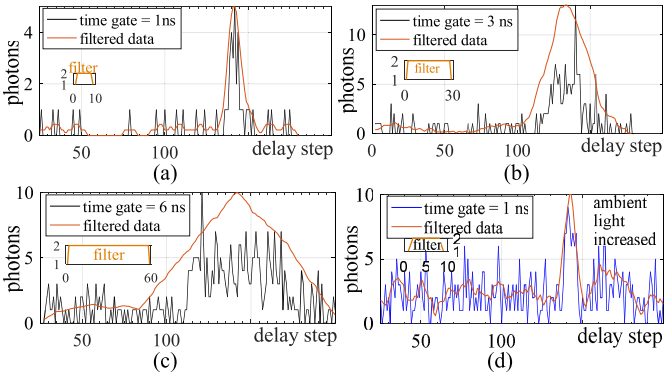

Fig. 14. Example measurement results of histograms of detected photons when time gate width is set to (a) 1 ns, (b) 3 ns, and (c) 6 ns at ∼200 lux and (d) time gate set to 1 ns at ∼600 lux.

detection probability is ∼4% at 810 nm with an excess bias voltage of 3.3 V. The 3-D measurements for this paper were performed with a cathode voltage of 22.1 V, since the DCR and the number of "hot" pixels increase considerably at higher voltages, presumably due to the lower breakdown voltages of those pixels.

C. Sensitivity to Ambient Lighting

By reducing the time gate width of the SPAD, the amount of ambient light that may trigger the SPAD can also be lowered, see Fig. 14. The figure contains example histograms of photon detections for one pixel measured with time gate widths of 1, 3, and 6 ns. The x-axis shows the shift of the center of the time gate in 100-ps steps when the scanning range is started ∼14 ns before the arrival of the reflected laser pulse photons at the target detector. In this measurement, the target was a piece of white paper at a distance of 3.5 m, and 160 laser pulses were sent for each time gate position under normal office lighting (<600 lux, produced by additional illumination with a halogen lamp). An example of the filtering

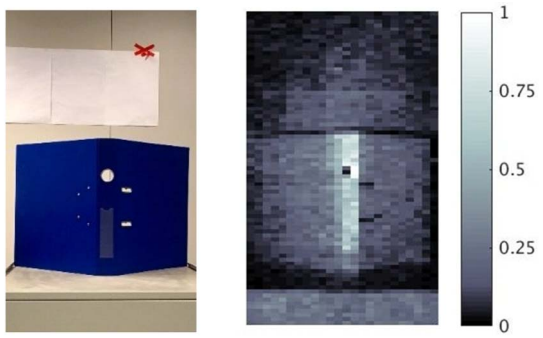

Fig. 15. (a) Picture of the scene. (b) Intensity image (normalized photon detection rates in the pixels).

of histograms with a weighted moving average is also shown in the figures. As can be seen, the effect of noise is minimized by shrinking the time gate. An optical 50-nm bandpass filter with a center wavelength of 875 nm was used in all the measurements in front of the detector lens to suppress ambient light.

D. 3-D Measurement

The 3-D measurements were made with a system FOV of 18° × 28°, aiming at near-range (<5 m) indoor applications. To demonstrate the functionality of the system, a folder was placed on top of a drawer, and the 3-D range images were measured. Figs. 15 and 16, respectively, show a photograph of the target scene and a set of measurements for 80 × 25 pixels. Point cloud representations of the measurements are shown in Fig. 16(b) and (c), in which the range is measured by means of a full scan and a partial scan, respectively. In these representations, the raw data from the imager have been converted from spherical to Cartesian coordinates in order to show the distance result on the x-, y-, and z-axes.

By restricting the scanning ranges to small regions near the results of the previous frame by taking advantage of the independent time gate control in the subarrays, the FR can be increased considerably. In this example, the FR is 13× higher when scanning the range partially with 40 subarrays instead of a full scan of the range, see Fig. 16(b) and (c). The partial scanning in the subarrays was set to cover a range of 21 cm starting from the nearest surface of the target. Limiting the range to 21 cm within one sub-FOV can be seen from the lack of blue distance results from the back wall in those subarrays in Fig. 16(c) which have detected photons reflected from the side of the folder as compared with the full scan result in Fig. 16(b). Scanning of both the back wall and also the folder within a single sub-FOV could in principle be implemented by setting two partial scan ranges: one at the surface of the drawer and the other at the surface of the back wall.

The angular shape of the folder and the detection of a few pixels on the upper surface of the drawer can be seen better in the point cloud representations of the distance results with various measurement settings shown in bird's-eye view (*XZ* view) in Fig. 17. The measurements were made under office lighting conditions and the measured background light at the surface of the target was ∼200 lux. The effect of the time gate width on the precision can be seen from Fig. 17(a) and (b), where the precision of the result decreases from ∼2 to ∼5 cm when the time gate width is increased from 800 ps to 2 ns. Fig. 17(c) shows the *XZ* view of the result when scanning is performed with 100-ps time delay steps. This setup gives better resolution but halves the FR from 0.7 to 0.35 fps.

The FPGA comprises a partial scanning algorithm that not only sets the scanning range at around the nearest surface in each subarray FOV but is also able to follow the movement of the surface in depth. To demonstrate the functionality of the algorithm, the scanning depth was set to 7 delay steps (each of 200 ps) and the distances from the same targets as above were measured. The results after the target had been found are shown in Fig. 17(d)–(f). The target scene was measured with 1600, 320, and 160 laser shots per each time gate position in Fig. 17(d)–(f), respectively. A precision of $\sigma \leq 2.1$ cm was measured ($\sigma \leq 1.6$ cm from the drawer and $\sigma \leq 2.1$ cm at the back wall and from the folder), with the setup as in Fig. 17(d) in which 1600 laser pulses were sent in each delay step, and 9 fps were achieved with this setup. The FR could be increased to 90 fps by reducing the number of laser pulses emitted to 160, but the lower averaging factor reduces the signal-to-noise ratio, resulting in lower precision. The time gate width was set to 800 ps in these measurements.

VIII. Discussion

The main contribution of this paper is the proposal for using adaptive time gating for single-photon detection-based pulsed TOF distance measurement. The setting of the ROI (scanning range) is based on the prior knowledge of the position of the target, the movement (position and speed) of which must be continuously followed, and the scanning range is adaptively modified accordingly. In order to allow for different target positions in different parts of the system FOV, the FOV may be divided into subfields within which independent regions of interest can be designated. Ultimately, a pixel-based setting of the scanning range would be desirable, of course, but unfortunately, this can only be achieved at the cost of increased chip complexity. On the other hand, in many cases, the surface of the target is "smooth," and thus a lower spatial resolution in the definition of sub-FOVs is possible.

A fair comparison of state-of-the-art 3-D imager systems is difficult, since they all have different parameters, e.g., FOV, pixel count, and illumination power, and they are usually targeted for specific applications. On the other hand, the system level performance depends greatly on these parameters. Also, the FR depends on the required precision and the signal-to-noise ratio (which is related to the illumination power per pixel, signal reflection from the target, distance of the target, and ambient lighting).

The distinct difference between this paper and other types of recently described solid-state imagers using illumination wavelengths of ∼800–900 nm, as listed in Table I, is this device's markedly lower illumination power and power consumption of the receiver electronics.

On the other hand, the performance of the present system has a substantial potential for further improvement, e.g., longer

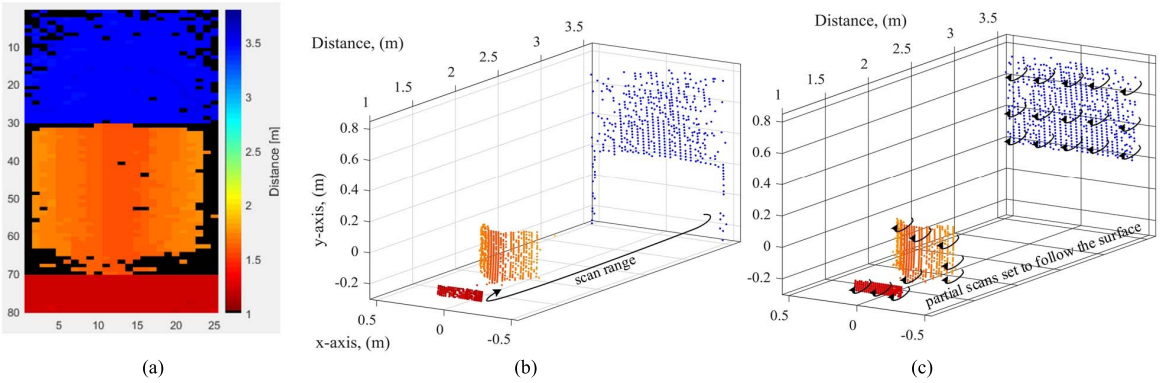

Fig. 16. (a) Raw color-coded distance result of the pixels, and point cloud representation of the measurements as (b) a full scan and (c) a partial scan the range using independent time gating of the 40 subarrays. The FR increases from 0.7 to 9 fps from the full to the partial scanning.

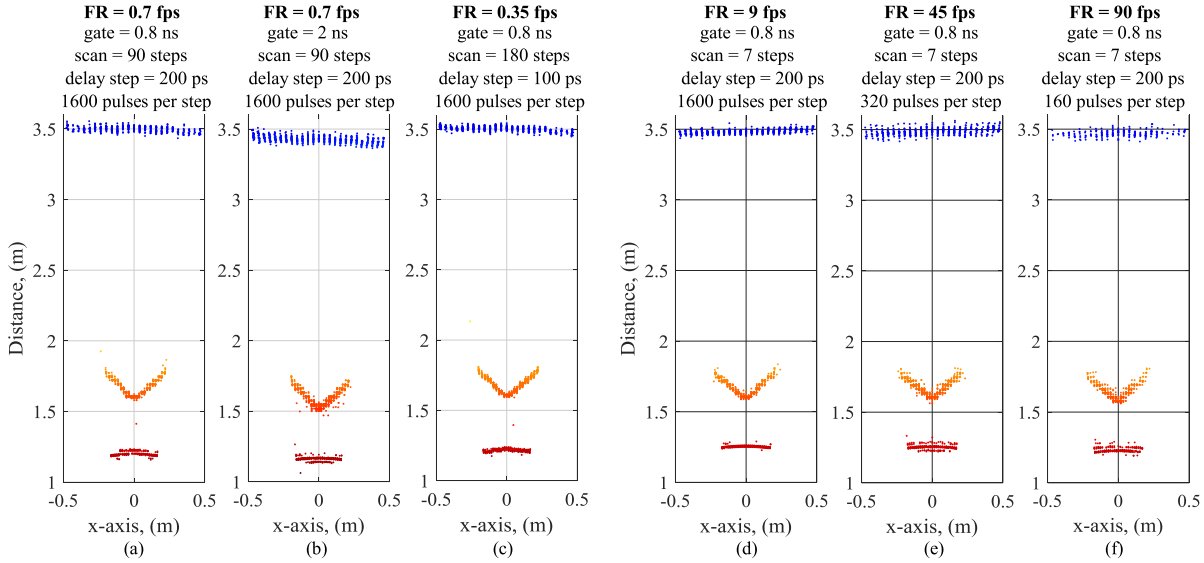

Fig. 17. *XZ* view of the measurements as (a)–(c) full scans and (d)–(f) partial scans of 7 steps (21 cm) grouped around the surface of the nearest target in the FOV of each subarray.

TABLE I
RECENTLY PUBLISHED SOLID-STATE 3-D IMAGER SYSTEMS

Ref	[12]	[16]	[19]	This work
CMOS Tech. (µm)	0.065 BSI	0.35 HV [e]	0.35	0.35 HV
# Pixels	1024 x 1024	32 x 32	32 x 32	80 x 25
FF (%)	~100 [b]	3 [e]	3	32
Power (mW)	650	-	-	66 [a]
Illum. P (mW)	300	188 [c]	90	0.1
FOV (HxV) (deg)	120 x 120	40 x 40	6.9 x 6.9	18 x 28
Acc/prec (cm,σ)	0.2%@4.2 m	6%/~20cm	- / ~cm	3 / 2 cm
Frame Rate (fps)	30	10	6[d]	9
Measured Range at Ambient Light	4.2 m 3 klux	21 m not stated	8 m < 50 lux	3.5 m 200 lux
TOF Technique	CW	PL-iTOF	dTOF	Gate scan

[a]power consumption of the sensor IC, [b]with microlens, [c]peak power of 750 mW·0.25 (duty cycle) , [d]250 mm optics (f/4.8), [e][30].

range, higher ambient light tolerance, or measurement speed by scaling up the pulse energy (to ∼5 nJ with sub-ns pulses, longer laser pulses with higher energy may in principle be used as well) and the pulsing rate (∼1 MHz). Since the transmitter optics use a diffuser, the transmitter power can be scaled up relatively easily using stacked laser diode structures, for example, without affecting the quality of the illumination beam. In addition, since the amount of data measured per emitted laser pulse is relatively low, the transmitter pulsing rate can be increased while keeping the data transfer volume reasonable. Finally, microlens techniques could be used to improve the effective fill factor of the detector array.

IX. CONCLUSION

An 80 × 25 pixel solid-state 3-D imager using independent flexible time gating and spatial grouping of pixels of a 2-D receiver array has been presented here. The prototype uses short laser pulses (FWHM∼110 ps) and determines the TOF of the pulse by scanning the scene in the depth direction using short time gates (<1 ns). A possibility for optimizing the FR of the target scene distance measurement by dividing the detector array into subarrays with time gating that can be set independently around the surface of the target (range of interest) was demonstrated. This can increase the FR considerably as compared with the full-depth range scan. The present prototype contains 40 subarrays of 50 pixels and achieves an FR of 9 fps, for example, with ∼3-cm-depth resolution at a system FOV of 18° × 28° and depth range of ∼4 m with an average laser power of only 0.1 mW. The ROI of the FOV of each subarray was set to 18 cm starting from the nearest surface to the imager in the measurement concerned.

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Henna Ruokamo received the master's degree from the University of Oulu, Oulu, Finland, in 2007, where she is currently pursuing the Ph.D. degree in electrical engineering.

Since 2008, she worked as a Mixed-Signal Integrated Circuit Design Engineer at STMicroelectronics and later at ST-Ericsson until she joined the Circuit and Systems Research Unit at the University of Oulu in 2015, as a post-graduate student. Her research interests include electronic design of single-photon avalanche diode (SPAD)-based arrays for 3-D range imaging applications.

Lauri W. Hallman was born in San Diego, CA, USA, in 1979. He received the M.Sc. and Dr.Tech. degrees in electrical engineering from the University of Oulu, Oulu, Finland, in 2006 and 2015, respectively.

He has done research in areas of laser transmitter development, pulsed time-of-flight range finding, and pulsed Raman spectroscopy. Since 2016, he has been a Post-Doctoral Researcher with the Circuits and Systems Research Unit, Faculty of Information Technology and Electrical Engineering, University of Oulu.

Juha Kostamovaara (M'83–SM'13) received the Ph.D. degree in electrical engineering from the University of Oulu, Oulu, Finland, in 1987.

He is currently a Full Professor in electronics with the University of Oulu, where he teaches courses on analog electronics, microelectronics, and optoelectronics. His main research interests include the development of pulsed time-of-flight devices, circuits, and systems for electronic and optoelectronic measurements. He was an Academy Professor with the Academy of Finland, University of Oulu, from 2006 to 2011 and from 2012 to 2017. He has authored or co-authored more than 450 papers and presentations in international journals and conferences. He holds more than 20 patents, mainly in the field of optoelectronic sensors.