Ka-Band 4-Stack 45nm CMOS SOI Power Amplifier Supporting 3GPP New Radio FR2 band n258

Janne P. Aikio, Alok Sethi, Mikko Hietanen, Timo Rahkonen, Aarno Pärssinen
Faculty of Information Technology and Electrical Engineering, University of Oulu, Finland

Abstract— **This paper presents a fully integrated, four-stack power amplifier for millimeter-wave wireless applications, designed and fabricated using** 45 nm **CMOS SOI technology. The operation frequency is from** 20 GHz **to** 30 GHz**, with a maximum gain of** 13.7dB**. Maximum RF output power, power-added eficiency and output** 1dB **compression point are** 20.5 dBm**,** 29% **and** 18 dBm**, respectively, achieved at** 24 GHz**. EVM of** 12.5% **was measured at average channel power of** 14.5 dBm **using** 100 MHz **16-QAM 3GPP/NR OFDM signal at** 26 GHz**.**

Keywords— **CMOS, SOI, mmWave, PA, 3GPP, NR, 5G.**

I. Introduction

3rd generation partnership project (3GPP) new radio (NR) standard has allocated several new wideband millimeter-wave (mmWave) frequency bands for commercial wireless telecommunication [1]. This is inevitable in order to achieve higher data rates envisioned by the fifth generation (5G) wireless systems. For example, between 24 GHz and 30 GHz bands n258 (24.25 GHz - 27.5 GHz) and n257 (26.5 GHz - 29.5 GHz) propose 3 GHz wide frequency bands. However, at these frequencies we must overcome significant path losses as well as the decreased antenna size. Large phased arrays with RF beamsteering have been proposed to provide decent antenna gain. However, the distance between antenna elements is A/2, (A « 1 cm at 30 GHz), which means that the transmitter needs to be relatively small [2], [3]. In such phased arrays, the output power levels required at each antenna decrease proportionally to the number of antennas. It is evident that each antenna is preceded by a medium power amplifier (PA) preferably integrated on the transceiver RFIC.

In this paper, we describe a four stack PA compatible for 3GPP/NR FR2 bands n258 amd n257 implemented using Global Foundries 45 nm CMOS SOI technology. The nominal VDD of the 45 nm CMOS SOI is 1 V, limiting the achievable voltage swing at the output of the PA considerably. However, the SOI technology enables transistor stacking and hence allows increasing the operating voltage close to 5 V.

II. Stacked Power Amplifier

The proposed PA consists of a stack of four transistors. The schematic of the design is shown in Fig. 1. In this work we are stacking 40 nm floating body devices. The total width of M1, M2, M3 and M4 is 258 pm each. Stacking four transistors enables VDD to be increased up to 4.6 V taking into account the inductor and routing losses. As specified in the design manual 1.1 V is the maximum VDD for one transistor for optimal reliability.

The gate impedances of the transistors are optimized for the inter-stage matching and voltage swing in the source nodes of M2 - M4. Keeping the source waveforms synchronous and progressively increasing is essential in terms of avoiding breakdown. In addition, device size and gate capacitances are dimensioned for direct 50 Q load, which relinquishes the need for additional output impedance matching, thus simplifying the implementation and minimizing the parasitics and losses. The value of the DC feed coil L2 along with the parallel high Q (HQ) metal-insulator-metal (MIM) capacitor C6 is jointly optimized for output matching and maximum gain. The magnitude of the gate capacitances required decreases as one moves up in the stack i.e, C3 is the biggest capacitance at 330 fF and C5 is the smallest capacitance at 208 fF.

The PA is biased in moderate class AB via external analog controls except M1, which is biased using a variable current (Current DAC) source along with a diode connected transistor. With 3 bit control, the gate bias of M1 can be tuned from 100 mV up to 700 mV. Nominal V_{gs} of each transistor is set to 450 mV. In addition, R1 and R2 are used to set 100 mV voltage at V_{g1} in case current DAC is off.

The input is matched with high density (HD) MIM capacitor C1 and center tapped L1 providing high Q and good matching around 25 GHz. Given the size of M1, the input impedance as seen at the gate of M1 is predominantly capacitive. To drive this large capacitive load, the input resonator is designed so that it resonates out the capacitive load, thus making it easier to push power in. Since, the resistive parasitics of the L1 has a significant impact on the Q factor of the resonator, by taking the signal out from the center tap of the L1, the sensitivity to the resistive parasitics is reduced to a large extent. The input and output are DC blocked with HD MIM capacitors C1 and C8 of 1 pF.

III. Measurement Results

The micrograph of the developed integrated stacked PA is shown in Fig. 2. The dimensions of the PA, including the input and output pads is 684 pm x 331 pm = 0.225 mm2 . The active area without pads is 239pm x 331 pm = 0.079mm2, which is very small. HD and HQ MIM capacitors are highlighted in red and cyan rectangles in Fig. 2, respectively.

The proposed PA was measured using Keysight PNA-X network analyzer with Cascade I40 probes. For 1-tone measurements pre-amplifier (Caio Wireless CA263-141) was used to drive the PA into the saturation. The power calibration was performed at the end of the cable before the probe. The

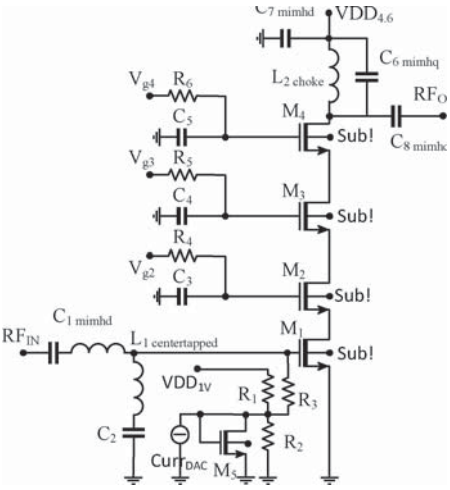

Fig. 1. Schematic of the stacked PA.

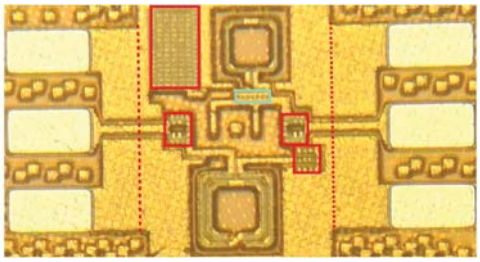

Fig. 2. Photograph of the fabricated PA.

measurement was normalized using the on-chip Thru standard. This procedure was repeated for each measured frequency point. The losses of the probe and the Thru were measured and hence the actual input amplitude of the PA was calculated to the edge of the active PA (dotted red lines in Fig. 2).

A. S-Parameter Measurements

The measured S-parameters at the V_{g1} bias set to maximum setting (i.e. I_{dQ} = 48.7 mA) are shown in Fig. 3. The measurement was calibrated to the tips of the probes using Cascade calibration substrate P/N 101-190. It can seen that the measured peak gain 13.1 dB occurs at 26 GHz. The proposed PA is wideband ranging from 20 GHz to 30 GHz matching 3GPP/NR FR2 bands n257 and n258 [1]. The input and output matching at 26 GHz are —18.5 dB and —11.5 dB, respectively. The corresponding simulated S21 matches the measurements within 1 dB at the center of the band but estimate slightly narrower bandwidth. This is due to the fact that EM-modeled matching resonators estimate higher Q-values and less losses than fabricated circuit.

B. 1-Tone Measurements

Gain, power added efficiency (PAE) and AM-PM as a function of output power at 26 GHz (center of 3GPP/NR FR2 band n258) with available V_{g1} bias settings are shown in Fig. 4. The achieved Psat at 26 GHz is 20 dBm, which is achieved

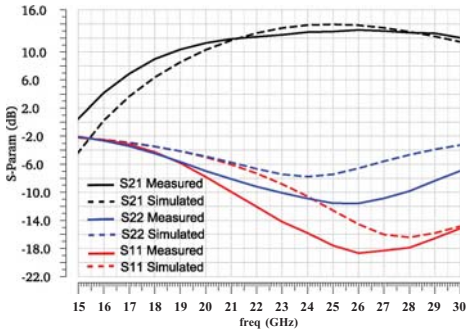

Fig. 3. Measured and simulated S-parameters of the stacked PA.

with each bias level. On the other hand the peak PAE of 29 % at 26 GHz is measured at the lowest bias. The lowest bias is very close to class B and thus the effect of self bias is obvious. This is also the reason why AM-PM of the I_{dQ}=17.7 mA decreases later than the other curves. The total AM-PM is less than 16°. However, the most significant difference as a function of bias level can be seen in PAE results in the back-off region. For example, PAE at Pout = 14 dBm varies already 6.5 percent units (9.7% at I_{dQ}=48.7mA and 16.2% at I_{dQ}=17.7mA), while the gain difference is 2.2 dB (11.5 dB at I_{dQ}=17.7mA and 13.7 dB at I_{dQ}=48.7mA).

The simulation results (dashed lines) using maximum V_{g1} bias setting are also shown in Fig. 4. It can be seen, that the gain is matching very well with the measured large signal gain at lower power levels. However, simulated results predict higher compression level than measurements and higher quiescent current with the same bias voltage. Similarly, the simulated AM-PM shows less phase distortion. The main difference can be seen in PAE response, which is mainly a result of larger quiescent current of the simulated PA.

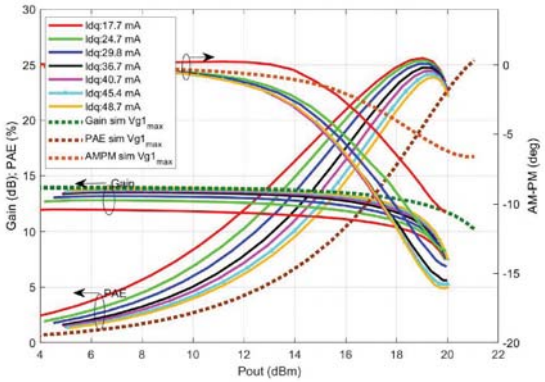

Fig. 4. 1-tone power sweep measurements at 26 GHz with different Vgl bias.

The main figure of merits are plotted as a function of frequency in Fig. 5. The solid lines correspond to the lowest bias value (I_{dQ} = 17.7 mA) and dashed line to the highest bias value (I_{dQ} = 48.7 mA). From Fig. 5 a) it can be seen that the maximum 1 dB compression point and Psat are 18.8 dBm and 20.5 dBm at 24 GHz, respectively. The difference between the curves is small in the saturation. PAE curves show similar

behavior in Fig. 5 b). The peak PAE is 29 % at 24 GHz and decreases at higher frequencies. The difference between high and low bias curves is small at 3dB compression and Psat but increase towards the back-off region (as mentioned above) being already 6.5 percent units at 6dB back-off at 26 GHz.

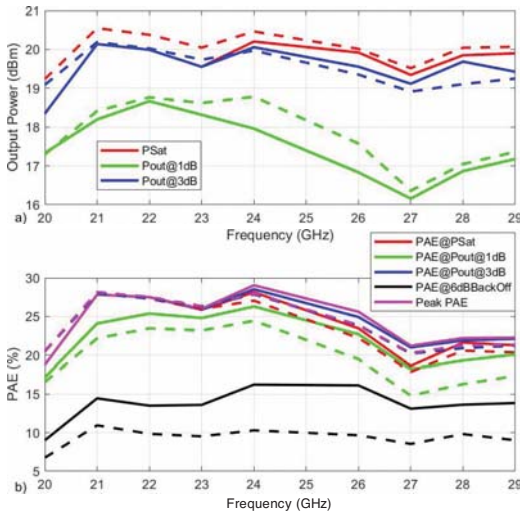

Fig. 5. Measured figure of merits vs. frequency. a) Pout and b) PAE with IdQ = 17.7mA (solid line) and IdQ = 48.7mA (dashed line).

C. Measurements with Modulated Signal

Finally, error vector magnitude (EVM), PAE and adjacent channel leakage ratio (ACLR) was measured using 100 MHz 16-QAM 3GPP/NR OFDM signal. The measurements were performed with Keysight UXA N9040A signal analyser. 3GPP/NR FR2 OFDM 100MHz wide 16-QAM signal was generated using Keysight arbitrary waveform generator M5502A and mixed to millimeter waves using Keysight E8267D signal generator.

The results are shown in Fig. 6. EVM and PAE are plotted as a function of output channel power using three different bias currents, I_{dQ} = 17.7 mA (Red lines), I_{dQ} = 36.7 mA (blue lines) and I_{dQ} = 48.7 mA (black lines). In terms of EVM blue and black lines are overlapping, while the EVM with the lowest bias is above 5% at lower output channel power levels but overlapping with others above 13 dBm of output channel power while the EVM level is at 8%. The EVM specification for the used signal is 12.5% [1], which is achieved at 14.5 dBm regardless of the bias current, which is excellent result taken into account that the measured 1 dB compression point at 26 GHz is around 17.5 dBm. However, in terms of ACLR the 3GPP/NR specification for the used signal is -28 dBc. Based on the results shown in Fig 6 b) it is interesting to note that the best ACLR results at the specification limit (–28dBc) is achieved with the lowest bias current (red lines) at output channel power of 13.5 dBm while EVM is at the level of 9 %. With higher bias currents the ACLR curves increase linearly, overlap and are symmetrical, while asymmetry and higher low level distortion is notable in the lowest bias current (I_{dQ} = 17.7 mA). There seems to be an IMD sweet spot between 12 dBm and 13 dBm before ACLR begins to rapidly collapse and reach the curves of the higher bias.

PAE results in Fig. 6 a) are quite different. For example, at specified EVM of 12.5% (channel power=14.5dBm). Measured EVM is the same for each bias setting but with I_{dQ} = 48.7 mA PAE is 12%, which is already a good result, but with I_{dQ} = 17.7 mA bias current PAE is reaching up to 16%. However, linearization is required to meet the ACLR specifications for these channel power levels. The presented results are competitive against the recent State-of-the-Art e.g. [2], [3] and [4].

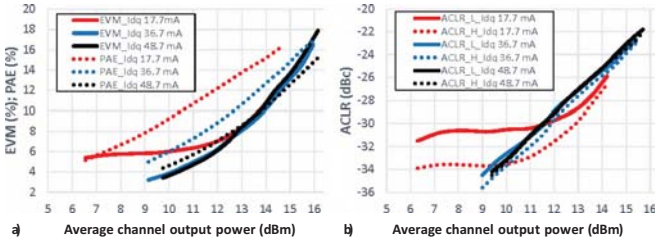

Fig. 6. a) EVM, PAE and b) ACLR vs. output channel power with different bias levels at 26 GHz using 100 MHz 16-q Am 3GPP/NR2 OFDM signal.

IV. Conclusion

In this paper we proposed a 4-stack power amplifier implemented using 45 nm CMOS SOI technology. It was shown that the PA can operate over a frequency range of 20 GHz - 30 GHz. The PA achieved a maximum saturated power of 20.5 dBm along with a maximum peak PAE of 29 % and the output 1 dB compression point of 18.5 dBm at 24 GHz and maximum gain of 13.7 dB at 26 GHz. The active area is as small as 0.079 mm2. The measured ACLR of –28dBc was measured at channel power of 13.5 dBm using 100 MHz 16-QAM 3GPP/NR OFDM signal at 26 GHz with the EVM and PAE of 9 % and 15 %, respectively, and hence meeting the specifications for 3GPP/NR FR2 band n258.

References

[1] 3GPP, "Base Station (BS) radio transmission and reception," 3rd Generation Partnership Project (3GPP), Technical Specification (TS) 38.104, 3 2019, version 15.5.0. [Online]. Available: http://www.3gpp.org/ftp/Specs/archive/38_series/38.104/38104-f50.zip

[2] C. Li, M. Wang, T. Chi, A. Kumar, M. Boenke, N. Cahoon, A. Bandyopadhyay, A. Joseph, and H. Wang, "A high-efficiency 5G K/Ka-band stacked power amplifier in 45nm CMOS SOI process supporting 9gb/s 64-qam modulation with 22.4 % average pae," in *2017 Texas Symposium on Wireless and Microwave Circuits and Systems (WMCS),* March 2017, pp. 1-4.

[3] S. N. Ong, S. Lehmann, W. Chow, C. Zhang, C. Schippel, L. H. K. Chan, Y. Andee, and D. M.and Harame, "A 22nm FDSOI Technology Optimized for RF/mmWave Applications," in *2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC),* 2018, pp. 72-75.

[4] J. Aikio, M. Hietanen, N. Tervo, T. Rahkonen, and A. Parssinen, "Ka-band 3-stack power amplifier with 18.8 dBm Psat and 23.4 % PAE using 22nm CMOS FDSOI Technology," in *2019 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR),* January 2019, pp. 1-4.