Two Capacitive-Pulling Techniques to Aid the Settling of SC Residue Amplifier

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***Abstract*—This paper presents two capacitive-pulling techniques to aid the settling of the switched-capacitor residue amplifier in a pipeline analog to digital converter. The main idea is to pre-charge the load capacitors to proper voltages, connect them to the output of the operational trans-conductance amplifiers (OTAs) during the evaluation phase, and hence pull the passive charge sharing so that the initial voltage step of the OTA input is instantly minimized. The OTA hence skips the slew region, and enters into the linear settling region, leaving just a minor charge to be moved by the OTA. This allows you to get the same settling precision with saving 30% power consumption of the OTA using minimal three-level pre-charged method. Alternatively, the conversion rate can be increased by over 30% using the continuously controlled pre-charged method.**

Keywords—pre-charge; initial input voltage; capacitor-pulling; charge redistribution; slew rate; pipeline ADC; switched-capacitor

I. INTRODUCTION

For medium and high resolution applications, the pipeline analog to digital converter (ADC) represents a very suitable architecture and uses a switched-capacitor (SC) circuit based on a trans-conductance amplifier (OTA) for sub-ranging AD conversion and for amplifying the residue. SC circuits use OTAs to transfer the charge, and there will be large transient voltage spikes Vi0 in the inputs of the OTA. If the initial step exceeds the linear input range Vlin of the OTA, it drives the OTA into the slewing, where the OTA output current gets clipped to Imax. The time spent in slewing is taken away from the linear settling time, and this causes highly non-linear settling error [1]. Alternative slew rate (SR) enhancing approaches include: increasing DC bias current of the OTA which increases the power dissipation; adaptive biasing technique in a class-AB input stage [2], but combining the class-AB operation and rail to rail signal swing in [2] usually requires a complicated biasing circuit to extend the common-mode input range of the buffer, this increases the overall circuit complexity and power consumption; a novel adaptive biasing circuit [3] that senses the voltage difference of input and boosts the tail current by a positive feedback, but only works for single stage OTAs; [4] adopts an auxiliary monitor circuit to adjust the driving current but can hardly operate under a low supply voltage; [5] employs a dynamic bias current for a large output current but only works for single stage OTAs; [6] presents a low-voltage SR enhancement technique used in two-stage OTA which detects input voltage of the OTA and brings an external boost current to the OTA while the OTA is slewing; a charge pump [7], where the on-times of up and down currents are controlled by two comparators, performing rapid change of the OTA bias condition between a low-current mode and a high-current mode during non-overlapping clock periods of the two phase clocks; Modifying the OTA bias requires that the OTA is dimensioned to handle the boosted current, and may cause some internal settling transients. In this paper we present a solution, where the boosting is done outside the OTA, based on prior knowledge of the charge sharing. This makes the design of the OTA easier and the correction faster. We utilize passive capacitive charge-sharing principle, where two capacitive-pulling methods are used to pull the charge sharing so that the initial step of OTA is instantaneously minimized close to the final steady-state. Section II describes the concept of charge redistribution in a double sampling OTA sharing SC residue circuit in a pipeline ADC. Section III introduces two capacitive-pulling methods which aid the settling of SC residue circuit. The first gives a coarse cancellation with minimalistic implementation. It has been previously presented in [8], but is now analysis in more depth. Second, we present a more precise and more complex active charge-pulling technique requiring some additional hardware. The performance of the implementations is compared, and it is seen that the first one is more suited on reducing power consumption, while the latter helps to increase the sampling rate. Section IV presents the circuit implementations. Section V shows experimental simulated results of the two methods, Section VI gives the conclusions.

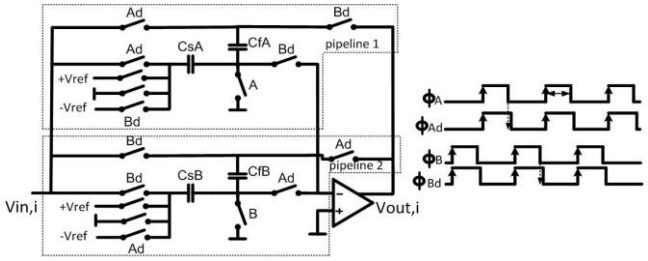

Figure 1. Double sampling, OTA sharing SC residue circuit used in pipeline ADC.

II. CHARGE REDISTRIBUTION OF TRADITIONAL SC CIRCUIT

Figure 1 shows a double sampling, OTA sharing SC residue circuit that is commonly used in pipeline ADCs. The residue OTA has two set of capacitor banks (bank A and bank B). The

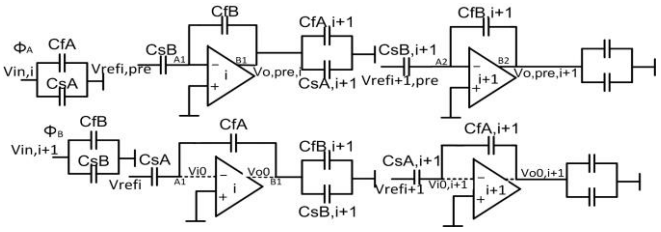

Figure 2. Charge redistribution in a double sampling OTA sharing SC residue circuit used in pipeline AD converter.

two capacitor arrays are used alternatingly by the same OTA: when the input signal is being sampled by one capacitor bank, the other capacitor bank is connected to the OTA for the evaluating the residue. Figure 2 shows the capacitor connection of the 1st and the following stage at the end of sampling phase ϕA and at the beginning of evaluation phase ϕB. The passive charge redistribution equation (1) [8] is the core of the capacitor pulling idea, and to understand the operation proposed implementations, it is explained in some detail here. At the very beginning of ϕB we assume that the OTA itself has no effect yet, and the total charge is passively and almost instantaneously redistributed. The instantaneous charge redistribution results into the initial voltages at the input and the output of the two OTAs (V_{i0}, V_{o0} and $V_{i0,i+1}$, $V_{o0,i+1}$), from where the OTAs start the actual settling. Since the total charge in node A1 or B1 has no path to move in the beginning of ϕB, the total charges of node A1 or B1 in the beginning of the evaluation phase are the same as the end of ϕA. The charge conservation in nodes A1 and B1 of Fig. 2 are shown in (1), and from these the initial voltages Vi0 and Vo0 can be solved. Here Vrefi and Vin,i are the subtracted reference voltage and input voltage of the first stage, and V2 and V1 are the voltage of the next stage sampling capacitors – if not zeroed or pre-charged, those will be the reference and previous output of the next stage.

$$\begin{aligned} A1&: CsA\times\left(V_{i_0}-V_{refi}\right)+CfA\times\left(V_{i0}-V_{o0}\right)=CsA\times\left(0-V_{in,i}\right)+CfA\times\left(0-V_{in,i}\right)\\ B1&: CfA\times\left(V_{o0}-V_{i_0}\right)+V_{o0}\times\left(C_{fB,i+1}+C_{sB,i+1}\right)=CfA\times V_{in,i}+V_1\times C_{fB,i+1}+V_2\times C_{sB,i+1}\end{aligned} \quad (1)$$

When Vi0 is smaller than the linear input range Vlin, no slewing occurs, the SC circuit operates fully linearly, and the charge-transfer error is proportional to the initial input Vi0. When Vi0 is large, the OTA will be slewing during the first part of the integration phase. Hence minimizing Vi0 is the key factor determining the amount of distortion.

III. Charge Redistribution Technique

The main idea of charge redistribution technique is to add appropriate amount of pre-calculated charge Qpre at the output of the OTA in the beginning of the evaluation period. Injected Qpre helps to move the charge and forces Vi0 close to zero, so that the OTA has little linear correction to do, and the output voltage reaches desired value quickly as well.

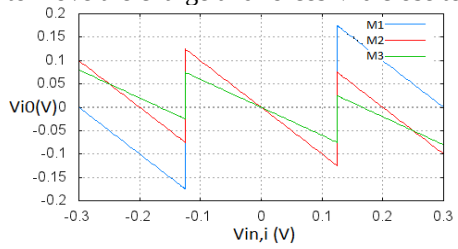

Figure 3. Vi0 as a function of Vin,i using three simple pre-charged methods

A. Minimal Pre-charged Technique

The basic idea is to simply pre-charge the load capacitors CsB,i+1, CfB,i+1 with the proper fixed voltages V1 and V2 in (1). To keep the implementation simple, we try to easily pre-charge V1 and V2 by using fixed and available voltage values, so that no additional OTAs on the purpose of pre-charging the load capacitors would be required. (1) Method 1 (M1): V1=0, V2=0; Zeroing the next stage sampling capacitors CsB,i+1 and CfB,i+1; (2) Method 2 (M2): V1=-Vrefi, V2=0; Pre-charging CfB,i+1 with -Vrefi, zeroing CsB,i+1; (3) Method 3 (M3): V1=-2*Vrefi, V2=2*Vin,i; Pre-charging CfB,i+1 with -2*Vrefi, pre-charging CsB,i+1 with 2*Vin,i; The initial input Vi0 is calculated by a computer algebra system-Maxima according to the above three methods, and plotted in Figure 3. [8] introduced several methods of minimal pre-charged technique in details and presented their schematics of circuit implementations. Here, we just briefly repeat them, and only focus on the proper method which can achieve the power consumption purpose. Simply by zeroing load capacitors (M1) we can reduce the max(|Vi0|) to 0.175V. By pre-charging CfB,i+1 to -Vrefi and zeroing CsB,i+1 (M2), the max(|Vi0|) drops to 0.13V. The Vi0 range is further minimized in M3 to the max(|Vi0|) of 0.075V. M3 seems to give the best reduction, but it increases the load capacitance during the evaluation phase since the capacitor CsB,i+1 has to be connected between the positive and negative output of the (i-1)th stage to pre-charge 2*Vin,i. As M2 does not add additional loading to the signal path, it is chosen for further study and implementation in Section IV.A. Using this extremely simple pre-charged method (M2), we can get rid of the biggest input initial step and speed up the settling.

B. Capacitive Pulling with Continuosly Controlled Pre-charge Voltage

Above we used only easily available voltages for pre-charging CL. Here the V1=V2=Vpre in (1) is calculated precisely, to result in complete nulling of Vi0. Charging CsB and CsB to same voltage Vpre, and solving (1) for Vi0=0 we get Vpre = 2.5×Vin,i – 1.5×Vrefi.

$$Vpre=2.5\times Vin,i-1.5\times V_{refi} \quad (2)$$

As shown above, Vpre does not depend on previous voltages of the previous phase, but is only affected by the sampled voltage Vin,i and reference voltage Vrefi. Yet, we need a summing amplifier to form Vpre.

IV. Circuit Implementations

A. Minimal Pre-charged Technique

As shown in Figure 4 the conventional double sampling is used in the first stage of the most significant bit. The sampling capacitors of the following stage act as the pre-charged load capacitor of the first stage, and are connected to the output of the first stage during the evaluation phase. To give enough time for pre-charging, one additional capacitor bank is needed: when bank A is sampling, capacitors in bank B are evaluating in the feedback configuration, and bank C is connected to fixed pre-charged voltages 0 and ±Vref. This repeats, and generates fs/3 periodicity. This allows us to sample in capacitors A,

evaluate with capacitors B and pre-charge capacitors C all at the same time. The pre-charging capacitor bank has three duplicated capacitors of Cf that are pre-charged to +Vref, -Vref and 0 separately before obtaining the comparison result, and chosen when the comparison result from the 1.5b-ADC block of the first stage is ready. The ADC comparator outputs are passed to the pre-charged capacitor chosen (PCC) block, where the decision is held and encoded to digital selection signals (ctrl1_na, ctrl1_nb, ctrl1_nc; ctrl2_na, ctrl2_nb, ctrl2_nc; ctrl3_na, ctrl3_nb, ctrl3_nc).

B. Continuously Controlled Pre-charged Technique

To pre-charge the load capacitor CL of a residue OTA stage to Vpre given in (2), we need a switched capacitor summing OTA as a pre-charging block added between the 1st and 2nd multiplying Digital-to-Analog Converter MDAC, as shown in Figure 5. The parallel time-interleaved switched capacitor summing OTA has two capacitor banks working in opposite clock phases by sharing the same OTA, which performs the pre-charging equation (3), i.e. the summing OTA samples the input signal Vin,i by the factor 2.5, then subtracts 1.5Vrefi.

$$Vpre = 2.5\times Vin,i - 1.5\times V_{refi} = \frac{Cin}{Csum}\times Vin,i - \frac{Cref}{Csum}\times Vrefi \quad (3)$$

To allocate enough time for pre-charging the load capacitor of 1st stage, we need to introduce one full cycle delay in the processing. This is implemented by having three alternating capacitor banks A,B,C in MDAC1. During the phase I shown in Table I, while the input voltage Vin,i is sampled onto CsA and CfA of the 1st stage, Vin,i is also sampled by the summing OTA. After the input is sampled onto the capacitor bank A of MDAC1 during the phase I, the sampled signal is held in the capacitor bank A during the phase II, during which time the pre-charged voltage Vpre is calculated according to (3) into the load capacitor (bank C of MDAC2) of the 1st stage. Then in phase III the capacitor bank A is connected as feedback around MDAC1 and the pre-charged load capacitor (bank C of MDAC2) is connected its output. In MDAC2 we need two sets of sampling capacitors, the one being pre-charged and the other one sampling. Hence, we have four capacitor banks rotating in order A→B→C→D→A. While the bank A is sampling during the phase I, bank B is being pre-charged, bank C is in the evaluation operation and D is not used. As seen the schematic of Figure 5 when ctrlA is on, Vin is sampled by CsA&CfA, and Vin is also sampled by Cin of the summing OTA since ctrla is on at the same time, CsB&CfB are in the evaluation mode, CsC&CfC do not work. In the following phase, when ctrlB is on, the sampled input signal is held in CfA&CsA, during which time the pre-charged voltage Vpre is calculated according to (3) into the load capacitor (bank C of MDAC2) of the 1st stage, Then the third phase when ctrlC is on, CsA&CfA which have the sampled signal are connected as feedback around MDAC1 to transfer the charges for evaluation period, at the same time the pre-charged load capacitor (bank C of MDAC2) is connected its output for add appropriate amount of pre-calculated charge Qpre at the output of the OTA in the beginning of the evaluation period. The initial input voltage drops which avoids the biggest input initial step and bypasses the slew limited behavior, allowing OTA to operate linearly.

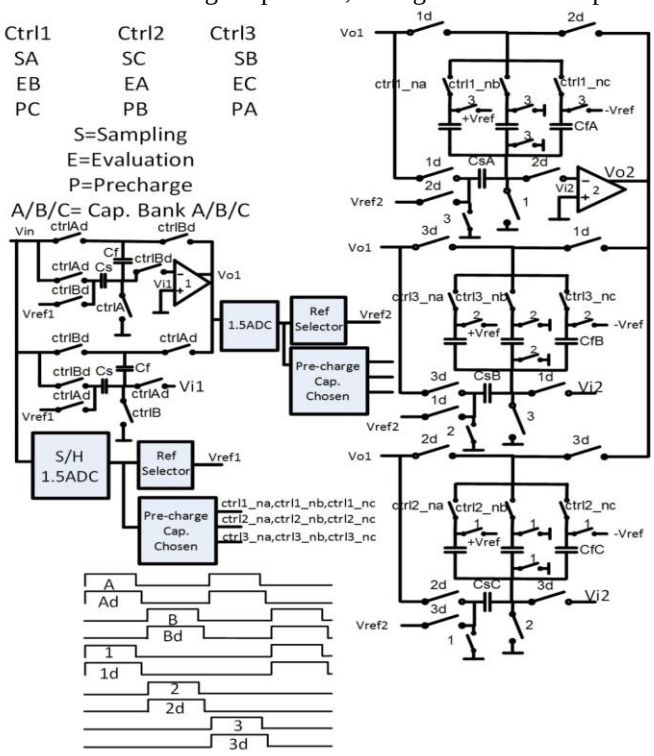

Figure 4. Circuit implementation of M2 for SC residue of pipeline stage

TABLE I. CAPACITOR BANK ARRANGEMENT OF EACH PHASE

		phase I	II	III	IV
MDAC1	CsA,CfA	Sampling	------	**Evaluation**	Sampling
	CsB,CfB	Evaluation	Sampling	------	Evaluation
	CsC,CfC	------	Evaluation	Sampling	------
MDAC2	CsA,CfA	Sampling	------	Evaluation	Pre-charge as CL
	CsB,CfB	Pre-charge as CL	Sampling	------	Evaluation
	CsC,CfC	Evaluation	**Pre-charge as CL**	Sampling	------
	CsD,CfD	------	Evaluation	Pre-charge as CL	Sampling
Pre-charge Circuit Block	Cin	Sampling	**Pre-charge CL**	Sampling	Pre-charge CL
	Cref,Csum	Empty Charge		Empty Charge	
	Cin'	Pre-charge CL	Sampling	Pre-charge CL	Sampling
	Cref',Csum'		Empty Charge		Empty Charge

The sampling frequency fs is not changed, but capacitor banks rotate at fs/3 in the 1st stage and rotate at fs/4 in the 2nd stage. The operation phases are shown in Table I. Note that the first stage needs 3T to process an input sample, determine the bits, and pass the residue to the 2nd stage. Each following stage needs 2T to process the sample and then propagate to the next stage. Hence the total data latency is 3T+8×2T=19T which is larger than in normal pipeline structure.

V. EXPERIMENTAL RESULTS

A. Minimal Pre-charged Technique

There are many advanced methods to deal with non-coherent test measurements e.g. [9]. In our simulation-based study we can avoid spectral aliasing by choosing a rational relationship between the test and sampling frequency, and use the figures of merit defined in [10]. The proposed SC residue circuit is

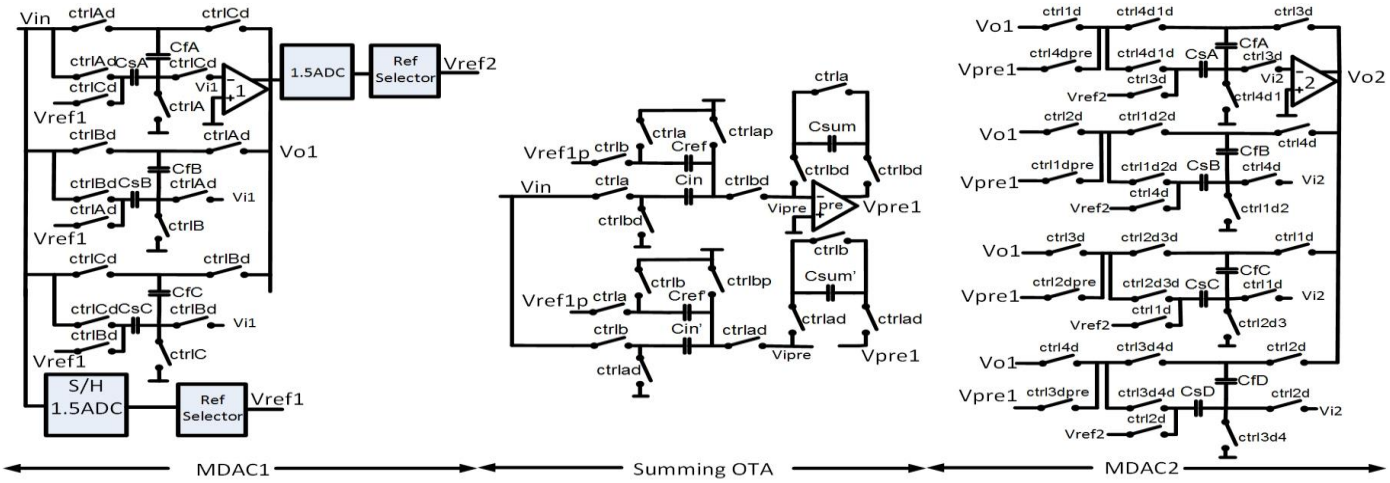

Figure 5. Schematic of the continuous controlled pre-charged technique.

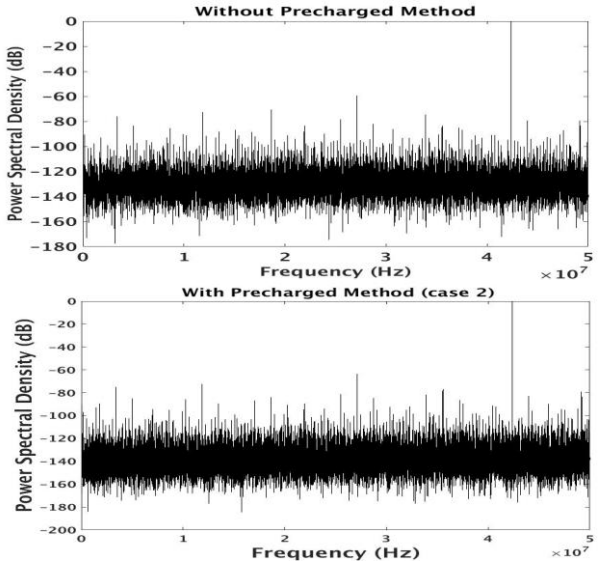

Figure 6. FFT performance of SC residue with an Nyquist-frequency input (Top: original implementation, bottom: pre-charged implementation M2)

designed using 90-nm generic CMOS process with 1.2-V supply voltage. The input signal frequency fin is 42.37 MHz, sampling frequency is 100MHz. Figure 6 shows the simulated 65536-points FFT output spectrum obtained from Cadence for the original structure and minimal pre-charged implementation (M2). The conventional structure resulting a spurious-free dynamic range (SFDR) of 59.4dB and signal-to-noise and distortion ratio (SNDR) of 58.3dB, while the proposed pre-charged M2 structure has SFDR of 63.8dB and SNDR of 62.3dB, revealing a 4dB SNDR improvement which is corresponding to about 0.67 bit increase of the effective number of bits (ENOB), 4.4dB SFDR improvement. The PCC block only introduces several DFFs (no additional OTAs), the increased complexity on the power consumption is minimal, compared to the ENOB benefit gained from the proposed technique. One of the main design considerations in SC circuit is to achieve required settling precision with low power consumption (Pdiss). With the proposed minimal pre-charged method, no additional amplifiers are required, but we can relax the OTA performance to get the original resolution with reduced power consumption. Since the input initial voltage is minimized we can relax both slew rate and bandwidth requirements.

TABLE II. OTA PERFORMANCE COMPARSION

Op-amp	**Original Op-amp in SC Without Pre-charged method**	**Relaxed Op-amp in SC with Method 2**
OTA structure	single-stage folded cascaded OTA	single-stage folded cascaded OTA
PhaseMargin	86 degree	86 degree
Unit Gain Bandwidth	452 MHz	361 MHz
Slew Rate	250 V/us	170 V/us
Current Ibias	166.25 uA	113 uA
SNDR	58.3 dB	58.6 dB
SFDR	59.4 dB	60.5 dB

Table II summarizes the main characteristics of the OTA. The static current Ibias of the original OTA is 166uA with a 452MHz unit gain bandwidth (UGBW), the proposed OTA shows a 113uA Ibias with 361MHz UGBW, indicates that utilizing pre-charged method 2 slew rate and UGBW of the OTA can be decreased about 30% to get the same resolution (about 58dB SNDR) compared to the original structure of SC residue circuit with the tighten OTA specification. The black solid curve in Figure 7 is the power spectral density (PSD) of the SC residue circuit without pre-charged method (M0), the grey dashed curve is the spectrum with the proposed pre-charged method 2 (M2), where the relaxed OTA of Table II is embedded. Figure 7 illustrates OTA's power can be saved about 30% to achieve the same dynamic specifications of the SC circuit compared with the original SC circuit which has a higher power consumption OTA.

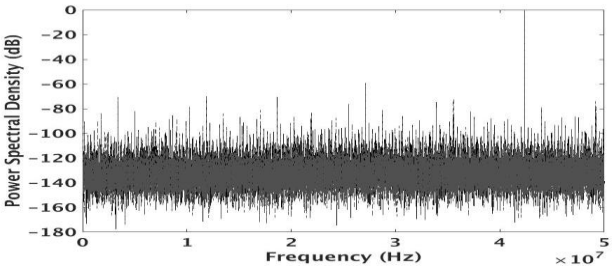

Figure 7. FFT performance of SC residue on the purpose of saving the power

B. *Continuously Controlled Pre-charge Technique*

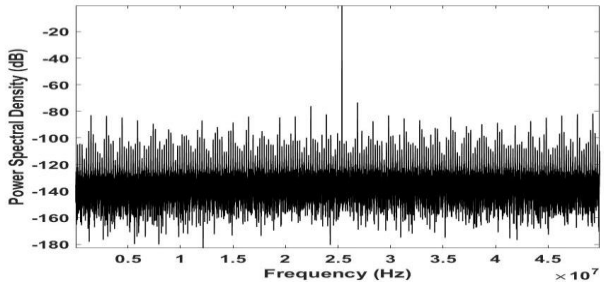

Figure 8(a). FFT spectra of conventional SC residue circuit with fs=100MHz

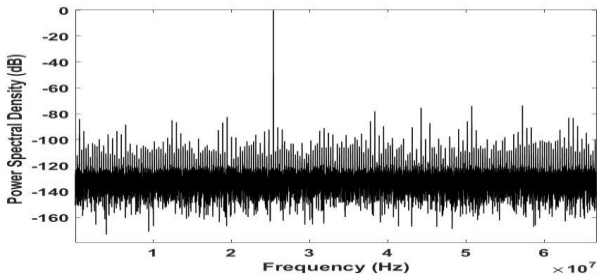

Figure 8(b). FFT spectra of proposed pre-charged technique with fs=133MHz

Here the pre-charge summing amplifier adds some power consumption, so it is more feasible to see if we can achieve higher sampling rate with the same power dissipation. Figure 8(a) shows the simulated 65536-point FFT output spectrum obtained from circuit simulation for the original structure with the input signal frequency fin is 25.37MHz and sampling frequency fs=100MHz (solid black line) and Figure 8(b) shows the FFT output spectrum with the proposed pre-charged method with fs increased to 133MHz. The SFDR and SNDR of the conventional structure with fs=100MHz were 73.4 and 67.6dB, resulting in the ENOB of 10.94 bit. The SFDR and the SNDR of the pre-charged speed-up structure with fs=133MHz were 73.6 and 67.2 dB, resulting in the ENOB of 10.87 bit.

TABLE III. OTA PERFORMANCE COMPARSION

OTA	**Original main OTA in SC Without Pre-charged method**	**Relaxed main OTA in SC with Method 2**	**pre-charge summing OTA**
Accuarcy	10b	10b	3%
OTA structure	two stage folded cascode OTA with Cc	two stage folded cascade OTA with Cc	one stage telescopic OTA
PhaseMargin	55 degree	71 degree	75 degree
Gain	71dB	71dB	300
Unit Gain Bandwidth	520 MHz	540 MHz	560MHz
Slew Rate	248V/us	62.4 V/us	266V/us
Load capacitor	2.375pF	2.375pF	------
Cs,Cf	0.75p	0.75p	------
Cc	0.5pF	0.5pF	------
Total Static I	1016uA	465uA	432uA
Total settling time	8ns	5.5ns	7.1ns

Table III summarizes the main characteristics of the OTA used in the original and pre-charged structure. The total power consumption of the SC residue circuit is dominated by the main OTA and summing OTA of pre-charged circuit block. The total static current consumption of 1016uA by the original OTA without pre-charged method, indicates the static power dissipation of 1.22mW. The total static current consumption of 897uA (465uA+432uA) by the relaxed main OTA and the pre-charged summing OTA, indicates the static power dissipation of 1.08mW, which is slightly smaller than the original structure. At the same time, the sampling frequency is increased from 100MHz to 133MHz. The complexity of the pipeline stage is increased and for the switches of a MDAC more clock signals with different phases are needed, and the pre-charged circuit block does induce some power. However due to the power saving of the relaxed main OTA, the total power consumption including the increased complexity remains almost the same as the conventional structure, but the sampling frequency can be increased over 30% to achieve the same performance as the conventional SC residue circuit.

VI. CONCLUSION

This paper presented two new architectures of capacitive-pulling technique that are suitable for speeding up the settling of SC OTAs in pipeline ADCs. With the minimal pre-charged technique, one simply pre-charges the load capacitors with selectable fixed and already available voltages, and no additional OTAs are required. Due to reduced input transients, the same performance is possible to achieve with amplifier with 30% lower power consumption. In the more complex approach, the load capacitors are charged to a continuously controlled voltage, and a more precise cancellation is achieved at the cost of an additional one-sample delay, one additional time-interleaved capacitor bank, and a moderate performance summing amplifier to form the correct pre-charged voltage. Vpre is calculated by the charge redistribution equations and implemented by the summing amplifier. According to the simulations the 1st OTA skips the slew rate region and settles more quickly. This makes it possible to achieve 30% higher sampling frequency with the same power consumption.

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