A Pulse Width-Controlled CMOS Laser Diode Pulser and a Time-Gated Time-Resolved SPAD Array Transceiver Chip for Diffuse Optics

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Abstract—A pulse width-controlled CMOS pulser for a semiconductor laser diode (LD) and a time-gated time-resolved 8×4 single-photon avalanche diode array with a time-to-digital converter (TDC) were designed on a single integrated circuit and simulated by using a 150 nm technology. The pulse width of the driving current can be adjusted from 0.5 ns to 2.5 ns with a resolution of 100 ps. The start time of the time-gating can be adjusted over a dynamic range of 4.8 ns with a resolution of 100 ps and, furthermore, a 121 ps time-gating can be achieved. The returning photons are detected by the TDC with a resolution of 50 ps and stored to the 128 14-bit counters for merging to the distribution time-of-flight histogram. The average power consumption of the whole system was 377 mW at a repetition rate of 10 MHz.

Keywords—Diffuse optics, Time-correlated single photon counting, TDC, DToF

I. INTRODUCTION

Research of diffuse optical imaging (DOI) has recently become very popular, since it can be used for characterizing diffusive media, for instance, wood, food, pharmaceuticals, or living tissue. Furthermore, operating on the red and near-infrared spectral range (600 nm – 1100 nm) enables a non-invasive approach to examine the tissue, because these wavelengths have the ability to probe deep (~cms) due to the significantly higher scattering coefficient than the absorption coefficient of the tissue [1]. The detected back-scattered optical signal can be used to define the microstructure of the tissue. DOI can be used in diverse medical field appliances such as optical mammography and brain mapping. Moreover, muscle oxygen saturation (SmO₂) can be monitored during physical exercise in athletic training with DOI [2].

There are various techniques used in wearable optical appliances. However, most of the commercial wearable optical appliances, such as smart swatches and activity bands, use continuous-wave (CW) or frequency-domain (FD) technologies due to the small scale of their components [2]. These appliances can measure the subject's heartbeat and oxygen content of the blood. However, the measurements are disturbed by movement during the exercise because technology is based on analog signal processing which is highly sensitive to movement induced interference. Moreover, to gain more accurate information of an athlete reaching an anaerobic state, for example, the appliance must be able to monitor muscle oxygenation, which can be achieved by deeper probing. Unfortunately, the attempt to probe deeper with a CW-based design will deteriorate the signal-to-noise ratio (SNR), as can be seen in Fig. 1 a), because the distance between the source and the detector must be increased as a result of the property of the CW to only enable measuring of the light intensity [3].

In contrast to CW-based systems, time-domain (TD) diffuse optical technologies allow adding an extra dimension in the measurement. Information of a depth is bound to the back scattered photon's arrival time, since the deeper the photon penetrates, the more time it takes to travel back to the surface. As the inspected medium characters can be determined from the distribution of a time-of-flight (DToF) histogram [3,4] shown in Fig. 1 b), the distance between a source and a detector can be kept as short as the technology allows and thus the time-of-arrival (ToA) of the photons of T1, T2 and T3 corresponds to the characteristics of a tissue from the depths 1, 2 and 3, respectively. Therefore, TD-based designs can achieve a higher SNR than CW-based designs, since a shorter roundtrip induces more photons to the detector. However, the detector can be saturated by the high amount of early photons from superficial layers of the medium. This issue can be avoided by using a time-gated single-photon avalanche diode (SPAD) to detect photons from a specific time window [5]. Furthermore, SNR and the dynamic range of DToF can be increased even more when time-gating is used [5]. For example, by selecting a time gate position T3 (in Fig. 1 b)) to enable the SPAD, the optical power can be incremented, providing better photon detection probability, and thus a higher count of photons that have penetrated deeper. In addition, SNR will be increased without the detector becoming saturated by early photons.

Despite the many advantages of TD systems, small-scaled designs have been possible over the past couple of years by means of the development of integrated circuit (IC) technologies. For example, in [6] the small-sized 10×10 mm² module with a time-gated SPAD, a laser driver and an analog counter have been fabricated. However, the proposed structure cannot produce DToF of the detected photons because only the pre-defined time gate width has been used in the measurements to collect back scattered photons. All needed components in TD diffuse optics, laser diode (LD) drivers, SPADs and time-to-digital converters (TDC) can be fabricated in a CMOS technology [7-9]. Thus, the small-scaled transceiver into a single die for a TD diffuse optics is feasible and will pave the way for fabricating a wearable device for health care and sport applications.

In this work, both the pulse width-controlled CMOS pulser for a semiconductor LD and the time-gated time-resolved 8×4

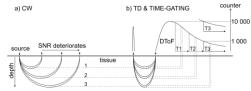


Fig. 1. a) The principle of CW-based measurement, and b) the principle of TD-based measurement including DToF and time-gating.

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SPAD array with the TDC were designed in a single IC and simulated by using a 150 nm technology. The personal monitoring of muscle oxygenation will be possible due to the ability of a time-gated time-resolved diffuse optics (TG-TR-DO) system to probe deeper than a CW-based system [3].

II. ARCHITECTURE OF TG-TR-DOI

The block diagram and the time chart of the designed TG-TR-DOI system are shown in Fig. 2 a) and b), respectively. The IC comprises a pulse width adjustable LD driver (PWA LD driver), and a time-gated time-resolved SPAD detector array (TG TR SPAD array). The PWA LD driver consists of a delay-locked loop circuit (DLL circuit), a delay line circuit (DL circuit), a buffer tree, and 24 driver cells. The DLL circuit is locked to an external reference clock to stabilize the delay elements used. The trigger pulses are supplied to pulse width control at 10 MHz (max. 25 MHz). The pulse width can be adjusted from 0.5 ns to 2.5 ns with a resolution of 100 ps to achieve a proper current pulse for a specific LD. The branchlike buffer tree distributes the pulse from the DL circuit to the all 24 driver cells with enough ability to drive all their gates. The driver cells simultaneously switch the current pulse through the LD creating an optical pulse, as seen on the time chart in Fig. 2.

The TG TR SPAD array consists of a DL circuit, for timegating, a 7-bit TDC with the LSB of 50 ps, 32 SPAD frontend electronics, and an 8×4 SPAD array. The start_gating signal to the DL circuit (time-gating) is shared from the PWA LD driver's buffer tree. The signal can be delayed from zero to 4.7 ns with a resolution of 100 ps by means of the DL circuit (time-gating) controlling the starting time of the load signal of SPADs and the start signal of the TDC through SPAD electronics. Hence, the early photons can be bypassed. The SPADs in the array are loaded by SPAD front-end electronics, and each of them can be disabled individually by a hot-pixel elimination control word in the case of a high dark count rate pixel. The differences of the start and stop signal are stored in IC for DToF by the TDC.

A. Pulse width adjustable LD driver

The block diagram and the time chart of the PWA LD driver are shown in Fig. 3 a) and b), respectively. The PWA LD driver comprises a DLL circuit, 2 DLs, 2 multiplexers (MUX), a buffer tree, and 24 driver cells. An auxiliary Ref_clk delivers frequency reference to the DLL circuit (the principle

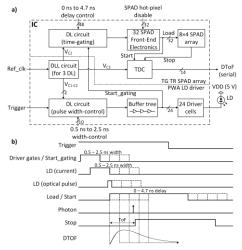


Fig. 2. a) A simplified block diagram of the designed TG-TR-DOI system with b) the timing chart.

is similar to [8, 9]) which generates control voltages (V_{C1}, V_{C2} and V_{C3}) for the 3 different delay cells (500 ps, 100 ps and 50 ps), albeit V_{C3} is only used in the TDC. The control voltages are used to stabilize the DLs delays against temperature, supply voltage and process corner variations. All DL cells are implemented with standard current-starved inverters. The trigger voltage pulse is brought to the coarse DL where the delay of the rising edge of the pulse from 500 ps to 2000 ps with a resolution of 500 ps can be selected with a MUX. A coarse delayed rising edge can be further delayed from zero to 500 ps with a resolution of 100 ps with fine DL. The other path from the trigger travels through dummy cells which are identical with the delay path components and thus produce the same offset delays. Therefore, the rising edges of the FD out and FDL out (in Fig. 3b)) can be combined to one selected pulse width-controlled pulse and delivered to the buffer tree. The start gating pulse is delivered to the TG TR SPAD array.

In order to produce ampere level current pulse for an LD, 24 properly sized switching transistors M2 in parallel are needed (DRIVER CELL in Fig. 3a)). Consequently, a branch like buffer tree must build up enough driving capability to compensate for the large input capacitance of the parallel switching transistors. When M2 transistors close simultaneously, the voltage VDD forward biases the LD. In addition, M1 transistors can be used to control the amplitude of the current pulse.

B. Time-gated time-resolved SPAD array

The block diagram and the time chart of the TG TR SPAD array are shown in Fig. 4 a) and b), respectively. The TG TR SPAD array comprises 2 DLs (bias voltage supplied by the DLL of the PWA LD driver), a MUX, 2 monostable flip-flops, 32 SPAD electronics, an 8×4 SPAD array, and a 128×14-bit counter shifter. A quench pulse (zero active quenching) is formed by the monostable flip-flop from the start gating pulse which is brought from the PWA LD driver in order to disable the quenching of SPADs. The start gating pulse is also shared to the DL 48×100 ps in order to control the start time of the gating with a resolution of 100 ps and over a dynamic range of 4.8 ns. In that case, early photons from the tissue can be avoided and the DToF measurement position can be adjusted. A load pulse for SPADs and a start signal for the TDC are formed by another monostable flip-flop from the time-gated pulse. Further, the SPADs are ready to detect the individual photons after the rising edge of the load, and the rising edge

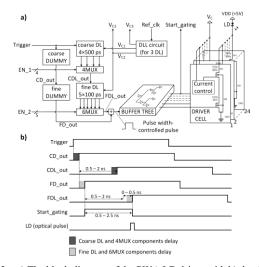


Fig. 3. a) The block diagram of the PWA LD driver with b) the timing chart.

of a start propagates in the DL 128×50 ps generating the rising edges (q1, q2 ... q128) between zero to 6.4 ns with 50 ps intervals as well. The state of the DL is stored by the detected photon to a counter register.

The block diagram of the TDC is shown in Fig. 5. The start pulse propagates through the 50ps_DL, and the one-hot code corresponding to the ToA of a photon is stored by the stop pulse to its equivalent counter_shifter by means of a stop-logic. When an appropriate amount of ToF measurements is achieved to accumulate the DtoF histogram, all counters are turned to shifters.

With the technology used in this design, the DL cell can achieve a 50 ps delay by means of pre-priming pmos P_3 , which accelerates the rising edge of the pulse of the inverter. In the proposed design, for P_3 to work efficiently, a gate forward (GF) control pulse is taken three DL cells beforehand to drive the gate of P_3 (PU in Fig. 5.). Therefore, three additional DL cells at the beginning of the DL are needed to provide a gate forwards paths for DL cells 0, 1 and 2. Every 14-bit counter can store up to 16 383 ToF measurements. Furthermore, the counters can be turned to the shifters by using 2-to-1 MUX and accordingly transfer a DtoF histogram out of the IC.

In the proposed design, to achieve fast loading of the SPADs, a switched capacitor approach has been used, as shown in Fig. 6, where the simplified schematic of the proposed front-end b) and the traditional actively loaded structure a) have been presented [10]. The 8×4 SPAD array in

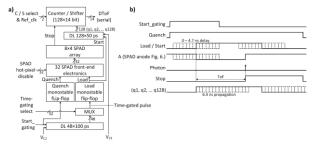


Fig. 4. The block diagram of the TG TR SPAD array with b) the timing chart.

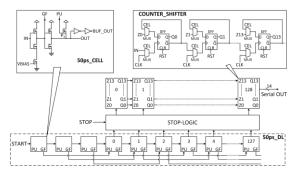


Fig. 5. The block diagram of the TDC with the counter_shifter and the 50ps_cell schematics.

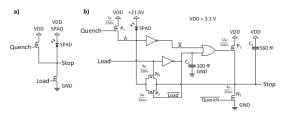


Fig. 6. The schematics of a) the traditional actively loaded structure and b) the proposed SPAD front-end electronics.

the proposed design has $3107.84~\mu m^2$ active area with 18.37% fill factor. In the traditional structure, the width of the load pulse must be very short to achieve fast time-gating because the anode node is shunted to ground during the loading pulse. However, the proposed switched-capacitor structure can be controlled by a wider loading pulse because the loading pulse is only controlling the charge sharing switch and thus the rising edge of the pulse is defining the speed of the time gating.

The proposed SPAD front-end electronics operation can be followed up in Fig. 4 b) and 6 b). At the beginning, a Quench signal is low so that an excess bias of the SPAD is zero and node A is at VDD ($V_r = 21.6 \text{ V} - 3.3 \text{ V}, V_{BR} = 18.5$ V). Moreover, the transistor N₂, which has a logical "1" at the gate, will discharge the capacitor C₁ to 0 V. After that Quenching sets MOSFET P₁ and N₂ to their cut-off region and then the rising edge of the load pulse closes the CMOS switch (N₁ and P₂) to bring node A near zero voltage by sharing the charge between node A and C1 (the load signal is kept high during the whole dynamic range of the TDC). C1 is selected to be approximately ten times larger than the parasitic capacitance at node A. Now the SPAD is biased over its breakdown voltage. Therefore, when the photon is detected by a SPAD, a breakdown occurs, making the stop signal rise. Furthermore, the rise time of the stop is boosted by pmos P₃ when the inverted node A falls. The stop signal is brought down when the quench sets N_2 back to ON-state.

III. POST-LAYOUT SIMULATIONS

The size of the layout of the proposed design is 6.11×2.35 mm² and all the simulation results shown are post-layout simulations. The LD current pulses within the width-control range of 0.5 – 2.5 ns are shown in Fig. 7. Although the shortest achievable pulse width was 300 ps, the buffer tree driving capability reduced its amplitude to 1.2 A and affected pulses shorter than 1 ns as well. Nevertheless, the rest of the pulses reached the 100 ps resolution with the average amplitude of 1.66 A. The total average power consumption of the whole IC was simulated to be 377 mW at a repetition rate of 10 MHz.

The delays of the DLs as a function of the bias voltage in worst-case scenarios are shown in Fig. 8. The DLs can achieve desired delays in all process corners and temperatures from –

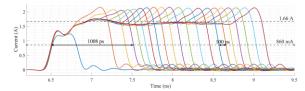


Fig. 7. The LD current pulses with 0.5-2.5 ns width-control.

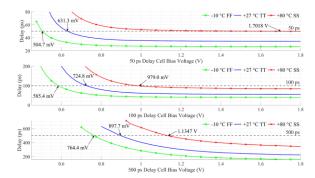


Fig. 8. The DLs worst-case scenarios.

10 °C to 80 °C. Furthermore, Monte Carlo mismatch simulation for 50 ps DL, which is presented in Fig. 9, showed the standard deviation of a delay of 1.24 ps.

In order to record the full DToF of the photons, SPADs must be loaded into the Geiger mode before the earliest photons scatter back to the detector. The start gating signal is triggering both the laser diode and the receiver (see Fig. 2 a and b)). The waveforms of LD current, Load/Start signal, the SPAD anode, Stop signal, phases of DL of TDC and the TDC counters triggered by a start gating signal are shown in Fig. 10 with an example of a photon generating a count within a specific time bin (zero time gate delay). The start pulse, generated from the load pulse, propagates in the 50 ps DL of the TDC until the stop signal transfers its position to the counter. By comparing the width of the current pulse to [8], where a quantum well LD has been driven with a similar pulse width, the delay of the optical pulse can be approximated to be 1.4 ns from the beginning of the current pulse, which gives the time when the SPADs have to be loaded to be able to detect the earliest photons from the tissue. The SPADs are loaded with the time of 121 ps (from 10% to 90%), 0.725 ns after the LD current pulse and are thus capable of detecting the early photons so that the full DToF can be collected to evaluate absorption and reduced scattering coefficients. Moreover, the Load/Start signal can be adjusted from this point to 4.8 ns at

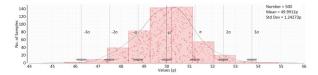


Fig. 9. The 50 ps DL Monte Carlo simulation

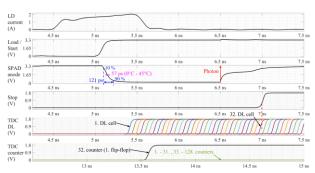


Fig. 10. The timing waveforms of the proposed design at the zero time gate delay (N.B. TDC counter has different time span).

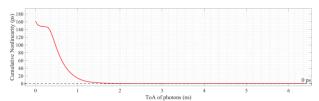


Fig. 11. The cumulative nonlinearity between the detected photons and the stop timing mark for the TDC.

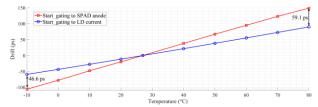


Fig. 12. The temperature drifts of the timing paths.

the 100 ps resolution to achieve fast gating to detect late photons from deeper tissue with the better SNR. The TG TR SPAD array operates with all process corners.

The nonlinearity error between start and stop signals from zero to 6.4 ns is shown in Fig. 11. The zero point corresponds to the time when the anode of the SPAD is discharged to 90% of its final value. The nonlinearity error is caused by the fact that the rise of the anode node starts from different voltage values when the difference between signals is shorter than approximately 1 ns. Temperature drifts of the LD current pulse and the load pulse measured at the anode of the SPAD when falling at the 50% level are shown in Fig. 12. The simulations showed a drift below 57 ps over the commercial product temperature range of 0 °C -45 °C. The cumulative nonlinearity can be amended in post-processing of the results, but the temperature drift must be accepted.

IV. CONCLUSION

Over the past few years, researchers have been miniaturizing TD-DOI systems. In this design, both the transmitter for LD and the receiver fabricated in a 150 nm technology were implemented on a single IC. The pulse width of the driving current can be adjusted from 0.5 ns to 2.5 ns with a resolution of 100 ps and, thus, the same pulser assorts with diverse structures of the LDs. To the authors' best knowledge, the fastest time-gating (121 ps) achieved in this work allows to reject the early photons while ensuring time to detect the more purposeful late photons efficiently. Furthermore, the measurements are merged on-chip to a DToF histogram, making the IC fast enough to be well-suited for wearable appliances.

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