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Neuromorphic thermal-electric circuits based on phase-change VO_2 thin-film memristor elements

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ABSTRACT

The basis of the powerful operation of the brain is the variability of neuron operation, i.e., it can be digital or analog, and the logic operation of a neuron-based system can be parallel and series. The challenge is to set up an artificial intelligent architecture that mimics neuro-biological architectures present in the nervous system. Our proposed new active device (phonon transistor = phonsistor) and thermal electric logic circuit (TELC) seem to be appropriate devices for neuron modeling. Key elements of the phonsistor and TELC are memristors realized by VO_2 phase change output resistors integrated with dissipating elements as inputs. These components are coupled to each other by thermal and/or electrical effects. On short distances, the information can be carried by heat diffusion and on longer distances by electrical signals. This is a similarity with human neurons where the information is carried by diffusing neurotransmitter molecules on short distances and electrically by the axons on longer distances. For example, very new ideas are presented of neuromorphic circuits for mimicking the biological neuron synapse operation and the action potential generation. Further similarities with biological neural systems are the auto-oscillation phenomenon with chaotic properties, the ability of integrating subthreshold excitations within the thermal time constant, and the memory effect of the memristive components. The TELC should be compatible with CMOS technology, as the realization of both systems utilizes conventional thin-film technology steps at similar temperature ranges. The physical appearance and construction of the TELC gate are also similar to the neuron.

I. INTRODUCTION

Phase change materials (PCMs) have recently been studied intensively for different electrical circuitry applications, for example, thermal-electric logical circuits (TELCs), THz-range programmable metamaterial sensor and modulator components, and artificial neural networks for future computation processor platforms, just to mention a few.[1–3] From this point of view, vanadium oxide (VO_2) is probably the most promising material due to its strong metal-insulator-transition (MIT) at around $T_{MIT} \approx 341$ K (68 °C). In the MIT phenomenon, VO_2 goes through a reversible first-order phase transition as a function of temperature from the high-temperature tetragonal phase to the low-temperature monoclinic phase. Above T_{MIT}, VO_2 has metallic properties with low resistivity $\rho = 10^{-3}$-$10^{-4}\,\Omega$ cm, whereas below T_{MIT}, properties are closer to those typical of semiconductors with $\rho = 10^{1}$-$10^{2}\,\Omega$ cm. Due to the relatively low transition temperature, the MIT effect can easily be triggered also by Joule heat generated by the electric current driven through the device, which makes the integration of the VO_2 based devices into complex electronic circuits a promising choice.

From the electrical circuit-engineering point of view, the most interesting property of the MIT effect is the negative differential resistance (NDR) of the order of 10^3-10^5 when the VO_2 device goes through the transition due to an increasing temperature sweep. When the VO_2 devices, most often only simple resistor elements, are connected to appropriate pull-up resistors and are biased, this functionality of the material can be measured as current gain β and transfer admittance g_m, representing exactly the corresponding properties of conventional active transistor elements.[4] When this kind of simple resistor networks are integrated together, perhaps with the present CMOS technology, they offer a totally new technological

platform for micro- and nanoelectronics integration, for example, in More-Than-Moore concept devices.

A particularly interesting property of PCM devices with the NDR effect is the auto-oscillation effect.[5] When one or more VO_2 resistors are appropriately connected with electrical or thermal energy storage, with relaxation process of characteristic time τ, i.e., capacitance C_E or C_{Th}, respectively, the circuitry starts to oscillate even though the driving energy source, i.e., voltage V_{CC} or current I_{CC}, is time independent. This makes it possible to design simple oscillating circuits, which generate various kinds of signal forms, starting from regular and uniform triangular waves, and complex multistable waveforms on the edge of the chaos, to totally irregular and essentially chaotic pseudo-random waves, depending on the selected operation set point. As it will be shown later in this paper, these oscillators can be used in neuromorphic circuits to mimic, for example, olfactory signals and spiking, single action potential waveforms, and brain waves and oscillations. Brain oscillations are characterized as waves with nonlinear dynamics and typically possess on the edge of chaos properties, such as bifurcations and multistability, for example, at the onset of a human epilepsy seizure.[6]

It is essential to point out that PCM devices, such as VO_2 resistors, with NDR and Joule heating effects, are capable of transmitting, receiving, and processing signals in both electrical and thermal energy forms simultaneously. This actually constitutes a concept of using (i) electrical signals, i.e., voltage V and current I, as well as (ii) thermal signals, i.e., temperature T and heat flow Q, as information in the same circuit at the same time in a very complex manner. This concept was first presented by Mizsei and Lappalainen in 2015.[7] When such circuits are integrated in the submicron scale, the speed of the devices is comparable to the speed of the present logical CMOS gates, and device architectures like thermal-electric logical circuits (TELCs) can be introduced.[1] However, as shown later in this paper, much larger device designs can operate at the frequency ranges of natural neural network signals, and even the electro-chemical operation of one neural synapse can be modeled and mimicked by the analog thermal-electric operation of thermally coupled VO_2 resistor circuits.

II. EXPERIMENTAL

Vanadium dioxide (VO_2) thin-film and nanostructured PCM devices studied in this paper were deposited using *in situ* pulsed laser deposition (PLD). Various single crystal substrate materials including *a*-, *c*-, *r*-plane cut sapphires and MgO with (100) orientation were used for the growth of polycrystalline and epitaxial pure single-phase VO_2 thin films. A small amount of oxygen up to 1.0×10^{-2} mbar in maximum was added into the vacuum chamber initially pumped down to a base pressure of 2.5×10^{-5} mbar for the PLD process. A Lambda-Physic Compex 201 XeCl excimer laser with a wavelength of 308 nm and pulse duration of 25 ns, pulse repetition rate of 5 Hz, and laser pulse energy density of 3 J/cm^2 on the target surface was used in the experiments. A high-purity sintered ceramic V_2O_5 pellet was used as a target. During the deposition, the substrate temperature was kept at 400 °C, and afterwards cooled down at the rate of 3.3 °C/min. After the deposition, the VO_2 thin-film samples were subjected to various structural characterization experiments in order to confirm their purity and to determine the structural properties. These results are presented in detail in our previous papers.[8]

For the electrical characterization and device structure integration and assembly, the aluminum electrodes with the thickness of 200 nm were fabricated on the top of the VO_2 thin-films using the standard photolithography process and e-beam evaporation to form the lateral device architectures. Then, the samples were wire bonded on the test-circuit boards. The wiring between the electrodes, the VO_2 thin-film area between the electrodes, together with the external discrete components, like capacitors C, formed the presented circuits used as TELC and oscillator components studied here. Thermal connection between the so-formed VO_2 resistor elements was established through the surrounding VO_2 thin film and/or the substrate. In the case of vertical device architectures, the focused ion beam (FIB) facility FEI Helios Nova 600 NanoLab was utilized in the processing. For electrical characterizations of VO_2 thin-film properties and circuit operation measurements and analysis computer controlled Memmert UFP400 low-temperature furnace, LabView controlled HP3458A multimeter and Keithley 2612 source meter, together with Tektronix TDS2004B four-channel digital storage oscilloscope, were used. External, forced cooling of the VO_2 resistor devices in TELC and oscillator circuits was also used in order to control the thermal relaxation characteristic time τ of the total circuit under the measurement during the Joule heat driven MIT processes. In such a case, a very low laminar industrial-standard purity nitrogen N_2 gas flow was directed perpendicularly to the VO_2 thin-film surface through a syringe needle. Although the experiment was not exactly controlled with respect to quantification of flow rate or type, the cooling proved that such a thermal-electric oscillator circuit can be driven in to essentially chaotic behavior in a controlled manner when NDR effect, Joule heating, and forced cooling processes are adequately synchronized. Collected data sets were analyzed, and the corresponding mathematical fitting and modeling procedures were carried out using OriginLab Pro 2016 software package.

III. RESULTS AND DISCUSSION

A. Neuromorphic features in analog operation

The electrical properties of the VO_2 thin films were first tested separately in order to determine the degree of MIT and NDR effects by heating the VO_2 resistor devices both by the furnace and by Joule heat generated by the electrical current. In Fig. 1(a), there are two typical MIT effect responses of the electrical resistivity ρ of epitaxial and polycrystalline VO_2 thin film on MgO (100) substrate presented as a function of temperature T ramping from room temperature (RT) up to 90 °C. It is obvious that both films go through a sharp MIT effect of 3-4 decades in the temperature range of 65–75 °C, which is an implication of very high quality of the VO_2 films.

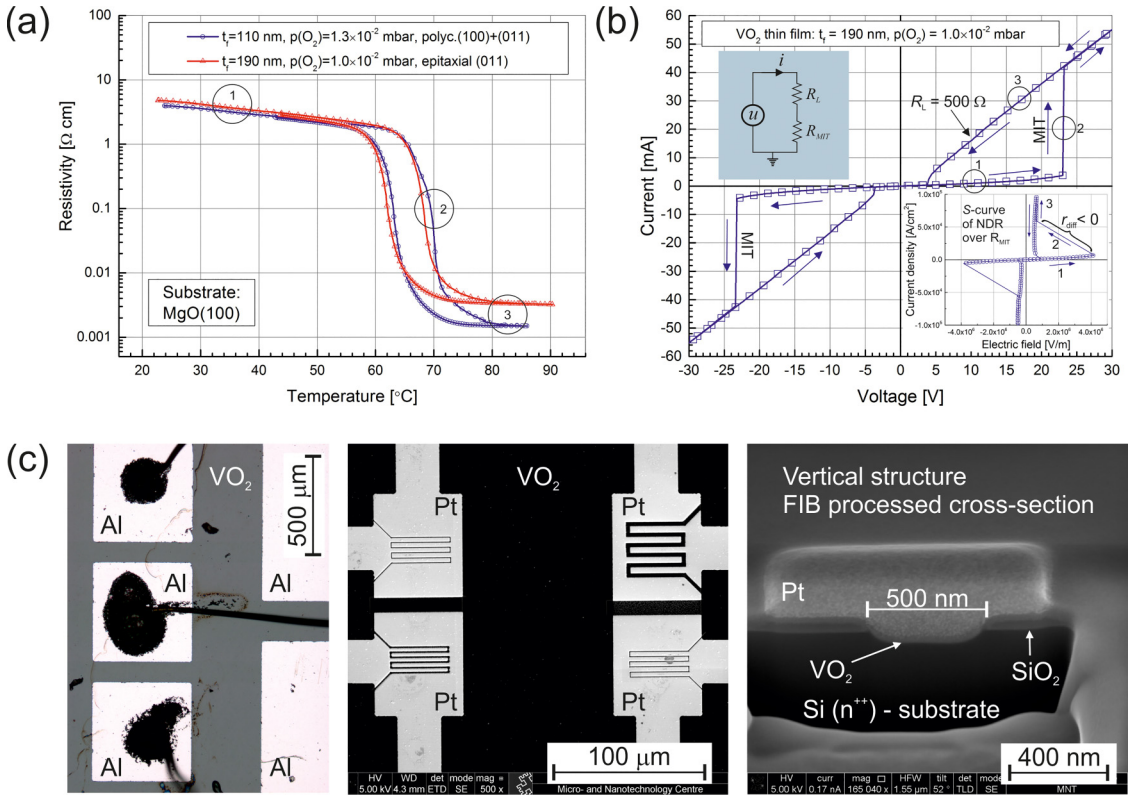

FIG. 1. Characteristics MIT effect responses of (a) two nanostructured VO_2 thin films deposited on MgO(100) substrates as a function of temperature heated in a furnace and (b) the *I-V* response of MIT effect of the other of the films in (a) when heated by Joule effect, together with corresponding measurement circuit and *S*-curve of NDR effect in the insets. (c) Optical microscope photograph of a VO_2 resistor device with the lateral electrode architecture with effective length of the resistor in the scale of hundreds of micrometers (left), and SEM micrographs of lateral architecture in the range of few micrometers (middle), and vertical structure in the scale of well below one micrometer (right).

There are three specific main states in the graphs, denoted by numbers (1), (2), and (3), in circles in Fig. 1(a), that deserve specific attention with respect to the device architectures presented later. Firstly, the device is in state (1), which is the insulator, or more precisely, the semiconductor state of VO_2 at the temperatures close to RT. Secondly, with increasing temperature, the device shifts to state (2), where the MIT effect happens and the negative differential resistance NDR is maximized. It is very important to consider here that in state (2), the parts of VO_2 resistor device are either in the low-temperature monoclinic phase or in the high-temperature tetragonal phase, or even in the middle of the phase transition between the two, simultaneously. Since the fundamental origin of first-order metal-insulator phase transition, structural or electrical, is unknown for mankind, despite several advanced theories and models, and since the different parts of VO_2 resistor device in state (2) strongly interact with each other and the external environment, the entire system is in a very complex nonlinear dynamic state of the behavior which is definitely chaotic, if not even random by its nature. Finally, with increasing temperature the device stabilizes to the high-temperature metal phase in state (3). When constructing thermo-electric VO_2 resistor devices, such as TELC gates or oscillators, in the determination of the operation point of the devices and circuits it is important to take into account, the states (1, 2, 3) or their combinations between which the utilized NDR effect actually happens.

In practical circuits, with both electrical and thermal information carrying signals, the Joule heating is certainly the simplest way to induce the MIT effect. In Fig. 1(b), there is current (I)–voltage (V) characteristic curve measured from the same VO_2 resistor device as in Fig. 1(a) epitaxial sample (red curve) using the circuit presented in the top left subset with external serial load resistance $R_L = 500\,\Omega$. Different states (1, 2, 3) are also pointed out as in Fig. 1(a). The onset of the MIT effect and NDR region is very sharp at around $V \approx \pm 23$ V, and it is also shown that the metal state with a low resistivity of VO_2 resistor device R_{MIT} stays on with decreasing voltages down to threshold values of $(V, I) \approx (4\,V, 5\,mA)$ above which the serial load resistance R_L dominates the *I-V*

response. The data shown in Figs. 1(a) and 1(b) are measured from the VO_2 resistor device structures with lateral electrode architectures shown in the left photograph of Fig. 1(c). Effective lengths of the VO_2 thin-film resistors, gray background between the bright rectangular Al electrodes with bonding wires, are in the scale of hundreds of micrometers. A more advanced integration scheme is shown in the middle of Fig. 1(c), where in a scanning electron microscope (SEM) micrograph of lateral VO_2 resistor devices is seen as black stripes processed by FIB etching through platinum (Pt) electrodes, now having effective lengths in the range of a few micrometers. Finally, a FIB processed cross section of the vertical VO_2 resistor device is roughly viewed in the right SEM micrograph of Fig. 1(c), and here the effective length of the resistor is now well below one micrometer. All the electrical data shown in this study were measured from the circuits with the layout and architecture with Al electrodes shown in the left optical microscope photograph in Fig. 1(c). In order to scale down the switching voltages by means of conventional integration techniques, the size of the proposed devices can be easily reduced down to micrometer scale, or so. In our previous study,[1] a vertical type of VO_2 resistor devices, now with platinum (Pt) electrodes, similar to the one presented in the right of Fig. 1(c), below 1 μm in every direction was developed and tested. Operation voltages could be limited even below 1 V, and of course, much shorter time constants could be achieved. Also, different geometries of lateral device architectures with Pt electrodes processed with FIB were studied, as they are shown in the middle of Fig. 1(c). Here, the electrodes were processed into the interdigitated fingers structures in order to increase the VO_2 resistor device cross-sectional area A, and thus to minimize the room temperature insulator state resistance of R_{MIT}. This, in turn, minimized the device switching voltages to the level 2-6 V.[1] However, these structures were not yet studied as oscillator circuits.

In order to see the negative differential resistance (NDR) effect of the functioning of VO_2 resistor devices presented in this study, one has to carefully study the data and the circuitry presented in Figs. 1(a) and 1(b). The top left subset of Fig. 1(b) is the schematic circuitry of the series connection of a load resistor R_L and VO_2 resistor device R_{MIT} presented against the blue background. From this circuitry, which is the typical biasing scheme of the presented circuits in this paper, one can easily obtain the expression $u_{MIT} = u[R_{MIT}/(R_L + R_{MIT})]$ for the voltage over the VO_2 resistor device R_{MIT}. Correspondingly, the expression $i = i_{MIT} = u/(R_L + R_{MIT})$ can be found for the current i in the circuit. The connection between the data in Fig. 1(a), i.e., MIT effect, and Fig. 1(b), can now be found by inserting, into the equations above, the dependence $R_{MIT}(T) = \rho(T)[l/A]$, where l and A are the length and cross-sectional area of the VO_2 resistor device R_{MIT}, respectively, and $\rho(T)$ is exactly the resistivity data shown in Fig. 1(a). When a temperature sweep from $T_1 < T_{MIT}$ to $T_2 > T_{MIT}$ is considered, from the data in Fig. 1(a) it follows that $R_{MIT}(T_2) \ll R_{MIT}(T_1)$, and thus $u_{MIT}(T_2) \ll u_{MIT}(T_1)$, and $i_{MIT}(T_2) \gg i_{MIT}(T_1)$. By definition, the negative differential resistance NDR is $r_{diff} = du/di < 0$, and thus $r_{diff} = [u_{MIT}(T_2) - u_{MIT}(T_1)]/[i_{MIT}(T_2) - i_{MIT}(T_1)] < 0$ practically for all realistic values of R_L. The value calculated using actual data from S-curve of NDR shown in the inset of Fig. 1(b), and exact component geometry, is $r_{diff} = -1356.26\ \Omega$.

The existence of NDR in VO_2 resistor devices R_{MIT} is also evident from the graph in the bottom right subset of Fig. 1(b), where a typical S-curve of the current controlled NDR can be seen, in the case of the same sample as in Fig. 1(a), where the film thickness $t_f = 190$ nm.[9] This S-curve was calculated only using the data of the Joule heat generated MIT effect in Fig. 1(b) by calculating only the contribution of VO_2 resistor devices R_{MIT} (u_{MIT}, i_{MIT}), and renormalizing the result along the component geometry parameters (l, A). So, to obtain this clear evidence of NDR in VO_2 resistor devices, the data presented in Fig. 1(a) were not used, even though both ways of calculation lead to the same result, obviously. For the sake of clarity, it is still useful to notice, that when looking at the data of the Joule heat generated MIT effect in Fig. 1(b), the current limiting property of R_L in that case, which does not exhibit NDR or MIT effect, is dominating the response when $T > T_{MIT}$, and the axis in the graph $(x, y) = (u, i)$, especially because u is the applied source voltage.

As it was already mentioned, the thermo-electric logic circuits (TELCs) can process both electrical and thermal forms of energy as information signals.[1,4] This concept can be extended further, beyond logic switching operation of the VO_2 resistor devices, for example, to mimic the biological neuron synapse structure and operation, as shown in Fig. 2. A typical TELC cell structure, such as the circuit schematically described in Fig. 2(a), can be divided into three sections including Electric node 1, Thermal node, and Electric node 2. Electric nodes include the two VO_2 resistor devices r_1 and r_2, or just normal heating resistors r_h, or both, for generation of electrical MIT and NDR effects and heat in r_1, and for detecting the heat and temperature using the same effects in r_2, for example. Between the components r_1 and r_2, there is the Thermal node, where the information is transferred as a heat flow. This structure constitutes a neuromorphic circuit highly analogous with the interconnection between two biological neuron structures shown in Fig. 2(b). Between the two connecting neurons, there exists a synapse, where basically electrical neuro pulses are transferred in chemical energy form carried by neurotransmitters. The interconnection between two neurons can be thus divided into three parts including Electric node 1, Chemical node, and Electric node 2, corresponding Axon, Synapse, and Dendrite, respectively. Thus, the Thermal node of the TELC in Fig. 2(a) corresponds to the Chemical node of neuron synapse in Fig. 2(b), and the transfer function of information can be expressed by the analogy between the thermal heat flow F_Q and the chemical flux F_C, as in the following equation:

$$F_Q = -\kappa \frac{dT}{dx} \propto F_C = -D \frac{dC}{dx}, \tag{1}$$

where κ is the heat conductivity and dT/dx is the temperature gradient between the VO_2 resistor devices r_1 and r_2 in

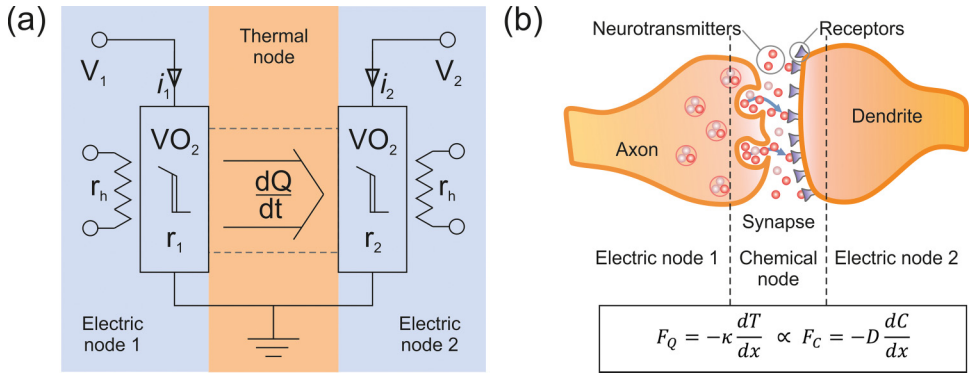

FIG. 2. (a) Typical basic TELC cell structure and schematic circuit diagram of the three sections compared with the analog to (b) interconnection between two biological neuron structures.

the TELC in Fig. 2(a), and D is the diffusion coefficient, and dC/dx is the chemical concentration gradient in synapse, as shown in Fig. 2(b). This analogy between heat conductivity κ and chemical diffusion coefficients D is actually quite familiar from the theory of energy transducers and sensors, but here it was also implemented in the neuromorphic TELC.[10]

When nonlinear relaxation processes with characteristic times τ_i are included in a system having active amplification and feedback properties, auto- or self-oscillations can occur although all the forms of energy imported into the system are essentially time independent. Taking into account that the nonlinear relaxation mechanisms can be either electrical or thermal in nature, a thermo-electric logic circuit (TELC) cell, such as the one presented in Fig. 2(a), is a potential VO_2 resistor device circuit to perform auto-oscillations.

It is a well-known fact that some of the phenomena in these prototype circuits, including thermal conduction $dT(\mathbf{r},t)/d(\mathbf{r},t)$, charging and discharging of electric capacitances C, and the MIT effect itself, are all very strongly nonlinear complex processes. For example, a thermo-electric logic circuit (TELC) cell, such as the one presented in Fig. 2(a), is composed of three different sections of Electric node 1, Thermal node, and Electric node 2, as described above, having three different thermal characteristic times $\tau_{1...3}$, one for each section, respectively. Since the VO_2 resistor devices in such a TELC cell do not really need to be identical, both r_1 and r_2, and also the thermal node between them, are described, each one separately, by the general heat equation $\partial T(r, t)/\partial t = [\kappa/(c\rho)]^2 \times \nabla^2 T(r, t)$, where $\boldsymbol{r} = (x, y, z)$ are the position coordinates, c is the specific heat capacity, and ρ is the density of the matter for each section.[11] This is, of course, due to the fact that both r_1 and r_2 have their own Joule heat generation processes, as well as has the thermal node, which can be tailored with specific materials and geometries to meet the designed thermal conduction properties. Furthermore, when an electrical capacitance C is added parallel to VO_2 resistor device, as in Fig. 3(a), and later in Figs. 4(a) and 4(e), yet another differential equation has to be considered when the operation of the circuitry is described. Since the TELC output signal is typically voltage $v(t)$, the nonlinear effect of capacitance C can be described by the general equation $C = dQ/dV = d[\int i(t)dt]/dV$, where $i(t)$ is the charging current.[12] Now the self-oscillation effect becomes also very clear, for example, when a circuit presented in Fig. 3(a) is considered. When voltage V_{cc} is switched on, the current through external resistor R_1 starts to charge up capacitor C, and output voltage v_2 increases, as long as the Joule heat generation is low enough to keep VO_2 resistor device r_2 in the insulator state. After the MIT effect in r_2, capacitance C is discharged through it, and v_2 drops down. Finally, the current is not anymore high enough to keep r_2 in the metal state, it flips back to the insulator state, and the cycle starts all over again. However, the most important point above is that the TELC system operation is always described by a set of, at least three, first or second order differential equations, which behavior is by the definition nonlinear in real space (x, y, z, t).[11] This also proves that such a system can evidently have chaotic operation points, as it is experimentally observed later in this paper. Even though the properties of such systems are simulated numerically by us and the other groups, it is hardly necessary go through those results in this paper, which is a presentation of the novel ideas and functionalities of the prototype circuits to be utilized in neuromorphic applications.[3–5,8]

Indeed, in Fig. 3(a), there is a circuit having two VO_2 resistor devices with thermal signal connection presented, analogous to the configuration in Fig. 2(a), but now also equipped with pull-up resistor R_1 and an external electrical capacitive circuit with time constant $\tau \approx R_2C$. The right hand side of the circuit actually resembles very closely the circuit studied by Kumar *et al.*;[5] however, in this case, the circuit is composed of lateral electrode architecture VO_2 resistor devices, as shown in the top left corner subset, and in the left part in Fig. 1(c) with effective resistor lengths in the scale of hundreds of micrometers. When this circuit is driven with the parameters $V_1 = 12$ V, $V_{CC} = 42$ V, $C = 10\,000\,\mu$F,

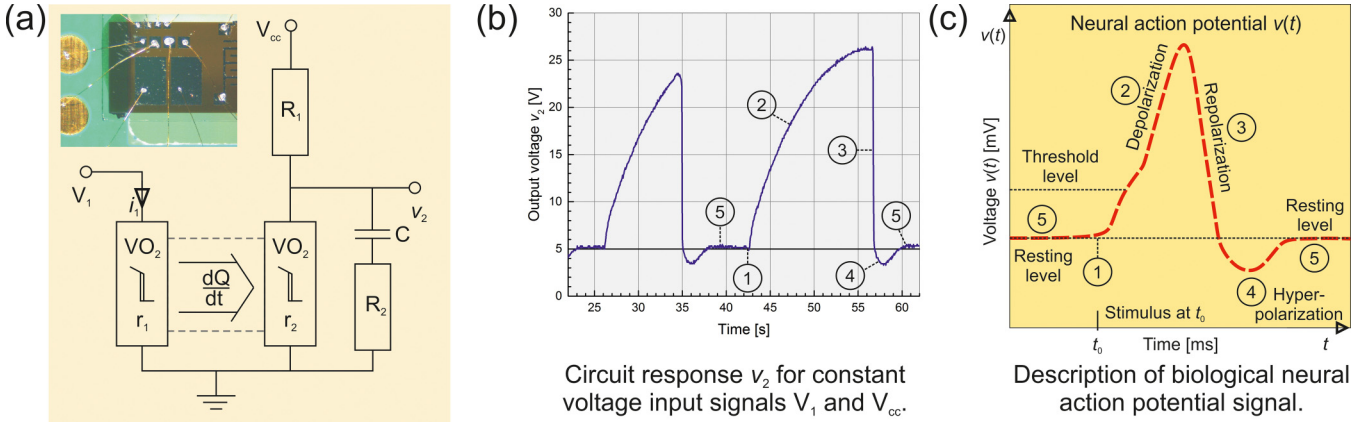

FIG. 3. (a) A schematic diagram of a VO_2 resistor device circuit with a top-view photograph in upper left inset, (b) self-oscillating with waveform mimicking, and (c) the biological action potential signal.

$R_1 = 1\,k\Omega$, and $R_2 = 100\,\Omega$, without any forced external cooling, it can be set to the operation point where the oscillations actually mimic the biological action potential signal, as depicted in Figs. 3(b) and 3(c), although the time scale is not comparable. However, this should only be a device-scaling problem, as suggested, for example, by Velichko *et al.*[3] It is especially important to note that the circuitry in Fig. 3(a) performs even the hyperpolarization state of the biological action potential, mostly due to complex interaction of the heat fluxes generated by r_1 and r_2, and biasing resistor R_2. Despite the complex waveform, in this case, the VO_2 resistor device r_2 is actually oscillating between the insulator state (1) and metal state (3), as is described in Fig. 1(a), and regular continuous oscillation is generated. Of course, in this case, the VO_2 resistor device r_1 could also be replaced by an appropriate heating resistor r_h, as described in Fig. 2(a). The generated waveform represents much of what is generated, for example, by the conventional unijunction transistor NDR circuits.[9] This time much more simplified circuitry is created by means of the VO_2 resistor device, which performs MIT and NDR effects. Also, more complex features of the waveform are created, like the hyperpolarization state.

By arranging the circuit components, namely, VO_2 resistor devices r_1 and/or r_2 differently, driving the circuit into different operation points by varying the circuit parameters, such as V_1, V_{CC}, C, R_1, and R_2, and using external forced cooling to increase the complexity of the nonlinear thermal conduction process, it is possible to generate irregular, even chaotic and pseudo-random signal waveforms. This kind of signal generators can be utilized in neural network computation problem solving, in non-Boolean computing, in encryption procedures of cryptography, and certainly in neuromorphic circuits.[5,13,14] In Fig. 4, there are three different kinds of waveforms in (b), (f), and (j), their amplitude distribution functions (ADFs) in (c), (g), and (k), and their phase space analysis (PSA) and Fourier transformation (FFT) graphs in (d), (h), and (l) presented, respectively. The waveform in (b) was generated by the VO_2 resistor device circuit in (a), similar to the circuit in Fig. 3(a), but now under forced cooling, and the waveforms in (f) and (j) were generated by the circuit in (e) without and with the forced cooling, respectively. It is important to notice here that the circuit presented in Fig. 4(e) has only one VO_2 resistor device r_1 and a directly shunting capacitor C connected parallel to it.

When a system capable of chaotic behavior starts to divert from its stable ground state, it typically goes through a process where the number of characteristic states of the system is doubled as the operation point is slightly changed, and very quickly, the system falls in the state of extremely complex combination of the states, which is called chaos. The doubling of the states is called bifurcation, and from the neural network computation, and neuromorphic applications point of view, for example, the most interesting area is the operation points where the first bifurcations take place at the edge of the chaos. In Fig. 4(i), there is the conventional bifurcation diagram of the logistic function presented as a function of parameter k, and the first two bifurcations are presented in detail.[15]

If one considers the oscillator circuits in Figs. 4(a) and 4(e) to be in the ground state, no self-oscillations should appear, and the state of the circuits would be described by the solid line, and the operation point by the parameter $k < k_1$ in Fig. 4(i). However, when the operation point is shifted a little bit so that the parameter $k_2(3.45) > k > k_1(3.0)$, the first bifurcation process happens, the system now shows two characteristic states, and the VO_2 resistor device TELC in Fig. 4(a) starts to oscillate between the two states generating the waveform shown in Fig. 4(b).[15] Here, the circuit is driven with the parameters $V_1 = 15\,V$, $V_{CC} = 30\,V$, $C = 10\,000\,\mu F$, $R_1 = 10\,\Omega$, and $R_2 = 80\,\Omega$, with forced cooling. The oscillation waveform is actually triangular at a frequency of $f = 0.75\,Hz$, and its ADF, shown in Fig. 4(c), is reasonably evenly distributed, but still pointing out

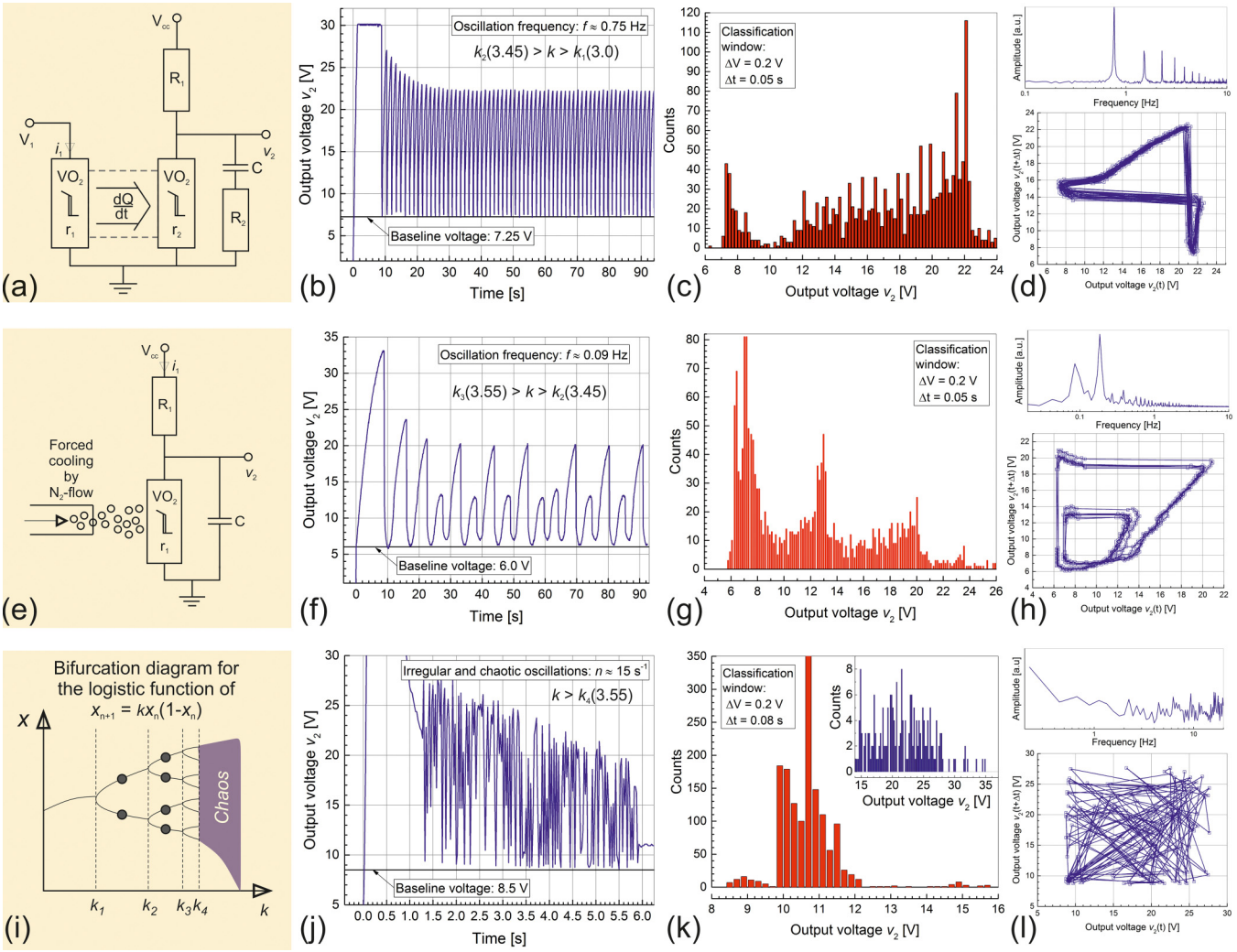

FIG. 4. Schematic circuit diagrams [(a) and (e)] of the two VO_2 resistor device circuits driven to different operation points showing three different oscillation output waveforms (b,) (f), and (j) that were characterized by using ADF data [(c), (g), and (k)], PSA maps, and FFT graphs (d), (h), and (l), respectively. (i) Conventional bifurcation diagram of logistic function used to explain the observed chaotic behavior of the circuits.

the two main states $v_2 \approx 7.25$ and 22 V. The PSA data in Fig. 4(d), where the concurrency of the generated waveforms as a function of time is presented as a graph $(x, y) = [v_2(t), v_2(t + \Delta t)]$, show a very clear two-loop attractor, which implements regular oscillations with uniform waveforms of the signal.[16] FFT analysis data in the upper part of Fig. 4(d) also confirm discrete frequencies of the oscillations. This circuit is also oscillating between the insulator state (1) and the metal state (3), as is described in Fig. 1(a).

When a single VO_2 resistor device presented in Fig. 4(e) is driven with parameters $V_{CC} = 64$ V, $C = 10\,000\,\mu$F, and $R_1 = 1\,k\Omega$, without forced cooling, an interesting twofold oscillation state at very low frequencies of $f = 0.09$ Hz is found. Obviously, the operation point is now shifted even more so that parameter $k_3(3.55) > k > k_2(3.45)$, the second bifurcation process has happened, and the system now shows four characteristic states on the edge of chaos, as is also shown by the four points in Fig. 4(i). In addition, the ADF in Fig. 4(g) shows the four main states of around $v_2 \approx 6.5$, 7.25, 13, and 20 V, and the PSA graph and FFT pattern in Fig. 4(h) confirm further the regular oscillations with uniform waveforms of the signal, however, now in a complex multiple-state oscillation operation point. Apparently, the circuit is now oscillating between the insulator state (1) and the metal state (3), but has also two other states closer to state (2), as is described in Fig. 1(a).

Finally, the operation point is pushed further away so that now parameter $k > k_4(3.55)$ in Fig. 4(i), huge amount of bifurcations has happened, and the system has fallen into chaos, and the VO_2 resistor device TELC in Fig. 4(e) generates extremely irregular random-like 5 s long bursts of oscillations, and then stabilizes to background voltage. Although this oscillation mode is not continuous in time, it can be started over and over again by resetting and cooling the circuit down to RT, and starting the sequence again by using circuit parameters $V_{CC} = 60$ V, $C = 47\,\mu$F, and $R_1 = 1\,k\Omega$, with forced cooling. Inside the oscillation burst, the signal shows strong chaotic and random properties, as is proven by the ADF data in Fig. 4(k) and the PSA graph and FFT pattern in Fig. 4(l). For both chaotic and essentially random signals, the PSA data should really look like the one in Fig. 4(l) with all data points scattered evenly inside a rectangular area in $[v_2(t), v_2(t + \Delta t)]$ map, and FFT pattern showing no preferred oscillation frequencies. However, the strongly asymmetric ADF data in Fig. 4(k) support the chaotic oscillation assumption, since the distribution of real random oscillation should be uniform and symmetric in nature. Thus, it is concluded that the oscillations shown in Fig. 4(j) are originating from a nonlinear dynamic VO_2 resistor device circuit with the operation point deep in chaos, oscillating all the time close state (2) shown in Fig. 1(a). With careful modeling and design, it should be a straightforward task to find the device structure and circuit parameters to set the oscillator in the continuous chaotic state.

When the significance of the presented results of neuromorphic circuits and neural networks for promising applications is considered, several points of view of implementation can be presented. First, the elementary TELC cell analogs to and mimicking the biological neuron synapse structure and operation can be used in the construction of information transmission lines similar to connections between single cells in neural networks. This has been presented in more detail below and is a novel idea in this manuscript due to exploitation also of heat as an information carrier signal. Otherwise, similar synaptic behavior have been proposed using purely non-volatile resistive switching memristor devices, such as Ti/ZnO/Pt thin-film structures, to emulate synaptic behavior, for example, by Pan *et al.*[17] Neural network applications of oscillator circuits are also severe. Presented oscillator circuits in Figs. 3 and 4, even those with chaotic responses, can be utilised as coupled van der Pol oscillators with memristive interconnection. These simple circuits could replace the programmable unijunction transistors in circuit presented by Ignatov *et al.*, and furthermore, the memristive coupling memory could be constructed of a VO_2 resistor device.[18] This kind of oscillator circuits with mutual coupling in complex geometries can be used for studying and mimicking, for example, Hebbian learning processes, the effects of synchronization for memory, etc. in biological neural networks. Adeli and Ghosh-Dastidar have also discussed how in EEG-based diagnosis of neurological disorders, such as epilepsy, the brain wave oscillations start to represent anomalies similar to those generated by TELC based oscillators in Figs. 4(b), 4(f), and 4(j).[15] By connecting a large group of such oscillators into the form of biological neural network, introducing externally local temperature effects, etc. into the system mimicking chemical effects, perhaps, such a kind of anomalies could be studied and modeled. Still, it is important to point out the excellent work by Kumar *et al.*, where they have studied similar chaotic oscillations and utilized another phase change material, namely, NbO_2, to construct chaotic artificial neural Hopfield networks for computational decision-making applications.[5] Such neural networks can also be realized with integrated TELC structure based oscillators presented in this study in Figs. 3 and 4.

When considering all the prototype circuits based on VO_2 resistor devices presented above, they are quite large, even though based on thin films of thickness below 200 nm. As a consequence, the operation voltages and the external capacitor and resistor values are high, and therefore impractical to be used in integrated devices. However, these laboratory experiments reported in this paper have proved the new ideas and functionalities that these kinds of device are offering and capable of performing. It is evident that by means of conventional integration techniques the size of the proposed devices can be easily reduced down to micrometer scale, or so. In our previous study,[1] a vertical type of VO_2 resistor devices below 1μm in every direction was developed and tested. Operation voltages could be limited even below 1V, and of course, much shorter time constants could be achieved. The integration of the external resistor elements should also be quite a straightforward task to accomplish,[3] although the integration of the capacitances is a well-known challenge, and most likely, some discrete external capacitors should still be used, however, now with much smaller nominal values in surface mount device (SMD) format. In the other previous work,[7] we have also considered the heat transfer and management controlling issues. The heat sink and barrier layers, e.g., thin film metallization or SiO_2 dwells, respectively, are envisaged for use in a three-dimensional (3D) manner around and between the VO_2 resistor devices. For even more complex integration schemes, the modern multichip-module (MCM) and system-on-package (SOP) technologies can be used, such as low-temperature-cofired-ceramics (LTCC) and 3D-silicon fabrication methods, to fabricate integration schemes including even gas and liquid flowing channels.

B. Neuromorphic features in Boolean operation

The simplest thermal electric gate (TELC inverter) consists of a phonsistor and a pull-up resistor. The pull-up resistor may serve as the thermal input of the next gate. That kind of TELCs (NAND, NOR gates) is introduced in Ref. 7, along with the measured results.

A concept for a slightly more difficult thermal-electric logic circuit (TELC) is shown in Fig. 5 with power supply voltage (V_{cc}) and pull up resistors. This four input (A, B, C, D) complex gate realizes an AND function considering the A and D inputs, as their input resistors are far from the VO_2 based output resistor, while either of the B and C input resistors can

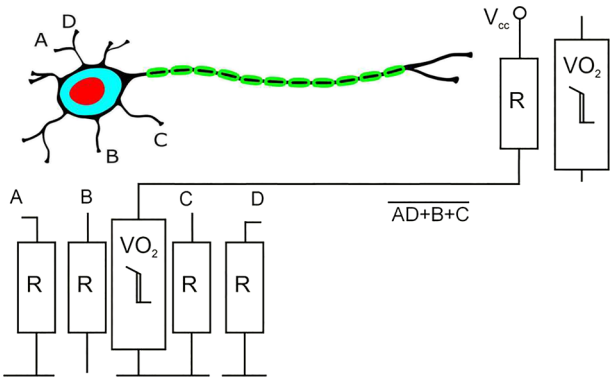

FIG. 5. A complex thermal-electric logic gate (inverted AND-OR) demonstrating the neuromorphic structure and operation. Note the pull-up resistor as input resistor of the next gate, and the resistor at the node B, which is the pull-up resistor of the previous gate.

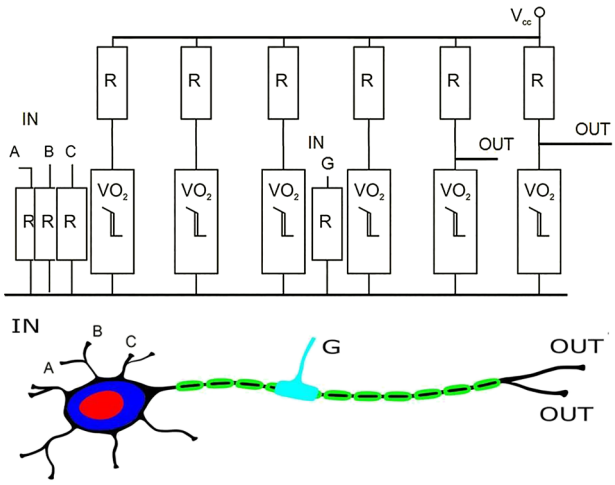

FIG. 6. Schematic picture of the neuron with glia contact and the thermal transmission line with three inputs (A, B, C "dendrites"). An additional excitation is possible somewhere in the inside of the system (G, "glia cell"), and there are two outputs ("synaptic terminals").

switch on the output, as they are next to the output resistor. Finally, the realized logic function is AD + B + C considering the thermal signal output, and opposite at the electrical output (see Fig. 5). Input resistors could be either grounded or connected to the V_{cc} power supply voltage, because a TELC gate pull up resistor may act as an input resistor ("dendrite") of the next stage, as shown in Fig. 5. By calculating the total number of components in a TELC system, one can conclude that it is the sum of the total number of logic inputs and the number of TELC gates: every TELC gate contains at least one VO_2 resistor switch and as many heating resistors as the number of logic inputs.

The neuromorphic structure and operation of the TELC is demonstrated in the same figure. Information propagates for shorter distances in the neuron by means of chemical diffusion of molecules, while the long axon transfers the electrical signal on larger distances, just like to the TELC, where information transfer is based on thermal diffusion for short distances, and on electric connection for longer distances. Information can be transferred directly by thermal diffusion also from one VO_2 resistor to another, thus a thermal transmission line can be built based on VO_2 resistors next to each other (Fig. 6).

Either of the A, B, or C input excitations can heat up and switch on the thermally sensitive (VO_2) resistor next to them. This "switched on" state propagates among the chain of the thermally coupled MIT resistors, thus the whole system acts as a transmission line. Further logic input could be coupled thermally to any stage of the thermal transmission line (see input G). A glia cell may have a similar effect on the long axon of the neuron. Experimental results from the thermal transmission line have been recently published in Ref. 19.

Artificial and natural intelligence has been discussed by Von Neumann.[20] He concluded that the basis of the enormous brain efficiency is the ability of analog, digital, parallel, and series operation of neurons, respectively. Analog operation means that higher excitation results in higher response, digital operation means that certain combinations of excitations result in response, sequential operation means that two (or more) subthreshold excitations within recovery time on the same input line result in response, while parallel operation means that certain combinations of excitations on a group of inputs result in response.

The above listed features are more or less valid for the phonsistor based TELC system too. It is basically a digital and parallel logic structure,[7] but the phonsistor can also be considered as an analog device (see the previous paragraph, as well as the measured thyristor-like input and output characteristics[1,4]). However, two or more subthreshold excitations within the thermal time constant on the same input of a TELC gate may result in switch on, i.e., sequential AND operation, similarly to the effect of subthreshold stimuli on neuron within recovery time.

IV. CONCLUSION

Nanostructured thermal-electric VO_2 resistor thin-film device circuits, utilizing both electrical and thermal energy forms as information signals, were fabricated for neuromorphic systems to be used in applications such as neural network computation problem solving, in non-Boolean computing, and in encryption procedures of cryptography. An elementary thermal electric logic circuit (TELC) was shown to mimic closely the operation of the interconnection of synapses between the neurons. On the other hand, various self-oscillating circuits were presented, which generate, for example, neural action potential signals, regular periodic oscillations, on the edge of the chaos waveforms, and pure chaotic waveforms. The neuromorphic feature appears in the

Boolean operation too, as both the schematic operation and the schematic structure of the TELC gate are somewhat similar to the neuron.

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