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Nanohole Structuring for Improved Performance of Hydrogenated Amorphous Silicon Photovoltaics

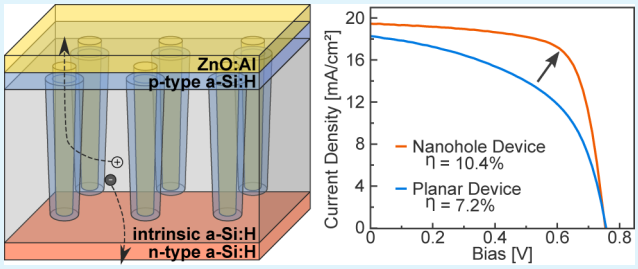
Eric Johlin,*[,†,§] Ahmed Al-Obeidi,[†] Gizem Nogay,[‡] Michael Stuckelberger,[‡,∥] Tonio Buonassisi,*[,†] and Jeffrey C. Grossman*[,†]

[†]Massachusetts Institute of Technology, Cambridge, Massachusetts 02139, United States

[‡]École Polytechnique Fédérale de Lausanne, CH-1015 Lausanne, Switzerland

Supporting Information

ABSTRACT: While low hole mobilities limit the current collection and efficiency of hydrogenated amorphous silicon (a-Si:H) photovoltaic devices, attempts to improve mobility of the material directly have stagnated. Herein, we explore a method of utilizing nanostructuring of a-Si:H devices to allow for improved hole collection in thick absorber layers. This is achieved by etching an array of 150 nm diameter holes into intrinsic a-Si:H and then coating the structured material with p-type a-Si:H and a conformal zinc oxide transparent conducting layer. The inclusion of these nanoholes yields relative power conversion efficiency (PCE) increases of ∼45%, from 7.2 to 10.4% PCE for small area devices. Comparisons of optical properties, time-of-flight mobility measurements, and internal quantum efficiency spectra indicate this efficiency is indeed likely occurring from an improved collection pathway provided by the nanostructuring of the devices. Finally, we estimate that through modest optimizations of the design and fabrication, PCEs of beyond 13% should be obtainable for similar devices.



KEYWORDS: *nanohole, photovoltaics, nanostructuring, amorphous silicon, thin-film solar cells, charge collection, efficiency*

INTRODUCTION

It is known that the low hole mobility (due mainly to the extended band-tail states) in hydrogenated amorphous silicon (a-Si:H) prevents effective hole transport and thus limits current collection in these photovoltaic devices.[1,2] The practical implications of this, other than limiting the efficiency of a-Si:H photovoltaics, is that the devices are made much thinner than would absorb the majority of the available (above-band gap) solar illumination.[3] The high number of previous studies into the optimization of a-Si:H devices,[4−6] coupled with recent improvements in understanding of the innate limitations to transport in the currently possible materials,[7] makes the further improvement of the bulk material especially challenging. However, we herein demonstrate the ability of nanostructuring to utilize the advantageous properties of the material, namely, the strong optical absorption as well as the low surface recombination,[8] critical for maintaining performance of nanostructured devices,[9] to counteract this inherently low bulk mobility and achieve a significant improvement in hole extraction (effective mobility) in photovoltaic devices.

The previous work on nanostructuring of amorphous silicon (as well as other forms of silicon) can be summarized in two categories:

The first method's aim is to improve device efficiency by improving photon absorption, either through bulk absorption increases (e.g., front-side texturing allowing a longer interaction path length and/or decreased reflection,[10−17] particularly with nonnormal incident illumination,[18,19] or back-side scattering or reflectors causing multiple interactions with the absorption path[20−23]) or by increasing absorption near the surface (e.g., surface-plasmon enhancement[24,25] or shallow structures exhibiting enhanced optical resonance[26,27]).

The second category focuses on improving carrier extraction from devices. This is mainly realized in the form of radially structured nanowire/-rod/-cone devices, but most have employed crystalline silicon in order to produce these structures. This can either be done by etching bulk silicon materials away, which still requires relatively high-efficiency (and expensive) bulk c-Si wafers,[28,29] or by vapor−liquid−solid (VLS) growth, where metals are used to incorporate adsorbed and then dissolved silicon atoms into an advancing solid wire structure. These latter methods, however, have suffered from very low efficiencies, usually less than a percent for reasonable device structures,[30,31] or rely on processing of single wires for higher efficiencies.[32] Furthermore, such methods often require numerous processing steps, commonly involving gold for either the VLS growth or for metal-induced etching, and thus decreasing the feasibility of production due to cost and complexity and increasing impurity contamination. Recently progress has also been made in a novel plasma-assisted VLS

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process, allowing deposition of up to 8.1% efficient a-Si:H on c-Si nanowire devices,[33,34] but as with all nanowire-based designs, these materials would also require substantial additional encapsulation on the cell-level to prevent damage to the nanowire structures in most actual device deployments.

In this work we propose a combination of the two approaches discussed above, using ordered arrays of nanoholes etched into thick (1000+ nm) intrinsic amorphous silicon bulk layers, followed by the filling with higher mobility materials, we work to improve hole extraction from the devices through either reduced transport path lengths, increased electric field gradients, or both. This approach can also allow for increases in absorption (due to decreased reflection and increased scattering) as well as concentrated surface absorption (through optical trapping in the regions between the holes), hopefully further compounding the benefits of this approach. Finally, because the inclusion of nanoholes into bulk films should not hinder their structural properties significantly (especially when filled), there should be no need for additional processing or encapsulation steps to ensure the devices are mechanically robust and compatible with traditional encapsulation.

We begin by proposing three different classes of nanohole structured thin-film device architectures, as depicted in Figure 1a–c. The main novelty here is the inclusion of a higher-mobility layer (non-a-Si:H p-type material or transparent conductor) to allow significantly improved extraction of holes from thick devices, while maintaining a overall planar geometry, thereby allowing the use of previously optimized deposition processes.

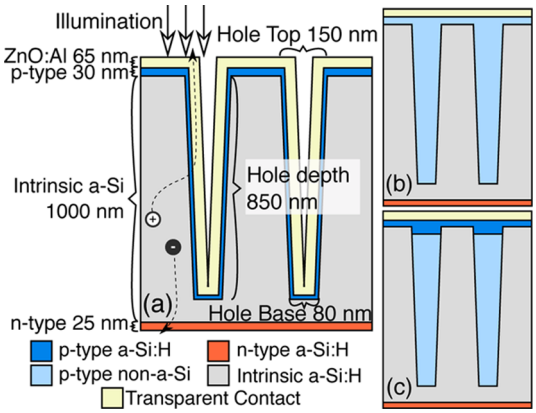

Figure 1. Cross-sectional schematics of three proposed nanohole structured a-Si:H device architectures, with part a representing the experimentally investigated homojunction design (with electron and hole transit pathways), and with the material types indicated at the bottom. Part b represents an alternative heterojunction design, with high mobility (non-a-Si:H) material filling the nanoholes, while part c represents a hybrid design using both high mobility filling material and a doped a-Si:H top layer.

The device in part a represents the most analogous device to planar and nanowire homojunction cells, with a p-type a-Si:H material coating the walls of the device and a transparent conducting material (e.g., a transparent conducting oxide [TCO] or metallic carbon nanomaterial) coating the hole surface. This would ideally operate by shifting the transport direction from through the device, toward the closest hole, thereby reducing the a-Si:H transit length.

The device in part b uses a higher mobility p-type material (e.g., PEDOT:PSS or Cu_2O) to create a heterojunction cell but without the need for permeation of the top conducting layer into the hole. This would operate by separating holes into the p-type material and leveraging the improved transport in this region to move the holes majority of the distance to the front contact. If the transport length in the p-type material were long enough (PEDOT:PSS has reached similar conductivities as indium–tin-oxide [a common TCO material] recently[35]), the front transparent contact could optionally be replaced by a simple sparse metal grid, as in c-Si devices.

The device in part c represents hybrid approaches, where carriers are transitioned from the intrinsic region, to the lightly doped p-type heterojunction material and then back into a thin layer of more heavily doped p-type a-Si:H layer. These orientations are designed to help in two regards, first, to improve depletion of the intrinsic layer by the extraction of additional free carriers into the heavily doped p-type amorphous silicon layer, and second, to provide additional field to direct carriers either more strongly toward the front contacts (shown) or toward the hole surfaces (selectively through the hole interior using a dual-layer coating).

In this work we focus on the first of the devices proposed in Figure 1a, the nanohole amorphous silicon (referred to simply as nha-Si:H) homojunction cell filled with a high-conductivity, transparent top contact layer. This choice is mainly due to the fact that the similarity to traditional planar a-Si:H homojunction devices both allows direct experimental comparison of the benefits of the nanohole structuring as well as permits simple estimates of the benefits of this structuring (see the Supporting Information, Figure S1).

The validation of the design takes place in two parts, first with a series of low efficiency "test devices" used as a proof of concept platform to determine the validity of the approach and explore the improvement mechanisms, and a second round of high-efficiency devices, used to confirm the applicability to near-record performance materials.

RESULTS AND DISCUSSION

Test Device Fabrication. Initial test devices are fabricated from *n-i* layer stacks, with a 1000 nm thick intrinsic a-Si:H bulk layer. Interference lithography is utilized for patterning of the 150 nm holes in a square array at a 300 nm pitch, seen in Figure 2a, with inductively coupled plasma reactive ion etching (ICP-RIE) used to create the 850 nm deep holes, as shown in Figure 2b,c. After fabrication of the nanohole structures, the holes are coated to form the final device structure, represented in Figure 1a, by deposition of the p-type a-Si:H layer and ZnO:Al combination TCO and antireflection coating (ARC). A final device is shown in both cross section and top view in parts c and e of Figure 2, respectively. Details of the deposition process are present below in the Methods section.

Test Device Optical Characterizations. To begin characterizing the fabricated devices, we first perform optical measurements of the planar and nha-Si:H materials after etching and mask removal, both before the doped layer and ZnO:Al coating, as well as after completing the full device stack. Modifying the deposition to be performed on quartz substrates, we acquire UV–vis absorbance data through the combination of reflectance and transmittance traces. Planar and nha-Si:H samples are fabricated identically with 1000 nm thick intrinsic layers, and in the nha-Si:H devices, an etch depth of ~850 nm for the nanoholes.

In Figure 3a,b, we see that the absorptance of the uncoated (no ARC) nanohole structures is substantially higher than that

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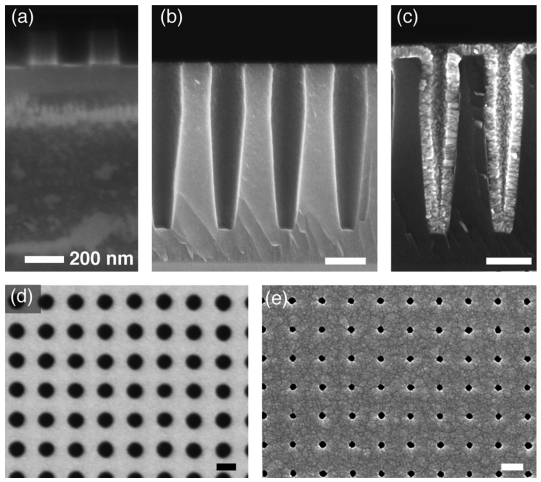

Figure 2. Scanning electron micrographs of the nanohole device fabrication process: (a) cross-section of SiO_2 mask layer, (b,d) cross-section and top-view, respectively, of the a-Si layer after etching, and (c,e) similarly after coating with ZnO:Al.

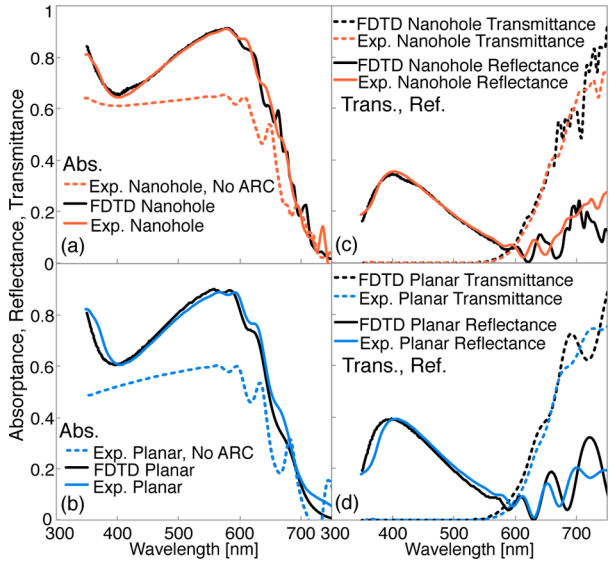

Figure 3. Comparison of absorptance profiles for planar and nanohole structures (a,b), before ZnO:Al coating and full devices, along with transmittance and reflectance (c,d) for full planar and nanohole devices compared to FDTD simulations.

but is actually benefiting from some constructive resonance within the a-Si:H surrounding material.

Furthermore, finite-difference time-domain (FDTD) simulations were performed using measured refractive indices of planar a-Si:H films (deposited previously, but at the same conditions), literature measurements of ZnO:Al refractive indices, and the observed geometries of the planar and nanohole devices. The strong agreement of the simulated and measured spectra in Figure 3a–d indicate that these differences are indeed structural phenomena and not due to contamination from etching or other spurious influences. Furthermore, this high level of agreement allows us to computationally distinguish the desired absorption in the a-Si:H bulk from the parasitic absorption occurring in the ZnO:Al with reasonable confidence.

In Figure 4, we plot the FDTD-calculated distribution of photon density between reflectance, transmittance, and

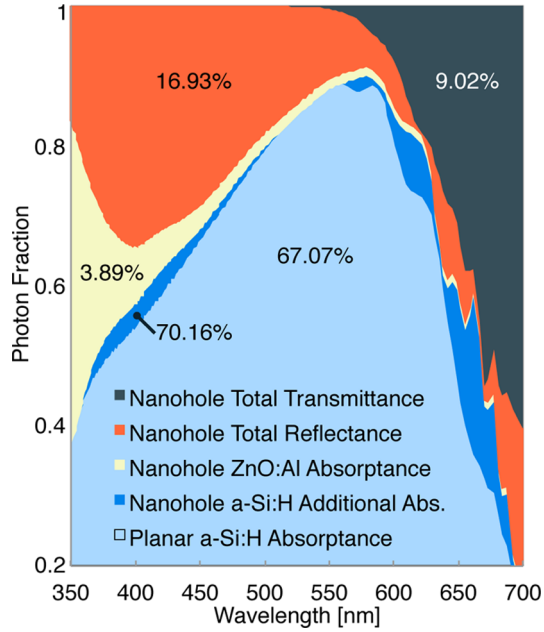

Figure 4. FDTD simulations of the distribution of photon density between transmittance, reflectance, and absorptance in the a-Si:H and ZnO:Al and indicating the differential absorptance between nanohole and planar devices. Percentage labels on the plot areas indicate the fraction of photons between 350 and 700 nm in the AM1.5 spectrum present in the given mechanism.

of the uncoated planar devices, likely due to the presence of the holes working as a gradient refractive index and thus moderately reducing reflection losses in the structured device. Both devices show quite low absorption overall, however. This is remedied by the application of that ZnO:Al TCO/ARC layer, also shown in Figure 3a,b and indicating substantial improvements in the absorptance of both device stacks.

In Figure 3c,d, we see that the transmittance of both the nanostructured and planar materials is negligible at wavelengths below ~600 nm. It is especially reassuring to see this lack of increased transmittance as the nanohole structures have ~16% of the material removed. This indicates that absorption in the nanohole structures is not simply acting as an effective medium (an average of the materials composing the nanostructure, in this case a-Si:H and air), as would be evidenced by an increased level of transmission, particularly in the absorption tail region

absorptance in the ZnO:Al and a-Si:H materials. Through integration of the absorption of the two devices over the solar spectrum, we can calculate that the nha-Si:H material absorbs ~3% more photons than the planar devices, after a ~1% increase in the ZnO:Al parasitic absorption between the nha-Si:H and planar configurations. While this ~3% is a fairly modest improvement, it should be noted first that this is only a secondary benefit, as the main goal of this work is to test the possibility of improving efficiency though increased collection probability, second, that this ~3% increase in absorbed photons is occurring despite the reduced amount of material, and third, that if the collection improvement is indeed successful, devices could be made substantially thicker, further compounding these absorption increases. This also is only a comparison of total absorption; if the location of the absorption in the nanohole devices is being shifted toward the surface, this could also

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produce further benefits in terms of improved collection probabilities.

Test Device Electrical Characterizations. We next investigate electrical characterizations of our devices, first by performing current density−voltage (J−V) measurements. A series of 16 samples were fabricated, consisting of 8 nanohole structured samples and 8 planar samples, and each pair was coprocessed (all processes, e.g., depositions, cleanings, were done together) to reduce possible spurious influences improving or degrading any of the devices. All samples further contained 4 devices (see the Supporting Information), at least two devices per sample are measured with all J−V data current-averaged to produce the traces in Figure 5a.

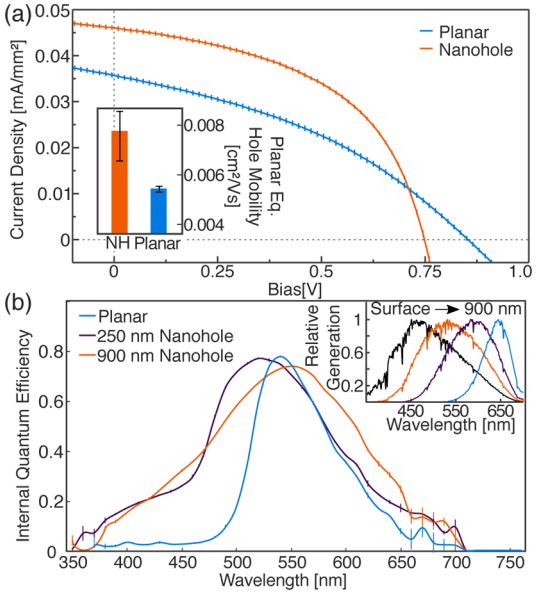

Figure 5. Characterization of nanohole test devices: (a) device current−voltage comparison, showing improvement in current density and fill factor of nha-Si:H devices over their planar equivalents. (Inset of part a) Time-of-flight hole drift mobilities for nha-Si:H compared to the planar device of similar deposition from ref 7. (b) Internal quantum efficiency (IQE), calculated by normalization to total device short-circuit current for 1000 nm thick devices, with planar, 250 nm, and 900 nm deep etched configurations, with increased high-energy IQE for small etches, and the lower-energy IQE for deeper etches. (Inset of part b) Simulated spectrum of relative generation rates depicting deeper absorption of longer wavelengths in a-Si:H. Vertical bars on all plots denote the standard error of the mean.

From the traces in Figure 5a, we can see a few interesting features: First, there is a considerable increase in the short-circuit current density, we observe an average increase of 28.8% in the current output of the nanohole devices, relative to the planar average. We also see substantial increases in the fill factor of these devices, a 33.5% relative increase of the nha-Si:H devices over the planar counterparts. Unfortunately, the open-circuit voltage (V_{OC}) is observed to decrease from the planar to nanohole devices; the relative change is around a 12% drop on average. Despite this decrease in V_{OC}, we still observe a 55% relative improvement in the efficiency of the nha-Si:H devices over the planar equivalents. It is important to note, however, that the devices in this round of samples are of quite low efficiency still; the cells tested showed only a 2.16% power conversion efficiency. In the final section of this work, we confirm these improvements for devices with much higher efficiencies, but first it is important to understand the mechanisms of the changes in our observed device performances.

While we observe significant efficiency improvements in the first series of nanohole-structured a-Si:H devices, there still remains some question as to the mechanisms permitting said improvement. It is plausible that there could be the intended modified drift field present, allowing holes to move toward the nanohole-filled contacts, as opposed to through the full device thickness, increasing the observed (planar-equivalent) mobility through the full cell; but it also is possible that the modified absorption profile (slightly more absorption in a substantially smaller volume) is allowing the improvement of the transport to occur from band-tail state saturation, thereby increasing the average mobility of the holes moving through the device or alternatively by simply causing a higher concentration of the absorbed photons and thus photoexcited carriers to exist closer to the surface of the cell, creating a shorter mean transit distance for the minority carrier.

In order to verify the presence of the intended improvement in collection pathways, we perform time-of-flight hole drift mobility measurements (procedure in accord with those performed in ref 7). The nanohole samples were fabricated similar to those used for the absorption measurements, but with an additional deposition of indium tin oxide sputtered onto the quartz slides before the a-Si:H deposition. This is necessary to make contact to the back of the device, and the transparent contact and substrate are necessary as the illumination must occur from the n-type side to measure hole mobilities, while structuring the p-type side.

As shown in the inset of Figure 5a, we see that while the uncertainty in the nanohole structures "planar-equivalent" mobility measurement is substantial, the observed value is still significantly larger than that of the planar device itself. It should be mentioned that we describe this measurement as a "planar-equivalent" mobility, as a true drift mobility measurement would require a constant electric field, with transit linearly through the full device, neither of which is likely the case in the nanostructured devices. While the difference in the observed mobility is more likely due to these deviations in transport direction, length, and field than the true hole drift mobility of the a-Si:H material itself, measuring the mobility that would correspond to a planar device allows us to compare the improvements in hole transport due to the nanostructuring. While some additional error may be introduced due to the comparison being made to a device deposited separately (albeit under the same conditions), this measurement does suggest that the improved current collection mechanism is indeed resulting in an improved extraction pathway, as opposed to purely preferential surface absorption. Furthermore, we see little to no change in the mobility of planar or nanohole devices as a function of the laser fluence (changes on the order of a factor of 2, through modified attenuation), also suggesting that we are seeing preferential extraction toward the nanohole regions, as opposed to simply the increased current density saturating valence band-tail states.

We observe further evidence of the improved collection arising from transport via the nanoholes in plots comparing the internal quantum efficiency (IQE) of planar, shallow, and deeply etched devices, Figure 5b. The IQE is calculated by measuring the external quantum efficiency of the devices, normalized to the total short-circuit current from corresponding J−V measurements and dividing by the computed

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absorptance within the a-Si:H material from the FDTD calculations presented in Figure 4. Using the computed a-Si:H absorptance prevents inclusion of absorptance of the ZnO:Al material, which varies slightly between the planar and nanohole devices. We observe that the shallow, 250 nm structuring allows for a substantial increase in the collection of the short-wavelength end of the spectrum, whereas the deeper nanohole structures permit increases in the longer-wavelength region. These correspond to shallowly and deeply generated carriers, respectively, as depicted in the simulated depth-dependent generations rates in the inset. This agrees well with the picture that the surfaces of the nanohole structures are providing enhanced local absorption (near the edges of the nanoholes), accounting for the short wavelength enhancement, whereas the deeper regions of the nanoholes are improving extraction of more deeply generated holes, as evidence by the improved collection in the longer wavelength regime. This agrees well with previous theoretical investigations into similar structures showing increases in total absorption for thin devices with shallow hole arrays, with the largest optical enhancements at shallow depths within the material.[36]

High-Efficiency Device Validation. To continue with the validation of the potential for efficiency improvements of this design, we fabricate a second series of higher material-quality devices, with the critical distinction being the higher purity of the a-Si:H i- and n-type layers, being deposited in dedicated chambers with processes optimized for high-efficiency devices. Device cross sections are shown in Figure 6a. Details of the fabrication of these devices can also be found in the Methods section below.

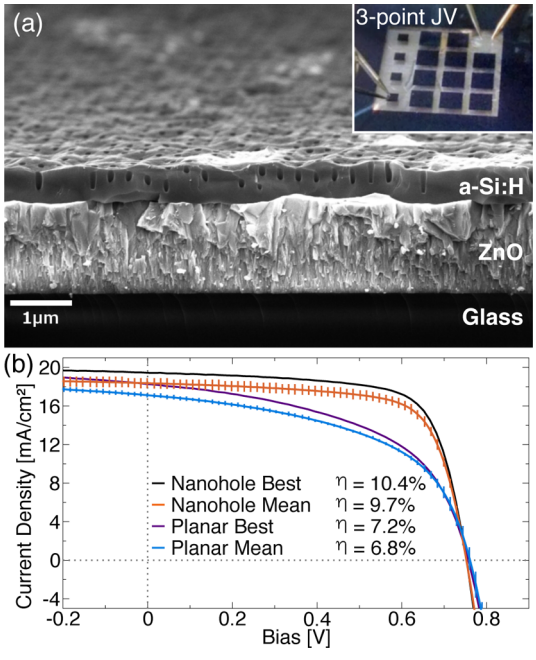

Figure 6. High-efficiency device characterization: (a) SEM cross-section view (at 9° angle) of higher-quality a-Si:H devices after etching but before top surface depositions. A slight random surface texturing from the thick bottom ZnO layer is visible, limiting the tractable etch depth. (Inset in part a) Device view under three-point $J-V$ testing. (b) $J-V$ traces comparing the highest efficiency planar and nanohole structured devices measured as well as current-averaged mean device traces, with conversion efficiency labeled in the figure. Vertical bars denote the standard error of the mean.

$J-V$ measurements were performed similarly to those discussed earlier, although with the device size limited to 1 mm × 1 mm squares, due to difficulties with surface contamination leading to shorting in many of the larger samples (likely during the cleaving of the devices with the thick ZnO back contact). The measurement setup is depicted in the inset of Figure 6a.

In Figure 6b we show the comparison of $J-V$ traces between the highest performing intrinsic layer planar and nanohole structured devices. We observe moderate relative improvements in the short-circuit current of the nanohole-structured samples of ∼6.7%, no degradation in the open-circuit voltage, and large enhancements in the fill factor, a 37% relative improvement. We attribute this enhancement in the fill factor to the decreased transit length and local field enhancement near the nanohole structures, allowing the extraction of carriers at lower bias voltages as well as a potential shift in the carrier generation location closer to the front contact (or hole surfaces). The increase in short-circuit current also indicates a larger collection probability even at the highest internal fields in the devices, although the marginal improvement of these devices is lower than before, likely due to the overall drift length increase courtesy of the higher purity intrinsic material as well as the ∼3% absorptance increase. The current-averaged mean device traces exhibit the same behavior, although with slightly lower performance.

In Figure 7 we investigate the dependence of the average solar cell parameters of our high-efficiency devices on the total

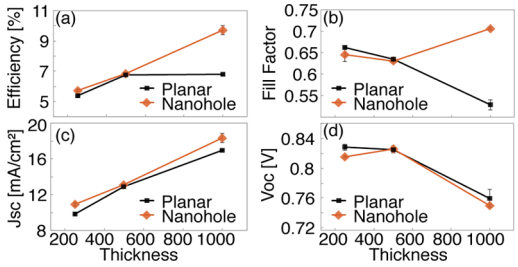

Figure 7. Comparison of mean high-efficiency device properties for both planar and nanohole structured devices, of varying thicknesses: (a) device efficiency, (b) fill factor, (c) short-circuit current density, and (d) open-circuit voltage. Error bars represent standard error of the mean.

device thickness. We see that for planar devices, moving from 250 nm thick intrinsic layers to 500 nm thick layers offers considerable improvement, but increasing further to 1000 nm offers no benefit, while the J_{SC} of the devices continues to rise as total light absorption increases, this benefit is offset by a substantial degradation in the fill factor as well as a more modest decrease in the V_{OC}. The nanostructured devices behave quite differently, while these 1000 nm thick devices enjoy similar improvements in J_{SC}, the increased fill factor allows for the efficiency to continue to climb. We attribute this decay in the planar devices to the limited carrier (hole) collection from the thicker regions of the device at the maximum power point, whereas the improved collection pathway of our nanostructured devices allows these carriers to be extracted, improving the fill factor substantially, slightly improving the J_{SC}, leading the significant efficiency gains. This provides additional evidence that our device design is indeed working as intended, allowing for improved charge extraction from our devices.

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Finally, it should be noted that due to the small size of the devices, the front probe blocks a substantial amount of the light incident on the cells; care was taken to place the probe contact on the furthest corner of the device to prevent shadowing losses as much as possible, but these are still likely substantial. We observe that when using a second front probe (a 4-point measurement) both planar and nanohole devices experience a short circuit current reduction of ∼8%, indicating that substantial current improvements could be immediately achievable from reduced probe shading. The open-circuit voltages of our samples are also lower than what is normally observed in high-quality a-Si:H devices. We attribute this to two influences: First, the front p-type layer deposition was optimized for coating conformality and not device performance; improvement of this deposition would likely improve our observed voltages and thus the efficiency of our devices. Second, the front contact ZnO:Al material was not fully optimized for high conductivity, increasing series resistance within our devices. Further tuning of this layer could also offer potential device voltage and efficiency increases.

CONCLUSIONS

In this work we discussed the motivations, simulation, fabrication, and characterization of homojunction nha-Si:H devices. We show both moderately improved light absorption (a ∼3% improvement) and significantly improved current collection (a ∼7% improvement in J_{SC} and a ∼37% improvement in fill factor) in our structured devices, ascribable to the intended goal of improved hole transport provided by the ZnO:Al TCO material permeating into the nanohole geometry. These factors combine to result in a ∼45% improvement in power conversion efficiency, up to 10.4% for the best performing devices. Additionally, the application of larger-scale texturing could allow for further optical improvements as could further geometric optimization of the nanohole array. Through optimization of the doped layers (mainly the p-type layer being tuned properly) and the front TCO (minimizing absorption and resistance), a reasonable open circuit voltage of at least ∼0.90 V should be obtainable.[37] We estimate that such improvements alone could yield efficiencies beyond 13% for similar devices (assuming an unchanged fill factor and a J_{SC} corrected for shading losses), with further increases possible from improved light absorption.

We also note that the structure explored herein can be made almost entirely with industrially scalable methods: Interference lithography allows near-instantaneous patterning of up to 6 cm^2 devices in a laboratory setting, and with a rastering Lloyd's mirror setup, full wafers or even roll processes could be feasible. ALD depositions could be replaced by more rapid pulsed CVD methods, or by solution deposition of TCO nanoparticles, carbon-based conducting structures (nanotubes or graphene nanoplates), or the alternative heterojunction structures (such as PEDOT:PSS), to improve the scalability of this step. The requirement of etching of the nanohole structures would likely be the largest barrier to large-scale fabrication, although this could as well be replaced by metal-assisted etching or other less capital-intensive methods than RIE. Finally, this process could be applied to other low mobility materials or combined into tandem cell structures, with other materials (e.g., perovskite or cuprous oxide) permeating into the nanoholes and allowing optical and collection enhancements in both layers. Because of the need for only processing the front side of the material, the structure is also compatible with more traditional a-Si on c-Si tandem configurations as well.

METHODS

Test Device Fabrication. The test device fabrication process begins by depositing the n-type and intrinsic a-Si:H layers. Similar to the deposition discussed in ref 38, plasma-enhanced chemical vapor deposition (PECVD) is used to deposit a phosphorus-doped n-type layer, of approximately 20 nm, followed by a 1000 nm thick intrinsic layer. A 180 nm SiO_2 layer is then deposited as a hardmask for future lithography steps.

The devices are then spin-coated with an antireflection coating and photoresist layer. Interference lithography is used to produce a linear interference pattern on the devices, which are exposed, rotated 90°, and then re-exposed to create circular features at the intersection of the orthogonal linear interference lines. After development this results in a square array of holes 150 nm in diameter with a pitch of twice the diameter (300 nm). The patterned photoresist layer is used for etching through the SiO_2 layer, performed with a CH_4 reactive ion etch (RIE). The resulting film is shown in Figure 2a. Next, the patterned SiO_2 layer is used to mask the etching of the nanoholes into the a-Si:H material. This is performed with a Cl_2 inductively coupled plasma (ICP) RIE step, yielding an anisotropically etched hole ∼800 nm deep. For additional details, see the Supporting Information.

Once the RIE processes are complete, the SiO_2 layer is removed by a 20 s wet etching in a 7:1 dilution of buffered hydrofluoric acid (HF). A slight widening at longer times confirms that the HF solution is permeating the holes and thus should be removing any SiO_2 material redeposited from the etching process as well as any damaged a-Si:H. The final films show extremely regular patterns of nanoholes across the entire patterned surface, as shown in Figure 2b,d.

Top layer deposition proceeds by first depositing a p-type a-Si:H layer coating the walls of the nanohole structures. In an effort to deposit a (at least) semiconformal coating, we determined that for our deposition regime that the most conformal films are formed at high pressure and high discharge power (see the Supporting Information). Unfortunately this corresponds to the highest deposition rate case as well, making thickness control and repeatability of the deposition more difficult. This is calibrated to give somewhat thick layers of 30 nm on the top surface but allows for more nominal wall thicknesses. Next, we perform atomic layer deposition (ALD) of 65 nm of aluminum-doped zinc oxide (ZnO:Al) as both the front transparent contact, as well as an antireflection coating.

Finally, because of the complete coating of the ALD process, we must isolate devices before testing. To do this we photolithographically define an array of four 2 mm × 2 mm squares of unexposed area in the center of the sample, isolating the surfaces of four devices. The exposed ZnO:Al is then etched using a 10% mixture of HCl. A final device is shown in both the cross section and top views in parts c and e of Figure 2, respectively.

High-Efficiency Device Fabrication. The second series of higher material-quality devices are deposited on glass, with a 1500 nm thick zinc oxide (ZnO) rear contact, followed by a similar n-type and intrinsic layer a-Si:H deposition (each performed in respective dedicated deposition chambers), with *i*-layer thicknesses of 250, 500, and 1000 nm, to allow for comparisons of the best performing thicknesses of planar and nanostructured configurations. More information on this deposition process can be found in ref 39.

As seen in Figure 6a, the ZnO back contact gives the material a slight random surface texturing, which limits the depth of the etching we are able to perform without risking shorting of the two contacts. For this reason, conservative etch lengths of 100, 200, and 700 nm, respectively for the three thicknesses were used.

ASSOCIATED CONTENT

Supporting Information

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Analytical device model motivating nanohole geometry, fabrication details of deposition and etch conditions, and additional characterization details of influence of etch depth on photovoltaic performance (PDF)

AUTHOR INFORMATION

Corresponding Authors

*E-mail: johlin@alum.mit.edu.
*E-mail: buonassisi@mit.edu.
*E-mail: jcg@mit.edu.

Present Addresses

[§]E.J.: FOM Institute AMOLF, Amsterdam, The Netherlands.
[‖]M.S.: Arizona State University, Tempe, AZ.

Notes

The authors declare no competing financial interest.

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