A Novel Current-Mode Low-Power Adjustable Wide Input Range Four-Quadrant Analog Multiplier

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Abstract- In this paper, a novel current mode enhanced input range four-quadrant analog multiplier is presented. The proposed class AB based translinear current squarer allows the designer to control the input range via a digital code. Moreover, the proposed scheme improves the linearity of the circuit and has a high robustness against process variations. The Post-layout and Monte Carlo simulation of the multiplier in a 0.18μm standard CMOS technology shows an input range of (1+m)×10μA (where 'm' is an adjustable parameter), a THD of 1% (@1MHz), a -3dB bandwidth of 332.3MHz (for m=3) and a power consumption of 186 μW.

Keywords- current mode, low-power, wide input range, analog multiplier, four-quadrant.

1. Introduction

Real-time analog multiplication of two signals is an important operation in the analog signal processing applications [1]. The multiplier is used in many analog signal processing systems such as modulators and mixers, variable gain amplifiers, adaptive filters, phase locked loops, artificial neural networks and fuzzy logic controllers [1, 2].

A significant work for implementing analog multiplication has been conducted in CMOS and BJT mostly focusing on circuit level techniques. Analog voltage mode multipliers, which produce a voltage/current signal proportional to the multiplication of two input voltage signals have been categorized and analyzed in [1].

However, the voltage mode multipliers undergo various limitations regarding their direct dependence on the voltage supply and sensitivity to process variations. Furthermore, by scaling the technology and consequently scaling the supply voltage, the operating (input) range of this type of multipliers are being squeezed even more.

Current mode signal processing offers low voltage and high speed in comparison to voltage mode signal processing. However, the proposed current mode multipliers thus far, have a limited input range. Based on [3] analog current mode multiplication of two signals is generally realized either in weak inversion or strong inversion. Weak inversion multipliers are an interesting choice for extremely low voltage/power applications; however, they undergo limited input range and narrow bandwidth [4-6].

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Various implementations for CMOS current mode strong inversion multipliers have been proposed [7-15]. Fig.1 shows the block diagram of different realizations of the current mode multiplier in the strong inversion. One approach is to convert the input currents to voltage and then apply the voltage to two/three voltage mode squarers. This technique suffers from strong dependence of the output current to the device parameters and power supply variations [12-15]. Furthermore, the input ranges of these types of multipliers are limited by the maximum allowable voltage swing in the voltage squarer, which is generally limited to the voltage supply. In the second technique, different types of translinear loops (TL) (stacked or up-down configurations [16]) are used to realize the current mode squarer and/or geometric mean blocks as basic building blocks of the multiplier [7-11]. A TL is a special device arrangement that allows a useful large signal relationship among their currents [16-18]. The advantage of this technique over other abovementioned voltage or current mode techniques is in its capability to provide pure current mode output which is independent of device parameter or supply voltage. However, the input range of these types of multipliers is usually limited to the imposed limitation of the current squarer, which is the prerequisite of working in saturation region for all the transistors in the TLs. Moreover, the only way to enlarge input range in these types of multipliers is to increase the bias current, which in turn leads to increase in power.

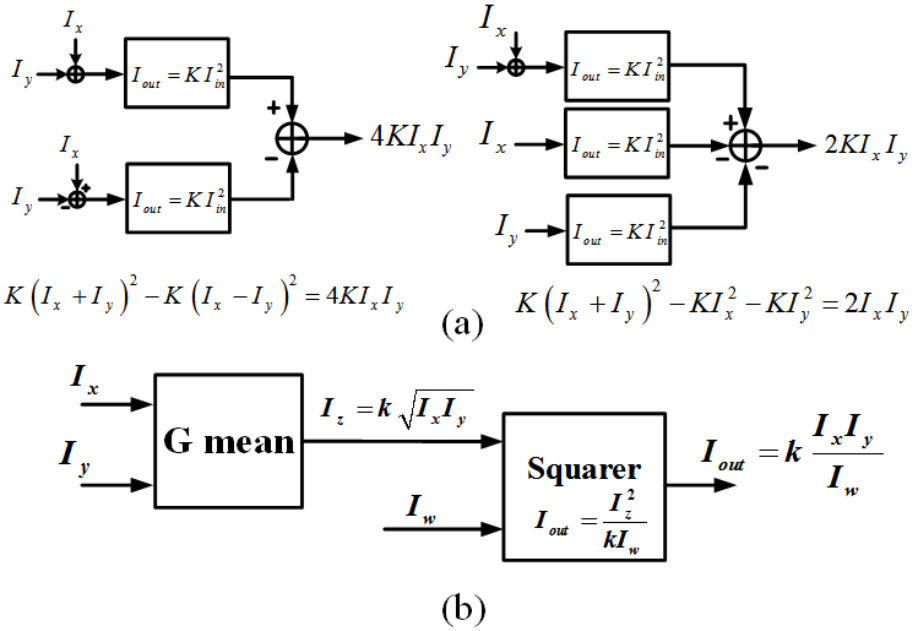

Fig. 1. Block diagram of different realizations of the current mode multiplier in the strong inversion
a) Using two/three squarers, b) Using geometric mean-squarer

The proposed multiplier offers a new solution to extend the input range without any increase in the power consumption. This solution combines modified low power class AB current buffer with translinear based current squarer to achieve a wide and adjustable input range multiplier that provides a pure current mode output. It is also shown that this technique improves the linearity of the multiplier. The paper is organized as follows. The proposed circuit is presented in Section 2,

the proposed structure is analyzed in section 3, simulation results are shown in Section 4 and conclusions are given in Section 5.

2. Circuit Description

The operation of the proposed multiplier is based on the implementation of the quadratic equation as

$$I_{out} = k(I_x + I_y)^2 - k\left(I_x - I_y\right)^2 = 4kI_xI_y \quad (1)$$

Where I_{out} is the output current, I_x and I_y are input current signals and k is the scaling factor. This technique provides four quadrant operation in principle, while the geometric-mean based technique is only capable of implementing two quadrant multiplication [7]. From (1) it is deduced that two current mode squarers are needed to realize the current mode multiplication. These squarers should provide two quadrant operation in order to achieve four quadrant multiplier. Therefore, the characteristics of the current squarers (e.g. power consumption, input range and linearity) directly determine that of the multiplier.

2.1. Current-mode Squarer Circuit

The current-mode squarer circuit is shown in Fig. 2. The circuit consists of two sub-blocks which are highlighted in the figure: A modified class AB current buffer stage and a translinear loop formed by $M_1 - M_4$ which are biased in the saturation region [19]. The function of the class AB buffer is to introduce the proper portion of the input current into the TL in such a way that the whole circuit works as a two-quadrant current squaring circuit. The key point is that the input current of the proposed circuit can be two quadrant without any need for extra bias currents thanks to the intrinsic characteristic of the class AB stage. For the sourcing input currents, M11, M17, M9, M7 conveys the current to the translinear loop and for the sinking input currents, M10, M16, M8, M6 do the same. Moreover, it is shown in section 3.1 that the modified structure of the current buffer helps to extend the input operating range of the squarer beyond the limitation dictated by the current squarer. Furthermore, it is shown in the following sections that the proposed scheme improves the linearity and robustness of the circuit against process variations. In the circuit the aspect ratios of $M_{16}\ and\ M_{17}$ (m-transistors) are 'm' times larger than $M_{10}\ and\ M_{11}$ respectively. Applying KCL in the input node gives:

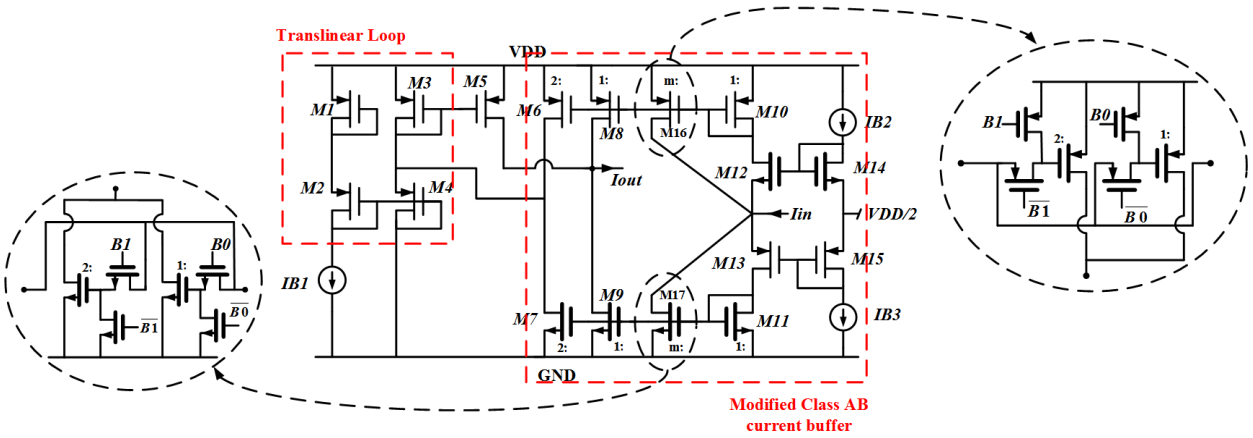

Fig. 2. The proposed Current-mode squarer

$$I_{in} = I_{M16} + I_{M10}\ (or: I_{in} = I_{M17} + I_{M11}) \quad (2)$$

The currents of transistors M_8 and M_{10} are given as

$$I_{M8} = I_{M10} = \frac{I_{in}}{1+m}\ \ (or:\ I_{M9} = I_{M11} = \frac{I_{in}}{1+m}) \quad (3)$$

Based on the class AB operation, M_8 and M_9 provide two quadrant output current. This is also valid for M_6 and M_7, which their aspect ratios are twice the diode connected transistors M_{10} and M_{11} respectively:

$$I_{M6} = \frac{2I_{in}}{1+m}\ (or: I_{M7} = \frac{2I_{in}}{1+m}) \quad (4)$$

These currents are injected into the TL in order to realize the two quadrant current squarer. Since the aspect ratios of $M_1 - M_4$ transistors are equal, based on the MOS translinearity (MTL) principle in saturation region ([16])

$$2\sqrt{I_{B1}} = \sqrt{I_{DS3}} + \sqrt{I_{DS4}} \quad (5)$$

Where I_{B1} is the bias current of transistors M_1 and M_2. I_{DS3} and I_{DS4} are the drain-source current of transistors M_3 and M_4 respectively, which can be expressed as

$$I_{DS_3} = I_{DS_5} = I_{out} + \frac{I_{in}}{1+m} \quad (6)$$

$$I_{DS_4} = I_{DS_3} - 2\frac{I_{in}}{1+m} = I_{out} - \frac{I_{in}}{1+m} \quad (7)$$

Where I_{DS5} is the drain-source current of M_5 and I_{out} is the output current of the squarer. Substituting (6) and (7) into (5) yields

$$2\sqrt{I_{B1}} = \sqrt{I_{out} + \frac{I_{in}}{1+m}} + \sqrt{I_{out} - \frac{I_{in}}{1+m}} \tag{8}$$

Squaring both sides gives the output current as

$$I_{out} = \frac{{I_{in}}^2}{4I_{B1}(1+m)^2} + I_{B1} \tag{9}$$

Equation (9) describes the operation of the proposed squarer circuit. It is noteworthy that the output current is insensitive to PVT variations thanks to the benefits of using TL based structure. Another point is that 'm' sets the amount of current injected into the TL. Therefore, with a larger m, the input range can be extended significantly. The implementation of 'm' is realized through a set of switches that can be controlled by a digital code, as it is shown in Fig.2 and is discussed in more details in sections 2.2 and 3.1.

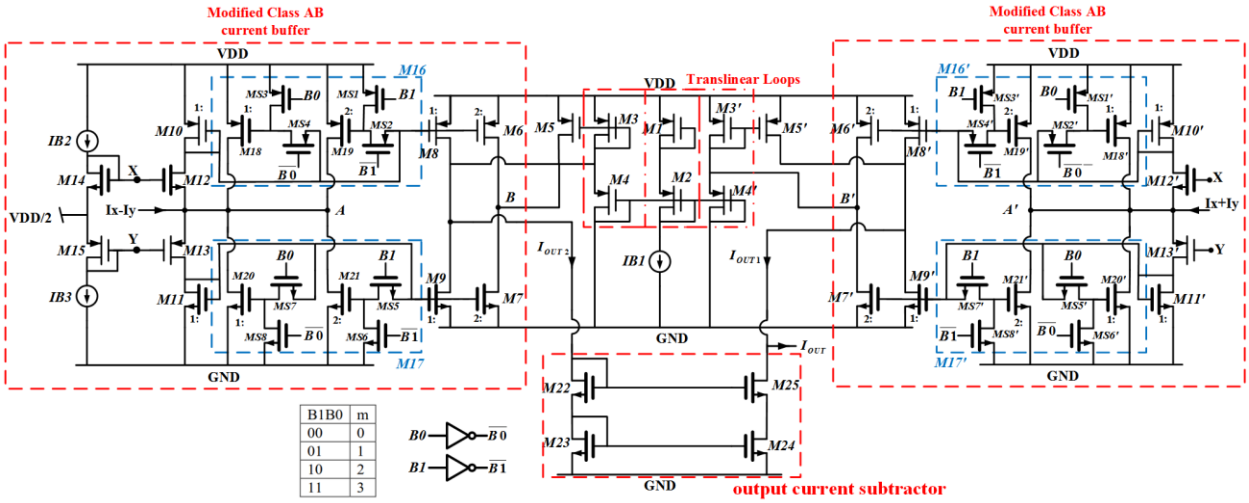

Fig. 3. The proposed four-quadrant multiplier

2.2. Current-mode Multiplier Circuit

The proposed current mode multiplier is shown in Fig. 3. It consists of two current mode squarers as discussed in section 2.1 and a current subtractor. Each current squarer comprises a class AB current buffer and a TL. In order to implement m-transistors (M_{17}, M_{17}', M_{16} and M_{16}') two binary weighted transistors and a set of MOS switches are used. For instance, the M_{17} is implemented by transistors M_{20} (:1) and M_{21} (:2) and MOS switches of M_{s5}, M_{s6}, M_{s7} and M_{s8}. In a similar manner, M_{16} is implemented by transistors M_{18} (:1) and M_{19} (:2) and MOS switches of M_{s1}, M_{s2}, M_{s3} and M_{s4}. A 2-bit binary code (B_1B_0) controls these switches to provide four values of 'm' (0, 1, 2 or 3). It is shown in the following sections that selecting higher amounts of 'm' leads to improve the input range and linearity of the multiplier. The two TLs (M_1, M_2, M_3, M_4 and M_1, M_2, M_3', M_4') share M_1 and M_2, which are biased by a constant current and provide a

constant bias point for the TLs. Using this technique, the power consumption of the TLs is reduced and the device mismatches between TL transistors and the biased currents are alleviated. M_{14} and M_{15} are also shared between two class AB current mirrors in the same manner. The input signal of the right squarer is $I_X + I_Y$ while $I_X - I_Y$ is applied to the left one. In current-mode, the summation and subtraction of two signals can be simply implemented by a combination of simple or class AB current mirrors as in [11]. According to (9) the output current of each squarer is

$$I_{out1} = \frac{(I_X + I_Y)^2}{4I_{B1}(1+m)^2} + I_{B1} \tag{10}$$

$$I_{out2} = \frac{(I_X - I_Y)^2}{4I_{B1}(1+m)^2} + I_{B1} \tag{11}$$

The current subtractor which is a cascade current mirror (M_{22}-M_{25}) removes the DC and other squared terms. Therefore, the output current of the circuit is derived as

$$I_{out} = I_{out2} - I_{out1} = \frac{I_X I_Y}{I_{B1}(1+m)^2} \tag{12}$$

Equation (12) indicates the function of the proposed current-mode multiplier and demonstrates that the output current is independent of process parameters. Parameter 'm' which is controllable via a 2-bit binary code (B_1B_0), determines the size of M_{16} *and* M_{17} and plays a key role in controlling the input range of the multiplier without an increase in power consumption. Therefore this structure allows obtaining wider input range by selecting larger 'm'. Moreover, it is shown in sections 3.2, 3.3 and 3.4 that increasing 'm' leads to alleviate the absolute error causing by the different types of mismatches (V_{TH} and transconductance parameter mismatches) and improves the linearity of the circuit.

3. Performance Analysis

3.1. Input Range

The input range of the multiplier is basically restricted by the prerequisite of working in saturation for transistors of translinear loops. Based on this, the input range of the proposed multiplier can be derived as

$$\frac{|I_X+I_Y|}{1+m} \le 2I_B \quad , \frac{|I_X-I_Y|}{1+m} \le 2I_B \tag{13}$$

Equation 13 yields in

$$|I_X| = |I_Y| \le (1+m)I_B \tag{14}$$

In the conventional current mode multipliers such as [3], [8, 9], [11], [15], the input range of the circuit is extended by increasing the bias current which leads to a higher power consumption. However, equation (14) indicates that the maximum allowable input current of the proposed multiplier can be adjusted as a function of m, without the need for extra power consumption. The implementation of this parameter can be done by controlling the sizes of M_{16} and M_{17} in each squarer. It is shown in Fig. 3 for four different amounts of 'm' (0-3) using NMOS and PMOS switches and two binary bits, as it is discussed in section 2.2.

3.2. V_{TH} Mismatch

The body-source voltage of a MOS transistor affects the threshold voltage by [20]

$$V_{TH} = V_{TH0} + \gamma(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}) \quad (15)$$

Where, V_{TH0} is the threshold voltage with $V_{SB} = 0$, γ is the body effect coefficient and $2\Phi_F$ is the substrate bias. This affect can be cancelled out if the bulk terminal is tied to the source. In the proposed circuit n-well CMOS technology is used therefore all PMOS bodies are tied to their source while all NMOS bodies are tied to the ground. Since all transistors in translinear loops are PMOS, the body effects of these transistors are completely eliminated. However, the fabrication process may cause a V_{TH} mismatch between these transistors. The V_{TH} mismatches of the M_1-M_4 are modeled as follows

$$V_{TH,i} = \overline{V_{TH}}(1 + \delta_i) \quad \text{i=1-4} \quad (16)$$

Where $V_{TH,i}$ is the threshold voltage of the i[th] transistor and $\overline{V_{TH}}$ is the average threshold voltage. The MTL principle in the presence of V_{TH} mismatches can be written as

$$\sqrt{\frac{I_B}{K}} + \overline{V_{TH}}(1 + \delta_1) + \sqrt{\frac{I_B}{K}} + \overline{V_{TH}}(1 + \delta_2) = \sqrt{\frac{I_{OUT} + \frac{I_{in}}{1+m}}{K}} + \overline{V_{TH}}(1 + \delta_3) +$$

$$\sqrt{\frac{I_{OUT} - \frac{I_{in}}{1+m}}{K}} + \overline{V_{TH}}(1 + \delta_4) \quad (17)$$

Where K is the transconductance parameters of the TL transistors. Squaring both sides and neglecting δ^2 terms, the output current of the squaring circuit is

$$I_{OUT} = \frac{{I_{in}}^2}{4I_{B1}(1+m)^2}\left(1 - \sqrt{\frac{K}{I_{B1}}}\overline{V_{TH}}[(\delta_1+\delta_2)-(\delta_3+\delta_4)]\right) + I_{B1} + \sqrt{KI_{B1}}\overline{V_{TH}}[(\delta_1+\delta_2)-(\delta_3+\delta_4)] \quad (18)$$

Equation (18) is obtained using the following approximation

$$\frac{1}{1+x} \approx 1 - x \quad for \quad |x| \ll 1 \quad (19)$$

Hence the output current of the multiplier can be derived as follows

$$I_{OUT} = \frac{I_X I_Y}{I_{B1}(1+m)^2}\left(1 - \sqrt{\frac{K}{I_{B1}}}\overline{V_{TH}}[(\delta_1+\delta_2)-(\delta_3+\delta_4)]\right) \quad (20)$$

Therefore the absolute output error of the multiplier resulting from threshold voltage mismatch is

$$|Error| = \frac{I_X I_Y}{I_{B1}(1+m)^2}\left(\sqrt{\frac{K}{I_{B1}}}\overline{V_{TH}}[(\delta_1+\delta_2)-(\delta_3+\delta_4)]\right) \quad (21)$$

Equation (21) indicates that introducing 'm' to the circuit reduces the absolute error due to V_{TH} mismatches.

3.3. Transconductance Parameter Mismatch

The effect of transconductance parameter mismatches is analyzed in two parts: The mismatch effect of the transistors in the TL and the mismatch effect of the class AB current buffers.

3.3.1. Transconductance parameters mismatch in TLs

The mismatch of the transconductance parameters of the TLs are modeled as follows:

$$K_i = \overline{K}(1+\sigma_i) \qquad \text{i=1-4} \quad (22)$$

Where K_i is the transconductance of the i[th] transistor and $\overline{K}$ is the nominal value of the transconductance. In this case, the MTL principle can be written as

$$\sqrt{\frac{I_{B1}}{\overline{K}(1+\sigma_1)}} + \sqrt{\frac{I_{B1}}{\overline{K}(1+\sigma_2)}} = \sqrt{\frac{I_{OUT}+\frac{I_{in}}{1+m}}{\overline{K}(1+\sigma_3)}} + \sqrt{\frac{I_{OUT}-\frac{I_{in}}{1+m}}{\overline{K}(1+\sigma_4)}} \quad (23)$$

Squaring both sides, neglecting σ^2 terms and using the approximation $\sqrt{1+x} = 1+\frac{1}{2}x$, $|x| \ll 1$, the output current of the squaring circuit is given by

$$I_{OUT} = \frac{{I_{in}}^2}{4I_{B1}(1+m)^2}\left(1+\frac{\sigma_1+\sigma_2-\sigma_3-\sigma_4}{2}\right) + I_{B1}\left(1+\frac{\sigma_3+\sigma_4-\sigma_1-\sigma_2}{2}\right) +$$

$$\frac{I_{in}}{4(1+m)}(\sigma_3-3\sigma_4) - \frac{{I_{in}}^3}{16{I_{B1}}^2(1+m)^3}(\sigma_3+\sigma_4) \quad (24)$$

Thus the output current of the multiplier in presence of the transconductance mismatches and the resulted absolute error are as follows

$$I_{OUT} = \frac{I_X I_Y}{I_{B1}(1+m)^2}\left(1 + \frac{\sigma_1+\sigma_2-\sigma_3-\sigma_4}{2}\right) + \frac{I_Y}{2(1+m)}(\sigma_3 - 3\sigma_4) - \frac{{I_Y}^3 + 3{I_X}^2 I_Y}{8{I_{B1}}^2(1+m)^3}(\sigma_3 + \sigma_4) \quad (25)$$

$$|Error| = \frac{I_X I_Y}{I_{B1}(1+m)^2}\left(\frac{\sigma_3+\sigma_4-\sigma_1-\sigma_2}{2}\right) + \frac{I_Y}{2(1+m)}(3\sigma_4 - \sigma_3) + \frac{{I_Y}^3 + 3{I_X}^2 I_Y}{8{I_{B1}}^2(1+m)^3}(\sigma_3 + \sigma_4) \quad (26)$$

From (26), the absolute error due to the transconductance parameters mismatches in TLs is diminished with the increase of 'm'.

3.3.2 Transconductance parameters mismatch in class AB current buffers

Assume there are mismatches between transconductance parameters of PMOS (or NMOS) transistors in the class AB current buffers in Fig.1. In this case

$$K_i = \overline{K}_i(1 + \varepsilon_i) \qquad \text{i=6, 9, 10, 16} \quad (27)$$

Where $\overline{K}_i$ is a nominal value for i[th] transistor. Therefore, the drain-source current of M_{16} is

$$I_{DS_{16}} = \frac{K_{16}}{K_{10}} I_{DS_{11}} = \frac{\overline{K}(1 + \varepsilon_{16})}{\overline{K}(1 + \varepsilon_{10})} I_{DS_{10}} \quad (28)$$

Assuming $\varepsilon_i \ll 1$, using (18) and neglecting second order terms yields in

$$I_{DS_{16}} = m(1 + \varepsilon_{16} - \varepsilon_{10}) I_{DS_{10}} \quad (29)$$

Substituting (29) into (2), the drain-source current of M_{10} is given by

$$I_{DS_{10}} = \frac{I_{in}}{1+m}\left(1 - \frac{m}{1+m}(\varepsilon_{16} - \varepsilon_{10})\right) \quad (30)$$

From (27) and (30), the drain-source currents of M_8 and M_6 are given by

$$I_{DS_8} = \frac{I_{in}}{1+m}\left(1 - \frac{m}{1+m}\varepsilon_{16} - \frac{1}{1+m}\varepsilon_{10} + \varepsilon_8\right) \quad (31)$$

$$I_{DS_6} = \frac{2I_{in}}{1+m}\left(1 - \frac{m}{1+m}\varepsilon_{16} - \frac{1}{1+m}\varepsilon_{10} + \varepsilon_6\right) \quad (32)$$

Injecting these currents into the TL transistors ($M_1 - M_4$) and calculating the output current of squaring circuit yields

$$I_{out} = \frac{{I_{in}}^2}{4I_{B1}(1+m)^2} + I_{B1} - \frac{I_{in}}{1+m}(\varepsilon_8 - \varepsilon_6) \quad (33)$$

Therefore the output current of the multiplier and the generated error can be expressed as follows

$$I_{out} = \frac{I_X I_Y}{I_{B1}(1+m)^2} - \frac{2I_Y}{1+m}(\varepsilon_8 - \varepsilon_6) \tag{34}$$

$$|Error| = \frac{2I_Y}{1+m}(\varepsilon_8 - \varepsilon_6) \tag{35}$$

From (26) and (35) it can be seen that the absolute error introduced due to transconductance parameter mismatches is reduced by increasing 'm'. Furthermore (35) indicates that M_{10} and M_{16} mismatches have no effects on the output current and the mismatch error is only proportional to the amplitude of the I_Y.

3.4. Total Harmonic Distortion (THD)

The two main sources of non-ideality in the proposed multiplier are the mismatches of the transistors and the channel-length modulation error of mirror transistors which affect the linearity of the circuit [21] (due to the fact that the TL transistors are diode connected, the channel length modulation effect would be waived for these transistors). Since the effect of V_{TH} and transconductance parameter mismatches is discussed in section 3.2 and 3.3, in the following expressions, it is supposed that there is a complete matching between the current mirror transistors (M9 & M11) and (M8 & M10) in the modified class AB current buffer (Fig.2). Taking into account the channel modulation effect for the NMOS side

$$\frac{i_{11}}{1+\lambda V_{DS11}} = \frac{i_9}{1+\lambda V_{DS9}} \tag{36}$$

Since $V_{DS11} = V_{GS11}$ (36) can be rewritten as

$$\frac{i_{11}}{1+\lambda(V_{TH}+\sqrt{\frac{i_{11}}{K_N}})} = \frac{i_9}{1+\lambda V_{DD}/2} \tag{37}$$

$$\frac{i_9}{i_{11}} = \frac{1+\lambda_N V_{DD}/2}{1+\lambda_N(V_{TH}+\sqrt{\frac{i_{11}}{K_N}})} \tag{38}$$

Where $V_{DD}/2$ is the dc voltage at the drain of M_9. Taking the derivative of i_9 with respect to i_{11} gives

$$\frac{\partial i_9}{\partial i_{11}} = \left(1+\frac{\lambda_N V_{DD}}{2}\right)\frac{1+\lambda_N(V_{TH}+\frac{1}{2}\sqrt{\frac{i_{11}}{K_N}})}{(1+\lambda_N(V_{TH}+\sqrt{\frac{i_{11}}{K_N}}))^2} \cong 1-\lambda_N\left(V_{TH}-\frac{V_{DD}}{2}+\frac{3}{2}\sqrt{\frac{i_{11}}{K_N}}\right) \tag{39}$$

Where the terms including λ_N^2 are neglected and it is assumed $2\lambda_N(V_{TH}+\sqrt{i_{11}/K_N}) \ll 1$. Following the same steps for the P-type current mirror (M8-M10) gives

$$\frac{\partial i_8}{\partial i_{10}} = 1 - \lambda_P \left(V_{TH} - \frac{V_{DD}}{2} + \frac{3}{2}\sqrt{\frac{i_8}{K_P}} \right) \quad (40)$$

Assuming the transconductance gain to be equal for both current mirrors ($K_N = K_P = K$), the second and third harmonic distortion are calculated as ([21]):

$$HD2 = \frac{1}{8}\left(\frac{\partial i_9}{\partial i_{11}} - \frac{\partial i_8}{\partial i_{10}}\right)_{i_{in}=I_M} = \frac{(\lambda_N - \lambda_P)}{8}\left(\frac{V_{DD}}{2} - V_{TH} - \frac{3}{2}\sqrt{\frac{I_M}{K(m+1)}}\right) \quad (41)$$

$$HD3 = \frac{1}{24}\left[\left(\frac{\partial i_9}{\partial i_{11}} + \frac{\partial i_8}{\partial i_{10}}\right)_{i_1=I_M} - \left(\frac{\partial i_9}{\partial i_{11}} + \frac{\partial i_8}{\partial i_{10}}\right)_{i_1=I_Q}\right] \cong \frac{(\lambda_N + \lambda_P)}{16}\sqrt{\frac{I_Q}{K}}\left(1 - \sqrt{\frac{I_M}{(m+1)I_Q}}\right) \quad (42)$$

Where I_M is the maximum amplitude of the input current and I_Q is the quiescent current of the class AB buffer. (41) and (42) indicate that both HD2 and HD3 are decreased by increasing 'm'.

4. Simulation Results

The performance of the circuit is simulated using Cadence by 0.18μm standard CMOS technology. A supply voltage of 1.8 V is used and I_{B1} is set to 10μA while I_{B2} and I_{B3} are set to 1.5μA. All current sources have been implemented using simple current mirrors. The device dimensions of the proposed multiplier are shown in Table I. The power consumption of the proposed circuit is 186 μW. The layout of the proposed multiplier is shown in Fig. 4 in which the occupied area is 1590μm^2.

Table 1. Device dimensions of the proposed multiplier

Transistors	Aspect ratios ($\mu m/\mu m$)
$M_1 - M_5$	$^2/_{0.5}$
M_6	$^6/_1$
M_7	$^8/_1$
M_8, M_{10}	$^3/_1$
M_9, M_{11}	$^4/_1$
M_{12}, M_{14}	$^2/_1$
M_{13}, M_{15}	$^5/_{0.5}$
M_{18}	$^3/_1$
M_{19}	$^6/_1$
M_{20}	$^4/_1$
M_{21}	$^8/_1$
$M_{22} - M_{25}$	$^5/_{0.18}$
$M_{s1} - M_{s8}$	$^{0.5}/_{0.18}$

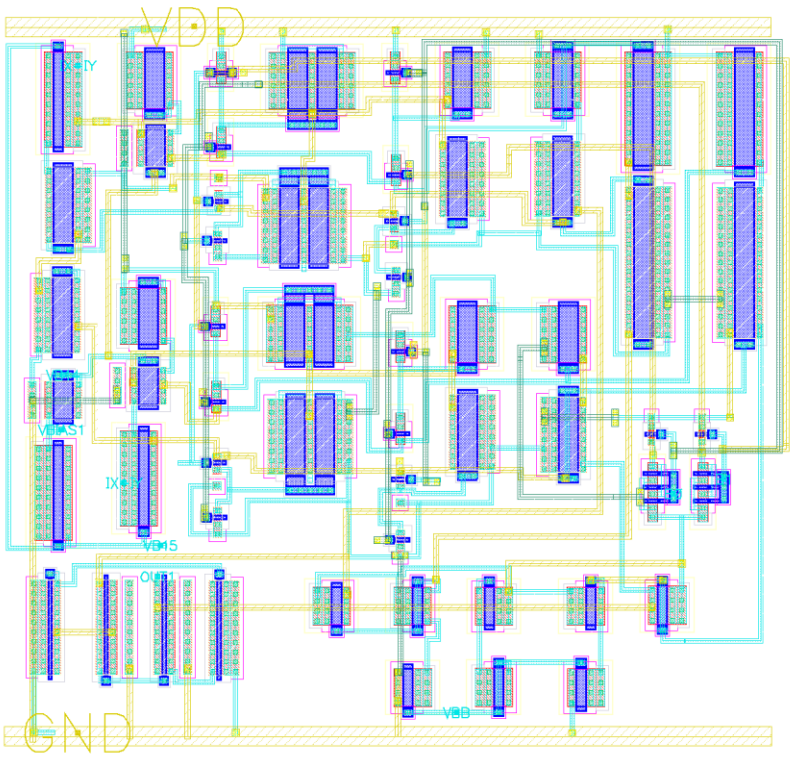

Fig. 4. Layout of the proposed current-mode multiplier

Fig. 5 illustrates the transient response of the multiplier for various amounts of 'm' and demonstrates the functionality of the circuit as an amplitude modulator for different input amplitudes. For each value of 'm' the input currents (I_X and I_Y) are set to the maximum allowable amplitude at 1 MHz and 100 KHz frequencies respectively. For m=0, 1, 2 and 3, the input currents are set to10 μA, 20 μA, 30 μA and 40 μA respectively. Therefore, the maximum amplitude of the output current for all values of 'm' would be equal to 10 µA based on equation (12). Thus, the output current of the circuit for different amounts of 'm' should be similar as it is shown in Fig. 5. It is noteworthy that the only difference between m=0, 1, 2 and 3 is the difference between their input ranges. For instance, the input range for m=1 is 20 μA which is two times bigger than the input range of m=0 (10 μA) while the output currents are the same for the two cases. Similarly, the input ranges for m=2 and m=3 are equal to 30 μA and 40μA respectively while there is no difference between their transient outputs.

Fig. 6 shows the DC transfer characteristic of the output current versus the input currents. For each amount of 'm', the first input is swept between $\pm(m+1) \times 10\mu A$ while a maximum allowable DC current is fed to the second input. For instance, for m=0 the input current is swept between -10 µA to +10µA while for m=3 it is swept between -40µ$A$to +40µA. It can be seen that the circuit works perfectly in the whole operating range for various amounts of 'm'.

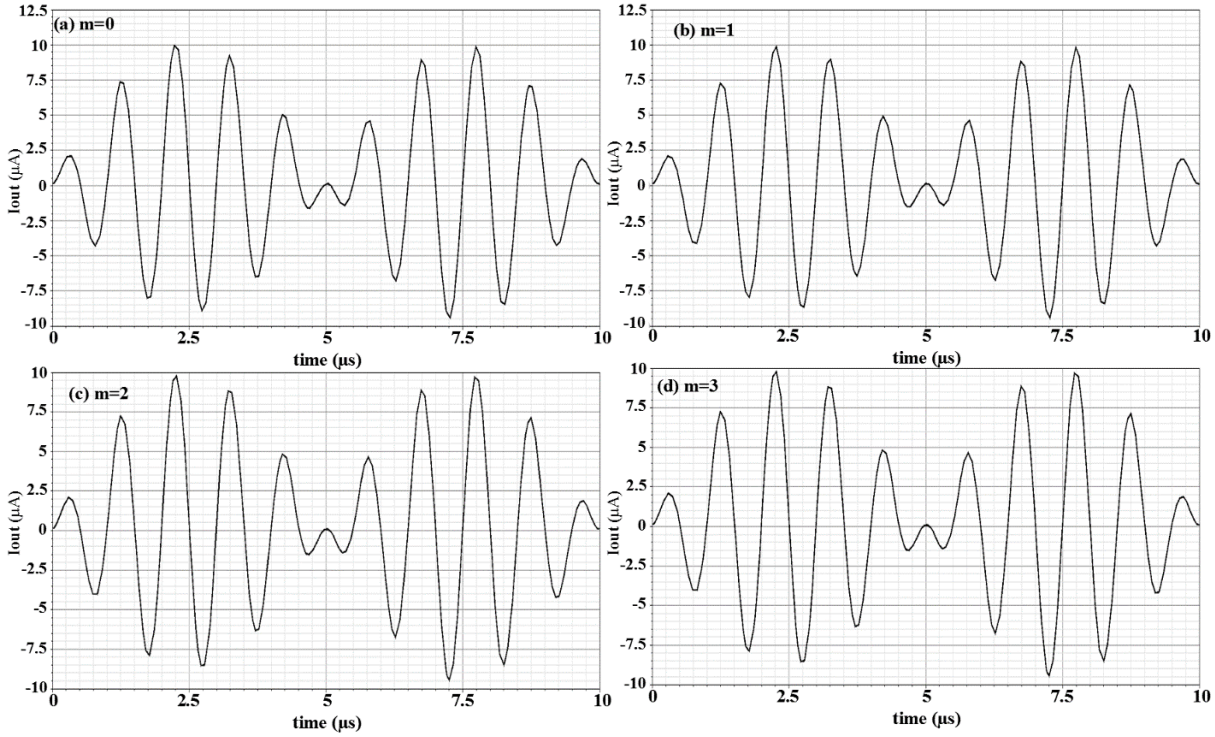

Fig. 5. Post-layout simulated Time response of the proposed multiplier for four different amounts of m, $I_x = (m+1) \times 10\sin(2\pi \times 10^6)\,\mu A, I_y = (m+1) \times 10\sin(2\pi \times 10^5)\,\mu A$
a) m=0 b) m=1 c) m=2 d) m=3

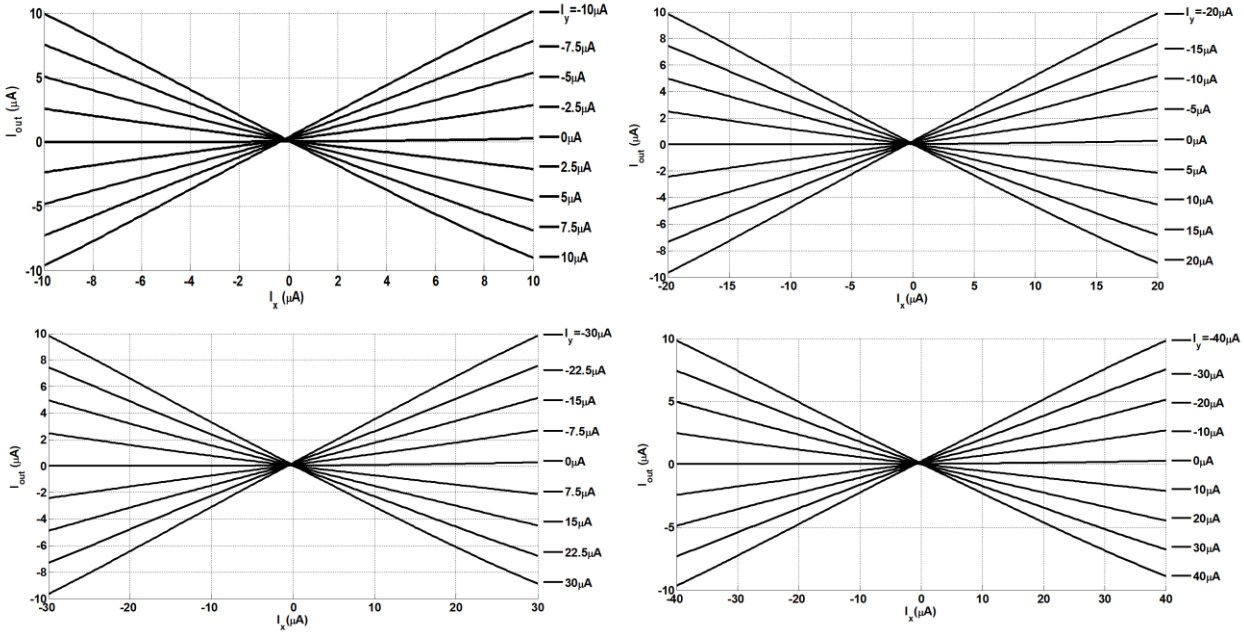

Fig. 6. Post-layout simulated DC transfer function of proposed multiplier
a) m=0 b) m=1 c) m=2 d) m=3

Fig. 7 shows total harmonic distortion (THD) in three input frequencies of 1, 20 and 50 MHz

versus the amplitude of the first input signal (I_X). Here I_X is a sinusoidal signal with an amplitude of $(m+1)\times 10\mu A$ while a same amount of DC current is fed to the I_Y.The THD of the circuit in 1 MHz frequency is ~1% for all amounts of 'm' and it lowers down from ~8% (for m=1, $I_X = 10\mu A$) to less than1.2% (for m=3, $I_X = 10\mu A$) at a high frequency of 50MHz. Fig.7 verifies that increasing 'm' improves the THD of the circuit as it is predicted in section 3.4.

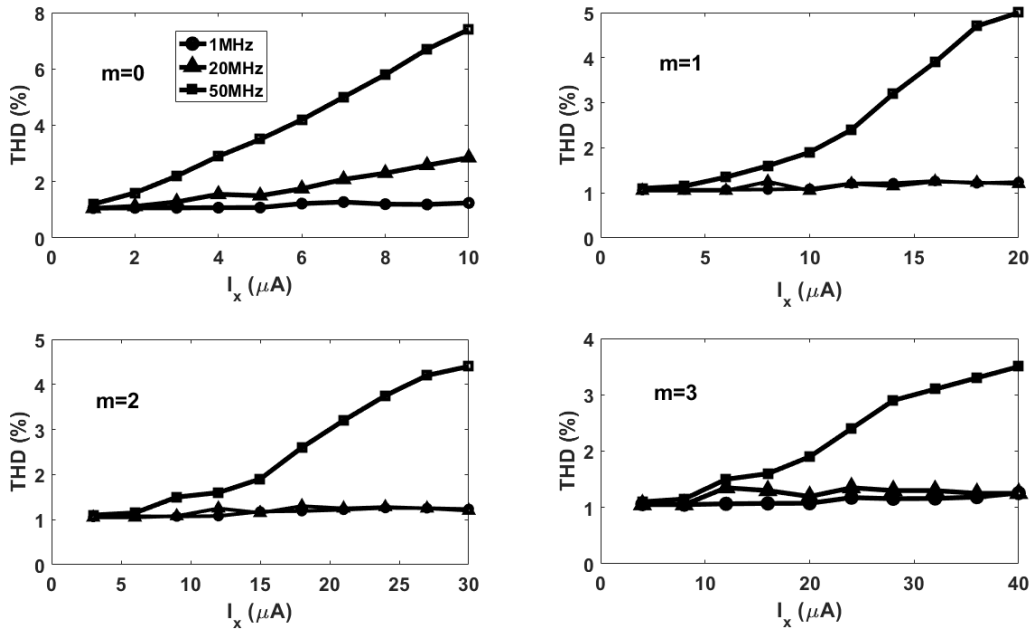

Fig. 7. Post-layout simulated Total harmonic distortion versus input current ($I_{Y_{DC}}$=$(m+1)\times 10\mu A$)

Fig. 8 shows the frequency response of the proposed circuit. In this figure, I_X is small signal and I_Y is set to 10μA, 20μA, 30μA and 40μA for m=0, 1, 2 and 3 respectively. The -3dB bandwidth of proposed multiplier varies from 253.4MHz for m=0 to 332.3 MHz for m=3.

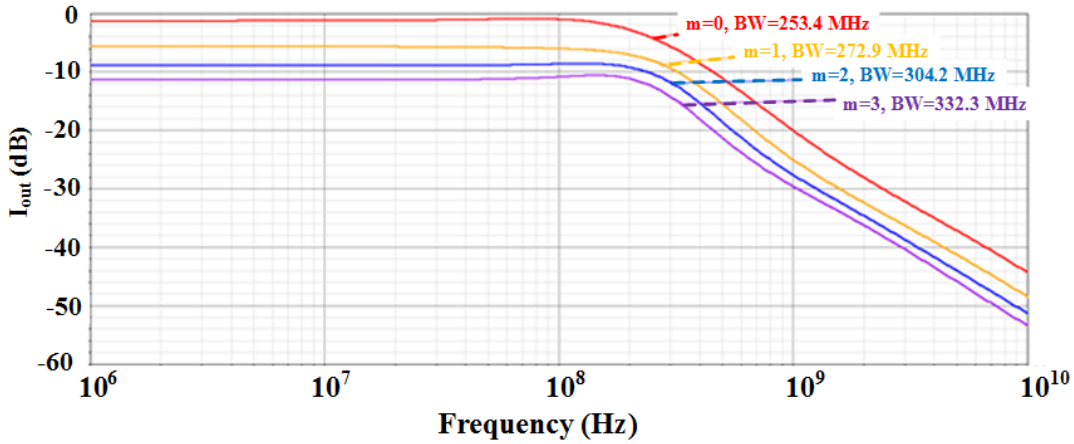

Fig. 8. Post-layout simulated AC response of the proposed multiplier for m=0, 1, 2, 3.

In order to develop a deeper understanding of the design, the effect of process fabrication, power supply and temperature variations on the circuit is studied through various simulations. The

simulation results of AC response at different temperatures for m=0 and m=3 are shown in Fig. 9. In these simulations I_X is swept as an AC current source and I_Y is set to 10µA and 40µA for m=0 and 3 respectively. The temperature is varied from -30°C to +70°C and the responses demonstrate high robustness over 100°C temperature variations.

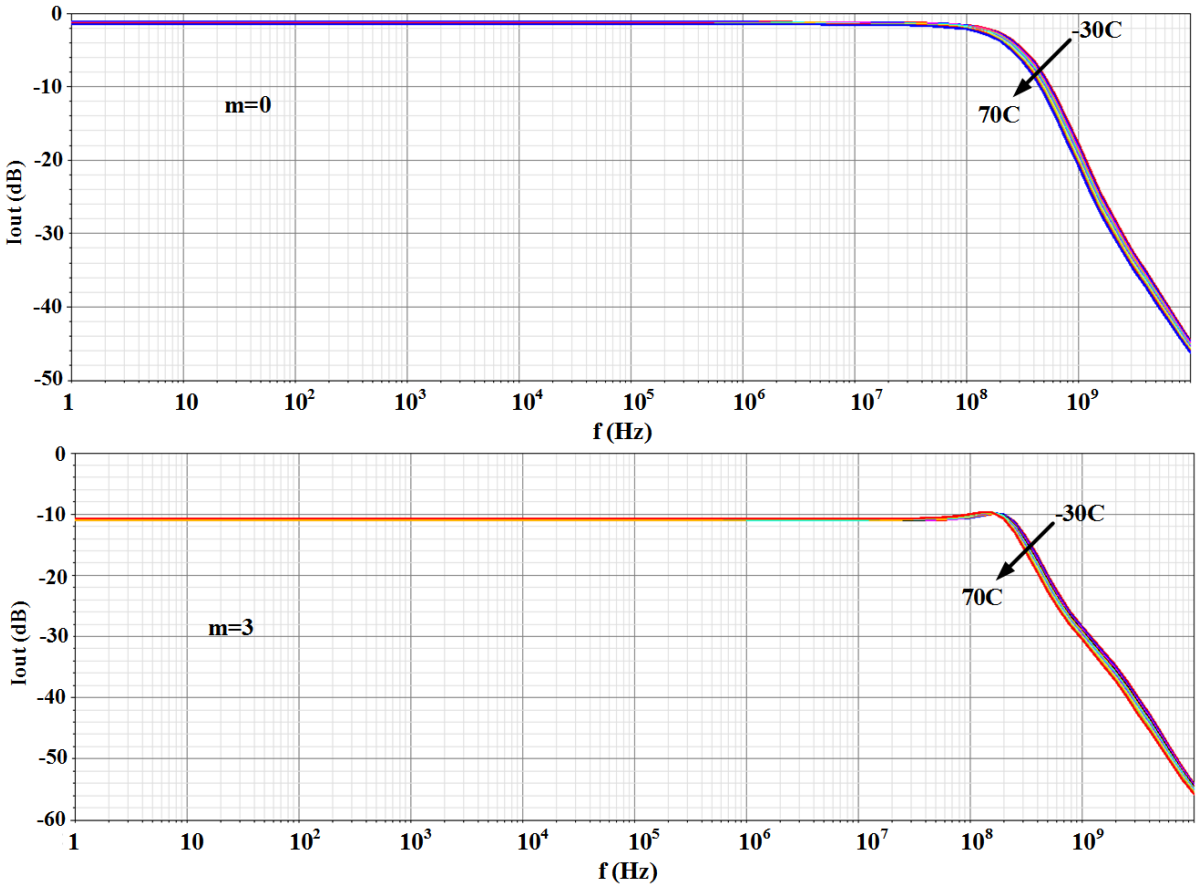

Fig. 9. Frequency response of the proposed multiplier versus temperature for m=0 and m=3

The effect of power supply variations on the output AC response is studied in Fig. 10, where the power supply is swept between 1.6V to 2V (±11% deviation from the nominal DC power supply value, 1.8V) for m=0 and m=3. The input setup for this test is the same as for temperature analysis. The results indicate that the circuit is highly insensitive to power supply fluctuations. This is achieved thanks to the advantages of using translinear based current squarers.

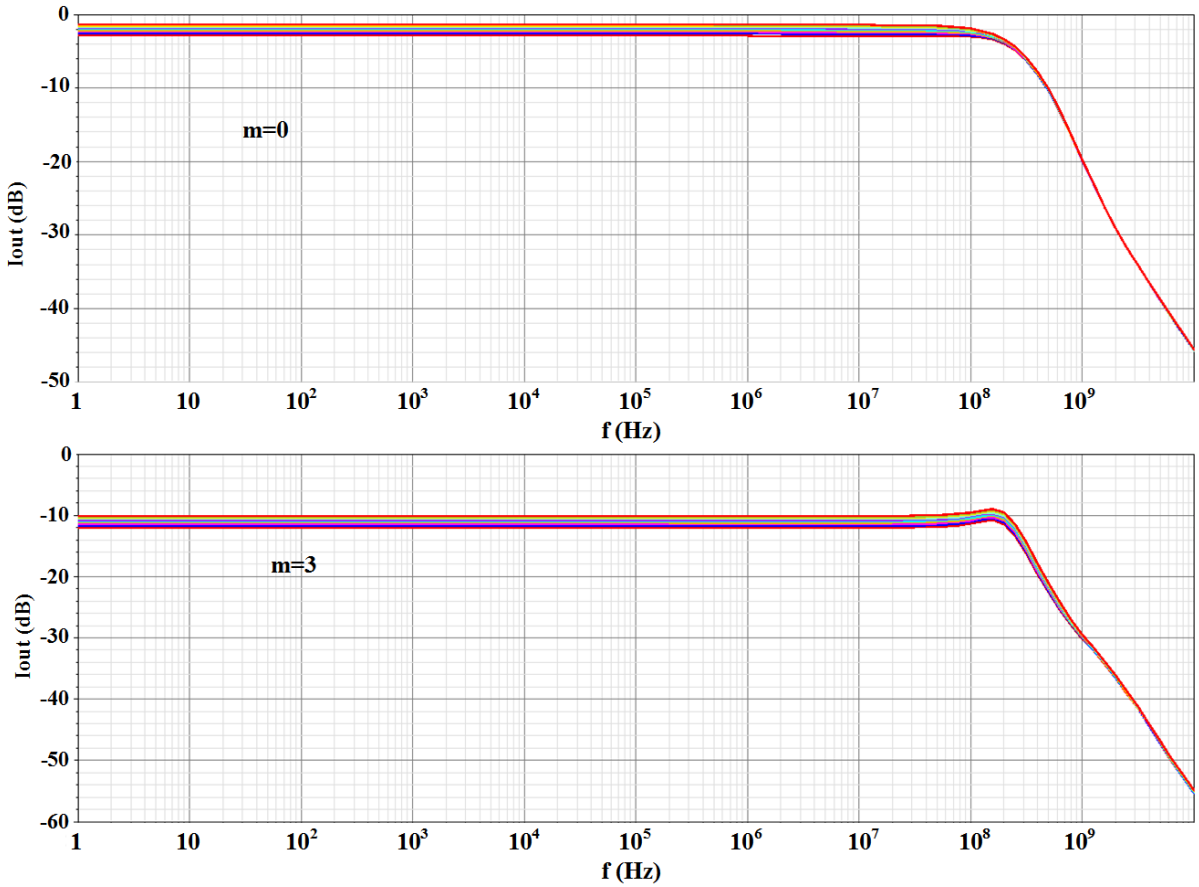

Fig. 10. Frequency response of the proposed multiplier versus power supply variations for m=0 and m=3

The effect of process corners in frequency response is shown in Fig.11. In this figure I_Y is set to 10μA and 40μA DC for m=0 and m=3 respectively while I_X is set as a small signal current. The AC response is simulated in fs, sf, ss and ff corners. The figure shows a high robustness against process variations (less than a 2dB difference over various corners in worst-case) which is achieved thanks to the pure independent current mode output.

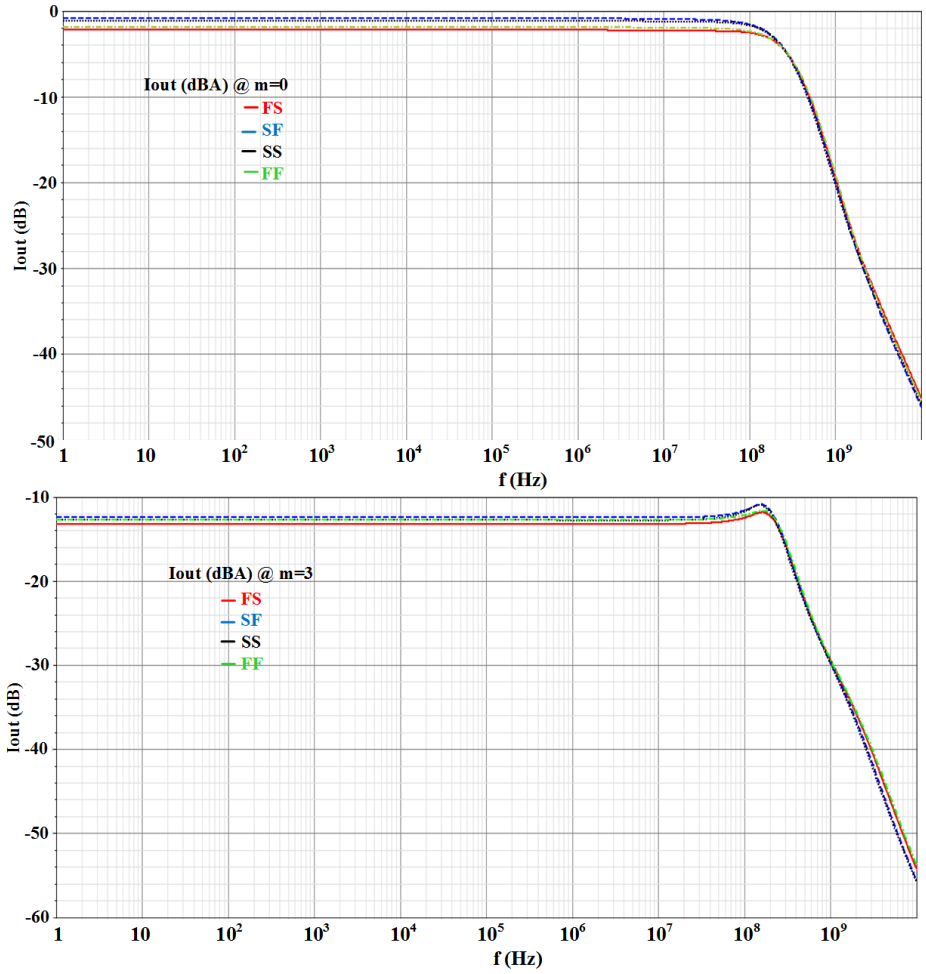

Fig. 11. Simulation of the frequency response for four different corners of sf, fs,ff and ss for m=0 and m=3

Monte Carlo analyses are carried out for bandwidth and total harmonic distortion to examine the robustness of the circuit against process variations and mismatches. All Monte Carlo simulations are performed with TSMC 0.18 µm model and based on the MC section of technology file for both process variations and mismatches.

Fig.12 shows the Monte Carlo analyses of total harmonic distortion of the circuit for 1000 simulations for m=0 and m=3. In this simulations, the amplitude of each input current is set to maximum ($10\mu A$ for m=0 and $40\mu A$ for m=3) at 1MHz frequency. The results demonstrate a mean value of 1.14 and 1.15 and a standard deviation of 0.05 and 0.07 for m=0 and m=3 respectively.

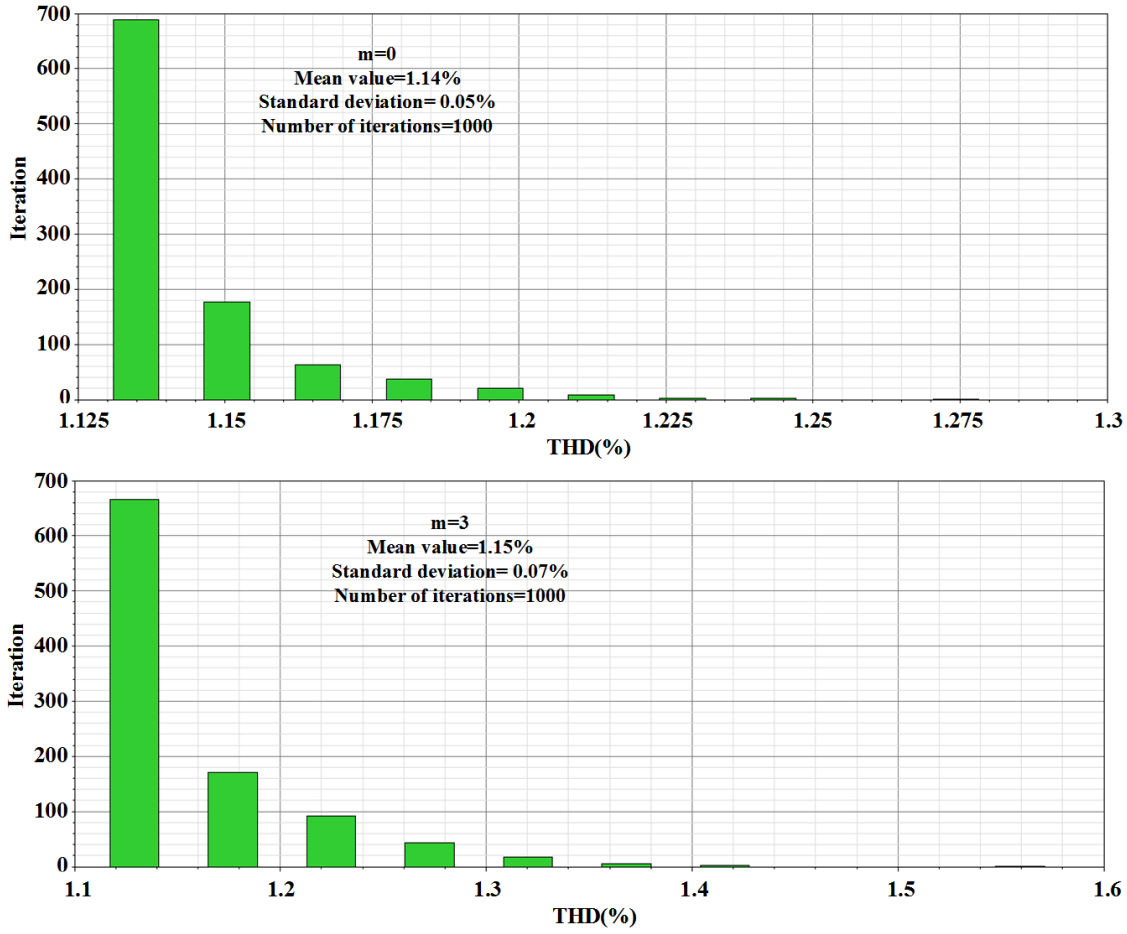

Fig. 12. Monte Carlo analyses of total harmonic distortion of the proposed multiplier for m=0 and m=3

The Monte Carlo analyses of -3dB bandwidth with 1000 iterations for m=0 and m=3 are shown in Fig. 13. The values of the currents are the same as in Fig. 8. The mean value is 255.5 MHz and 335.2 MHz and the standard deviation is 9.45 MHz and 7.42 MHz for m=0 and m=3 respectively.

From Figures 12 and 13 it can be deduced that the proposed circuit is highly robust against possible mismatches during manufacturing. This high level of robustness against mismatches is acquired thanks to the TL based design.

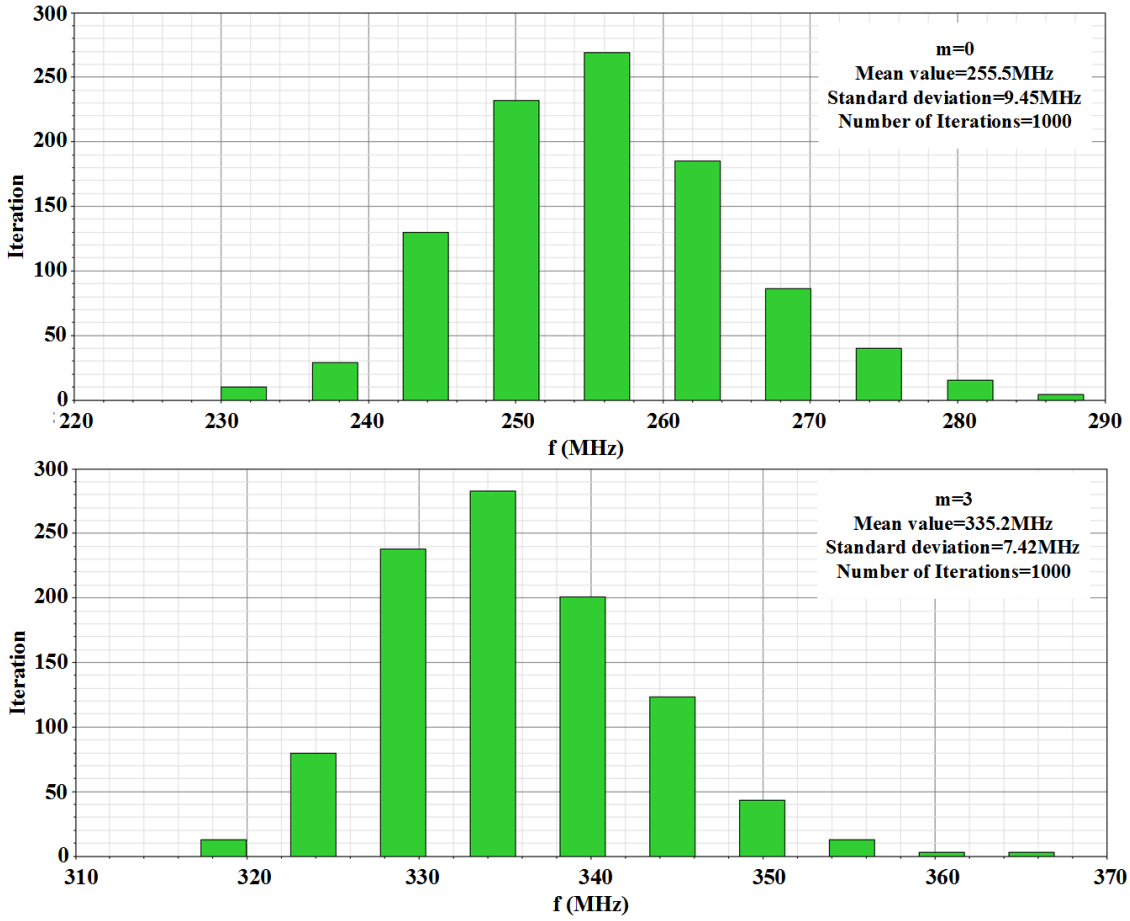

Fig. 13. Monte Carlo analyses of -3dB bandwidth of the proposed multiplier for m=0 and m=3

5. Conclusion

A new adjustable low power current-mode four-quadrant analog multiplier is proposed based on a new current squarer circuit. The circuit allows the designers to adjust the input range of the multiplier based on their own application without any increase in power consumption. The Post-layout simulation plus Monte Carlo analyses endorsed the functionality and robustness of the proposed multiplier against PVT variations. It is shown that THD and mismatch error of the circuit are reduced as 'm' is increased. The performance of the proposed multiplier is summarized and compared to the other recently published works in Table 2. The proposed multiplier is the only reported one to offer an adjustable input range while improving the linearity and robustness against PVT variations, yet keeping the bandwidth and power consumption at a reasonable level compared to the other reported multipliers in a similar technology.

Table 2. Summary of performance and comparison to prior works

Ref./Year	[22] /2003	[8] /2009	[23] /2010	[24] /2011	[9] /2012	[25] /2014		[15] /2015	[3] /2016	[11] /2017	This work
						Circuit1	Circuit2				
Tech. (µm)	0.8	0.35	0.5	0.5	0.25	0.18	0.18	0.35	0.18	0.18	0.18
Power (µW)	184	340	120	2000	168.1	60	75	232	89.2	150	186
THD (%)	0.9@ 1KHz	0.97@ 1MHz	0.63@ 10KHz	0.2@ 100KHz	0.91@ 1MHz	NA	NA	0.16 @1MHz	1.01@ 1MHz	0.8 @ 1MHz	1 @ 1 MHz
Supply Voltage (V)	1.5	3.3	3	3.3	2.5	1.2	1.2	2	1.8	±0.75	1.8
Bias current(µA)	6	10	10	40	10	40	40	4.6	10	10	10
Input range(µA)	12	±10	±10	±20	±10	0-10	0-10	±10	±20	±10	$\pm (1+m)\times 10^{m:0-3}$
BW (MHz)	5.5	41.8	18	3	278	79.6	59.7	485	840	300	332.3
Nº of quadrants	4	4	2	2	4	1	1	4	4	4	4
Sim/Meas	Meas.	Sim.	Meas.	Meas.	Sim.	Sim.	Sim.	Sim.	Sim.	Sim.	Post Layout+MC

6. Acknowledgments

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