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A Fully Integrated 4 x 2 Element CMOS RF Phased Array Receiver for 5G

--Manuscript Draft--

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Abstract:	This paper presents a fully integrated phased array receiver containing two four element Radio Frequency (RF) Beamforming (BF) receivers supporting two Multiple-Input Multiple-Output (MIMO) channels. The receivers are designed and fabricated using 45nm CMOS SOI technology. A 10 bit IQ vector modulator phase shifter (IQVM) is implemented in RF signal paths to control the phase and amplitude of the received signal before combining. Each IQVM provides 360 degree phase shift control and 17 dB gain variation. An off-chip, simultaneous high-Q impedance matching and bandpass filtering technique for each low-noise amplifiers (LNA) is presented using non-uniform transmission line (NUTL) segments. Measured downconversion gain at 100 MHz Intermediate Frequency (IF) and noise figure (NF) of a single path are 23 dB and 5.4dB, respectively, giving estimated 3.4 dB NF for a single element when simulated PCB and matching losses are taken into account. 1 dB compression and Input third-order intercept point (IIP3) are -37 dBm and -28 dBm, respectively. Each four-element receiver consumes 486 mW DC power from 1.2V power supply. Total area of two receivers is 5.69 mm2.

Point by Point Response to Detailed Written Comments and Suggestions on attached Paper

Dear Editor,

Subject: Submission of revised manuscript with responses to Reviewers' comments [ALOG-D-18-00069]

Thank you very much for handling and reviewing our manuscript. We also greatly appreciate the reviewers for their valuable comments and suggestions to our manuscript that will make our paper more focused, readable and easy to follow. Based on the reviewer's comments, we have revised the manuscript accordingly. Following are our responses given in point-by-point manner so that the respected reviewers can easily follow the changes and modifications made in the paper.

We hope that you find our responses satisfactory and our revised manuscript is acceptable for publication.

Sincerely,

Rana A. Shaheen, Rehman Akbar, Alok Sethi, Janne P. Aikio, Timo Rahkonen, Aarno Pärssinen

I. RESPONSE TO REVIEWER #1 COMMENTS

The manuscript describes nice design walk-through.

1- **Comment:** The motivation for moving up in frequency is clear, but why choose 15GHz when 5G starts at 24.5GHz? Please comment.

   Response: The design of discussed prototype was started in August 2015. At that time there was no clear information available about the specific frequency spectrum of 5G, i.e. 24G, 28 GHz or 38GHz, etc. More than 500 MHz bandwidth is available at 15 GHz band, which could be utilized in multiple 100MHz sub channels for multiple operators. In 2014, Ericsson and NTT Docomo also presented their work of achieving high data rate (5Gbps) communication at 15 GHz frequency band [1].

2- **Comment:** In the introduction, col. 1-line 37, it is stated that a "bandwidth of at least below...". This is a confusing statement and should be rephrased, presumably stating a "bandwidth of at least..."

   Response: Corrected

3- **Comment:** In the very beginning of section II.A it is stated that the system noise figure is benefiting from the array gain. This is not the case. The noise figure is independent of the array gain, and what is probably meant is that the system receiver sensitivity benefits from the array gain. Please correct this.

   Response: Corrected

4- **Comment:** At the end of the same paragraph, reference [8] is cited to explain NUTL segments. This should be [10].

   Response: Corrected

5- **Comment:** In section II.C, figure 4 sub figures c and d are swapped relative to the text. Please update and make sure text and figure correspond. Further, the figure label uses Quadrature selector (QS), whereas the text use vector selector (VS). Please be consistent, and check all occurrences of fig. 4 sub figure and VS references.

   Response: Corrected

6- **Comment:** Some acronyms are inconsistently written through out the text. E.g nmos/NMOS dc etc. Please be consistent and use upper case for acronyms.

Response: Corrected

7- **Comment:** In section II.A, just above section III.B there is a reference to fig. 1. It should be fig. 7.

Response: Corrected

8- **Comment:** A few lines from the beginning of section IV, there is an unresolved reference in the review PDF. Please check. It should perhaps be figure 8.

Response: Corrected

9- **Comment:** In section IV.A, the LO divider is discussed. As is well known, there is a 180deg. phase ambiguity after the quadrature divider. Please comment on how this is planned to be resolved for the two RX chains.

Response: We do agree with the reviewer regarding the need for phase synchronization, however, because of testing and measurement setup restriction, we had planned to measure each 4-channel Receiver independently. Thus, the lack of synchronization was not detrimental to the design. Moreover, in a communications system, digital signal processing will perform synchronization as well as MIMO channel estimation. That process will synchronize different MIMO paths and align phases taking into account radio channel as well as mentioned phase ambiguity.

10- **Comment:** The chip photograph in figure 16 is not very clear. Maybe you could zoom in on some of the details to highlight layout details.

Response: New Figure added, i.e. Figure 16 (b).

11- **Comment:** In section V the measured linearity results are mentioned. IIP3 appears to be rather low. Please add a discussion on why this is the case and what is the limiting factor.

Response: Discussion added in section V, also copied here.
"IIP3 measurements were taken from the entire single channel with maximum gain settings of all active blocks, i.e. LNA, S2D, buffers and VGAs in phase shifter. From AC analysis in spectre simulation tool (Virtuoso), it has been found that at the input of phase shifter (as shown in Fig. 1), cumulative voltage gain from preceding stages is ~19dB, and phase shifter appears to be the dominant contributor for non-linearity."

12- **Comment:** In the beginning of the last paragraph of section V, the NF is discussed. It is stated that NF is 5.4dB without PCB losses. This should probably be "including PCB losses" to be consistent with the estimated 3.4dB a few lines down.

Response: Corrected

13- **Comment:** Reference [8] appears to be identical to reference [19].

Response: Corrected

14- **Comment:** Neither reference [18], nor [19], are quoted in the text. For reference [19], this can be explained if it should be [10], which is quoted, but [18] should either be removed or quoting text be added at the appropriate place.

Response: Both of [18] and [19] are removed.

II. RESPONSE TO REVIEWER #3 COMMENTS

This paper describes a phased array receiver proposal which also supported with fabricated chip and measured results. It is well written and well organized. In my opinion this paper can be accepted for publication with minor modification to the text. Please see the comments below:

1- **Comment:** Abstract l.20 : Abbreviation IIP3 should be defined before use.

Response: Definition of IIP3 abbreviation is added in abstract

2- **Comment:** p.1 l.37 c.1, rephrase the sentence: "bandwidth of at least below hundred MHz" to, for example, "bandwidth of up to hundred MHz"

Response: Corrected

3- **Comment:** p.2 l.55 c.1, "nmos" in capital

Response: Corrected

4- **Comment:** p.4 l.6 c.1, rephrase the sentence: "with resonance control is for summing..."

Response: Corrected

5- **Comment:** p.5 l.42 c.2, citation has a problem: "Moreover, the distribution of LO is done at 30GHz as shown in Error! Reference source not found.."

Response: Corrected

6- **Comment:** Table I, last page, performance comparison, is not mentioned anywhere in the text. Since this is the conclusion of your study it makes sense to dedicate a paragraph to elaborate on the pros and cons of your achieved performance, comparing to other reported similar designs.

Response: Paragraph added and copied below.
"Table 2 shows comparison results of the work with the state of the art designs in cm-wave and mm-wave frequencies. As active configuration of phase shifter is used, therefore, this work outperforms in terms of area, but at the cost of power consumption and lower values of compression points."

7- **Comment:** Fig.12 has a table also captioned as Table I.

Response: Corrected

III. REFERENCES

[1] J. Gozalvez, "Prestandard 5G Developments [Mobile Radio]," *IEEE Veh. Technol. Mag.,* vol. 9, no.4. pp. 14-28, Dec. 2014

Article Title Page

Article title: A Fully Integrated 4 x 2 Element CMOS RF Phased Array Receiver for 5G

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Abstract— This paper presents a fully integrated phased array receiver containing two four element Radio Frequency (RF) Beamforming (BF) receivers supporting two Multiple-Input Multiple-Output (MIMO) channels. The receivers are designed and fabricated using 45nm CMOS SOI technology. A 10 bit IQ vector modulator phase shifter (IQVM) is implemented in RF signal paths to control the phase and amplitude of the received signal before combining. Each IQVM provides 360 degree phase shift control and 17 dB gain variation. An off-chip, simultaneous high-Q impedance matching and bandpass filtering technique for each low-noise amplifiers (LNA) is presented using non-uniform transmission line (NUTL) segments. Measured downconversion gain at 100 MHz Intermediate Frequency (IF) and noise figure (NF) of a single path are 23 dB and 5.4dB, respectively, giving estimated 3.4 dB NF for a single element when simulated PCB and matching losses are taken into account. 1 dB compression point and Input third-order intercept point (IIP3) are -37 dBm and -28 dBm, respectively. Each four-element receiver consumes 486 mW DC power from 1.2V power supply. Total area of two receivers is 5.69 mm^2.

Keywords: CMOS SOI, RF, mmWave, beamforming, receiver, input matching, phased array, LNA, phase shifter, mixer, vector modulator, wireless communication, 5G

A Fully Integrated 4 x 2 Element CMOS RF Phased Array Receiver for 5G

Rana A. Shaheen, Rehman Akbar, Alok Sethi, Janne P. Aikio, Timo Rahkonen, Aarno Pärssinen

Abstract— This paper presents a fully integrated phased array receiver containing two four element Radio Frequency (RF) Beamforming (BF) receivers supporting two Multiple-Input Multiple-Output (MIMO) channels. The receivers are designed and fabricated using 45nm CMOS SOI technology. A 10 bit IQ vector modulator phase shifter (IQVM) is implemented in RF signal paths to control the phase and amplitude of the received signal before combining. Each IQVM provides 360 degree phase shift control and 17 dB gain variation. An off-chip, simultaneous high-Q impedance matching and bandpass filtering technique for each low-noise amplifiers (LNA) is presented using non-uniform transmission line (NUTL) segments. Measured downconversion gain at 100 MHz Intermediate Frequency (IF) and noise figure (NF) of a single path are 23 dB and 5.4dB, respectively, giving estimated 3.4 dB NF for a single element when simulated PCB and matching losses are taken into account. 1 dB compression point and Input third-order Intercept Point (IIP3) are -37 dBm and -28 dBm, respectively. Each four-element receiver consumes 486 mW DC power from 1.2V power supply. Total area of two receivers is 5.69 mm^2.

Keywords—CMOS SOI, RF, mmWave, beamforming, receiver, input matching, phased array, LNA, phase shifter, mixer, vector modulator, wireless communication, 5G

I. INTRODUCTION

Recently, introduction of new wireless concepts such as “internet of things (IoT)” and enhanced live stream videos (video on demand) has opened a need of exponential rise in wireless devices and spectrum need. Minimum peak data rate requirements for future wireless communication systems, i.e. 5G [1], are set to be 10 Gbps. Higher order modulation schemes, e.g. 64 QAM, 128 QAM or 256 QAM, are used to achieve high data rates, which poses tough requirements for signal to noise ratio (SNR). To achieve higher SNR, bandwidth of at least hundred MHz is required. Wireless spectrum lower than 6 GHz is highly crowded with existing standards and there is not enough bandwidth available. One practical solution is to occupy higher frequencies with less crowded spectrum, which can offer the required network capacity than currently available. Therefore, millimeter wave frequencies are being considered for future communication systems.

One of the many possible scenarios for 5G architectures is the combination of multi standard and multi band systems. For example, use of low frequencies system for wider area coverage, mm-wave frequency systems for higher data rate links. Multiple antenna systems or phased arrays can provide the benefit of improvements in link SNR, i.e. array gain is used for compensating path loss at mm-wave frequencies, as well as beam steering capability for directivity. A 32-element and 16-element fully integrated RF beamforming architectures are presented in [2] and [4], respectively. Higher number of antennas, helps to improve link quality and long range but only for a single user scenario. In a dense environment where multiple scatterers and multiple users are present, a system, that can handle multiple streams simultaneously from different users, is inevitable. A MIMO system is fully capable of handling different spatial streams in more dense environments. A hybrid architecture of MIMO techniques and beamforming together can benefit improvements in link SNR as well as spatial filtering for multi-user environment at the same time. In [2], future wireless system for MIMO and RF beamforming is suggested for different communication link scenarios. It has been shown that non-coded data rate of 3 Gbps can be achieved using higher-order modulation schemes such as 256 QAM, which requires at least 33 dB SNR for 500 MHz bandwidth. However, with the use of multiple independent streams, the SNR requirements can be relaxed, e.g. a 4-5 Gbps data rate can be achieved with two MIMO channels using only 64 QAM modulation scheme, which requires reduced SNR of 25 dB [2].

Based on the position of phase shifting of received signal, different types of beamforming architectures are realized, e.g. RF path, LO path or baseband path phase shifting. RF path phase shifting and combining technique has the advantage of less complexity and lower power consumption, therefore, becoming a typical choice for implementation of CMOS receiver phased arrays. Various phased array architectures at cm-wave and mm-wave frequencies have been reported in literature [3], [4], [5]. In this paper, we present the implementation of integrated solution for RF beamforming receiver design supporting two MIMO channels in a single chip [6]. In addition to capacity, future 5G networks are expected to provide traffic density and spectral efficiency far beyond current radio systems. Therefore spatial filtering and side-lobe reduction are essential design criteria and necessitates amplitude tapering in addition to phase. Vector modulator phase shifters provide efficient means to control both phase and amplitude thus allowing calibration that can be managed both at the same time.

This paper describes a complete design and characterization of two-channel RF phased-array receiver implemented in 45nm CMOS SOI process. In Section II, the receiver design topology and key circuit parameters are explained. Input matching of high-Q input impedance of LNA is described in section III. Local Oscillator signal generation and distribution is discussed briefly in section IV. Measurement results and performance parameter tables are

presented in section V. Section VI and VII include chip measurements and conclusions, respectively.

II. ARCHITECTURE AND CIRCUIT DESIGN

The proposed hybrid beamforming system consists of two identical RF beamforming receivers for digital MIMO processing [6]. Each receiver supports four individual antenna elements with phase shifting and combining the received signals in the RF domain. Block diagram of the designed system is shown in Fig 1. Each RF element consists of a low noise amplifier (LNA), an active single-ended-to-differential converter (S2D) and active phase shifter. Instead of power combining using very large Wilkinson combiners, current mode combining technique is utilized, before the RF signal is downconverted to baseband (BB) using a Gilbert cell mixer. An external 30 GHz local oscillator (LO) signal is used, which is divided by 2 locally to provide 15 GHz LO signal for IQ downconversion. Digital control provides extensive means to control different gain settings, bias control, RF response tuning, phase, etc. Simultaneous input matching and bandpass filtering of LNA is implemented off-chip using NUTL segments.

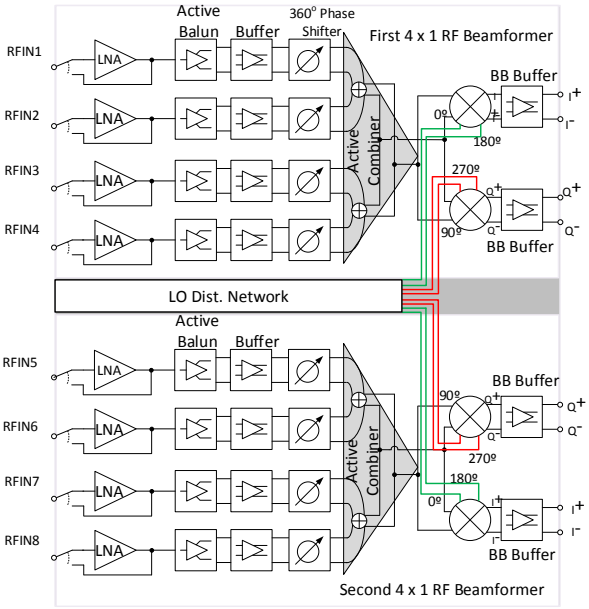


Fig 1: System Block Diagram

A. Low Noise Amplifier

LNA is the critical block in terms of total noise figure and sensitivity of the receiver. In phased array receiver systems, sensitivity of the complete system also gets benefit from the array gain of the phased array, which relaxes the requirements for achieving low noise figure [5]. As a result, a tradeoff can be made in terms of noise figure, linearity, power consumption and filetring. Due to the fact of its built-in filtering and matching conditions, common-source cascoded inductively degenerated (CSID) source topology is utilized for LNA design [7], shown in Fig 2. Source inductance of CSID LNA is selected such a way that it helps in canceling out the intrinsic capacitances of the input transistors, i.e. Cgs, and makes the input impedance of the transistor more real which can then be rotated to the centre of the smith chart to match with 50 Ohm source impedance. Parasitic capacitances from electrostatic discharge (ESD) diodes and input pads, introduce additional reactance at the input. This leads to relatively high Q impedance seen by 50 Ohm source port and needs additional gate inductance to cancel the parasitic capacitances. Instead of implementing gate inductance on-chip, external matching circuit is implemented with the help of NUTL segments [8].

In case, if high blocker signal is received at the input, drain of an NMOS transistor is connected in the signal path, which bypasses the input signal directly to next stage, hence reducing gain and improving linearity. Size of the switch is optimized for minimum off-capacitance to have minimal impact on actual input matching of the LNA. A resonance tuning control is realized with PMOS switches, which turn off/on unit capacitance to output load, changing the resonance of the load.

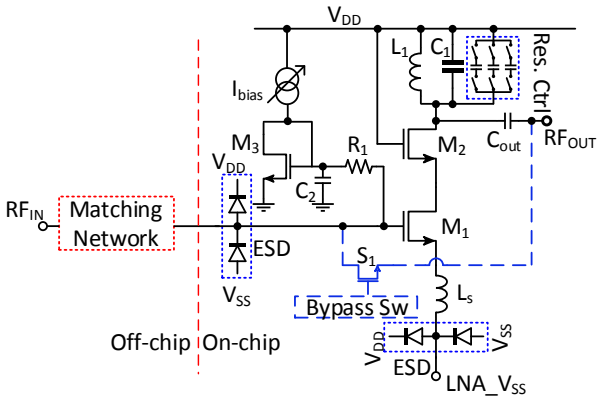


Fig 2 Common-source cascoded low noise amplifier

B. Single-ended to Differential Converter

Active balun circuit for low frequencies has been reported e.g. in [9]. Parasitic components appearing at critical nodes makes the design more challenging at 15 GHz, with minimum phase and gain errors in the output signal. In this work, a gain-boosting current-balancing balun circuit topology [9] is selected as a baseline for single to differential signal converter as shown in Fig 3.

S2D circuit is composed of two stages: common gate-common source (CG-CS) M1-M2 input stage for gain boosting and the output current is then balanced by CG devices M3 and M4 with cross coupled input also called differential current balancer (DCB). All the devices M1-M4 are of equal sizes. A resistive feedback inverter amplifier (X_1) is used to self-bias M1 and M2. A two-step resistive attenuator is implemented at the output. A center-tapped coil is used as a load and for tuning the frequency response at 15 GHz. Resonance tuning is also implemented in this block.

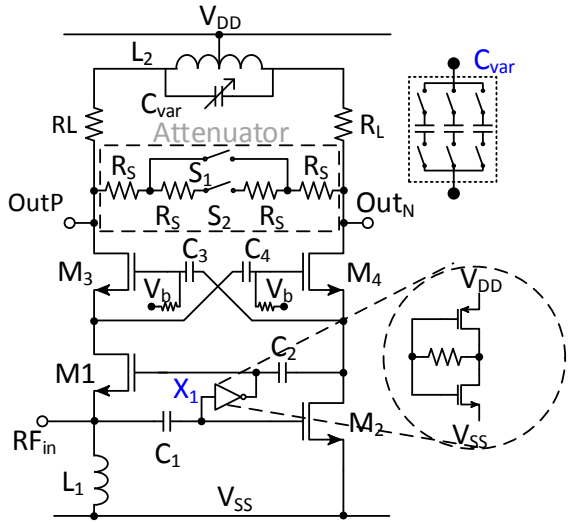


Fig 3: Single-ended to differential converter

C. IQ Vector Modulator Phase Shifter

RF phase shifter (PS) is the core block of RF phased arrays. Passive structures such as reflection-type PS and switched-line PS are demonstrated in [3] and [5], respectively. Passive phase shifters are linear and accurate in terms of phase error, but area can be large and loss is unavoidable. Active PS, such as, Vector modulator (VM) phase shifter provides compact size, better noise performance and opportunity to tradeoff with linearity using appropriate gain partitioning in internal amplifiers.

Active digitally controlled 10-bit vector-sum phase shifter topology is used in this work, which provides in total 1024 points in phasor plot in all four quadrants. Block diagram of the phase shifter is shown in Fig 4. A differential signal is split into four quadrature signals with the help of passive poly-phase filter. Each quadrature differential signal is then weighted individually with the help of a Variable Gain Amplifier (VGA), and the output currents from I and Q branches are summed up to form a resultant vector with particular phase. A quadrature selector is used for switching the quadrants of the resultant vector to implement full 360°.

1) Quadrature signal generator

Quadrature distribution of the input signal has been the major and critical building block for different RF applications. There are few topologies for distributing the input signal into its quadrature signals, e.g. poly phase filter, quadrature hybrid, frequency dividers and quarter wave length transmission lines. Among these topologies, quadrature hybrid and quarter-wave transformer are passive structures which are used because of their linear behavior in the signal path, but they are lossy and very large in size at 15 GHz. Frequency dividers are used to generate quadrature signals in LO distribution circuits. They are completely nonlinear devices and cannot be used in the signal path for phase shift. A poly phase filter (PPF) topology is used in LO/RF IQ generation to support direct conversion receivers. They are compact in size and if layout is properly drawn show good performance in respect of amplitude and phase variation. A wider bandwidth can be achieved by using multiple cascaded stages of PPF. An RC poly-phase filter topology, shown in Fig 4 (c), is utilized for quadrature generation due to its compact area. To achieve balanced signal at the output careful symmetrical layout is implemented.

2) Vector Selector

Differential I and Q vectors can sweep the amplitude and phase of the input signal for 180° phase shift. To achieve the full 360° phase shift, a quadrature selector or differential sign inversion block is required. Circuit diagram of vector selector (VS) is shown in Fig 4 (d). NMOS devices are used as switches by biasing the sources and drains of the transistors with local ground connections. On-resistance of the switch contributes the loss but off-capacitance also contributes the resonance variation of the poly-phase filter. Switch sizes are optimized to achieve minimum on-resistance and off-capacitance. To isolate or minimize the switching behavior of the VS, a dc coupled differential amplifier is used between PPF and VS. A digital control bit is used to select the set of the transistors at a time, i.e. in Fig 4 (d), bit b1 turns on M1 and M4, while inverse of b1 is applied to completely turn off M2 and M3.

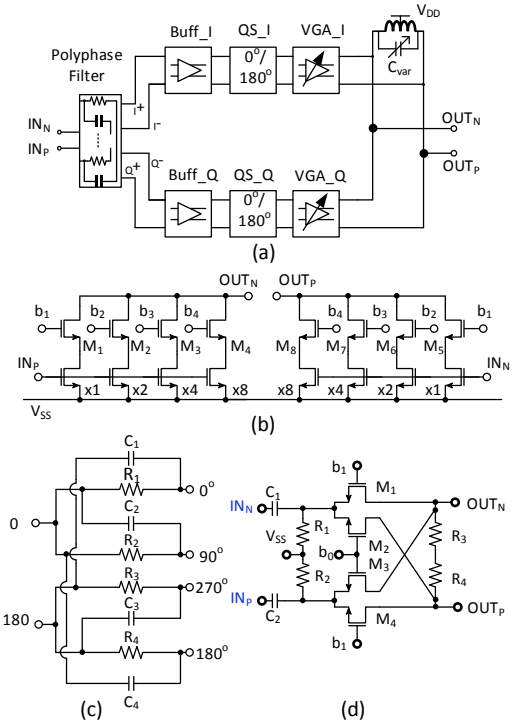


Fig 4: (a) Vector modulator architecture, (b) Variable gain amplifier (c) RC Polyphase filter (d) Vector selector (VS)

1) Variable Gain Amplifier

Amplitudes of I and Q branches of the IQVM are controlled and combined to achieve desired resultant vector, which as a result provides a unique phase and amplitude set to the input signal. In [5], a phase inverting variable gain amplifier is used in BiCMOS process at 60 GHz. A variable

gain amplifier (VGA) is used to control the amplitudes of the I and Q branches individually, as shown in Fig 4 (b). Because of limited supply voltage, i.e. 1.0 V, we used Common-source NMOS transistors as inputs with cascode connection of NMOS switches to digitally control RF current of binary weighted devices. The differential currents from both I and Q branch VGAs are combined with the help of center-tapped coil with resonance control.

D. Antenna Signal Path Combining

Wilkinson combiner is commonly used at mm-wave frequencies. However, at 15 GHz, integrated λ/4 TLs are very large and therefore, impractical to implement on chip. In large phased array systems, architecture affects gain budget and thus linearity and NF of the whole receiver. Wilkinson power combiners were utilized in [4], while a combination of a passive and active combiners were demonstrated in [5] for 16 elements.

Due to compact size at 15GHz operation a two-stage current combining is implemented in this work using first a parallel differential pair with fixed tail current topology, as shown in Fig 5 (b), which provides sufficient isolation from the other paths to avoid loading effects. In the second stage, output currents of the active combiners are summed using a narrowband LC load with low ohmic metal wires. A center-tapped coil is used for supplying DC power to these two combiners and resonate out the wiring capacitances at center node.

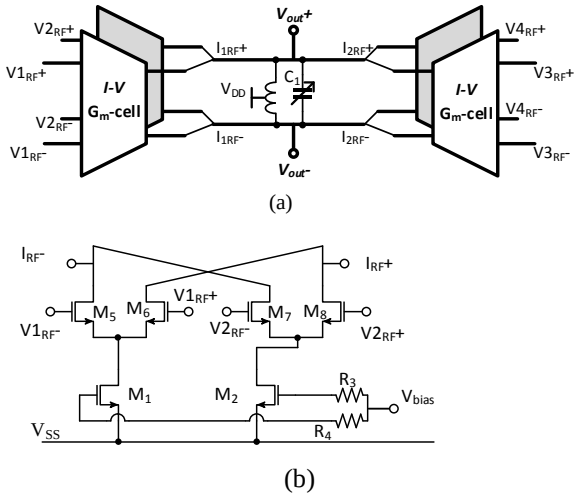


Fig 5: (a) 4 to 1 Active current combiner, (b) 2-1 V-I Gm-cells

E. Current Bleeding Mixer and IF Amplifier

Mixer schematic is shown in Fig 6. A Gilbert cell type double balanced current reuse topology [10] is used for two mixers, i.e. for I and Q outputs. Mixer input part is composed of a NMOS and PMOS pair connected in cascode, biased separately from bias blocks. Input RF signal is AC coupled from previous stage and both input devices are also AC coupled from each other. Conventional divide-by-two approach is used to generate I/Q signal from externally generated 30GHz LO signal.

Differential amplifier with resistive feedback is used for buffering the output at baseband. Longer channel length of the output devices is possible due to limited BW up to few hundreds of MHz. The pull up coils of the baseband amplifier are placed off-chip with external balun package.

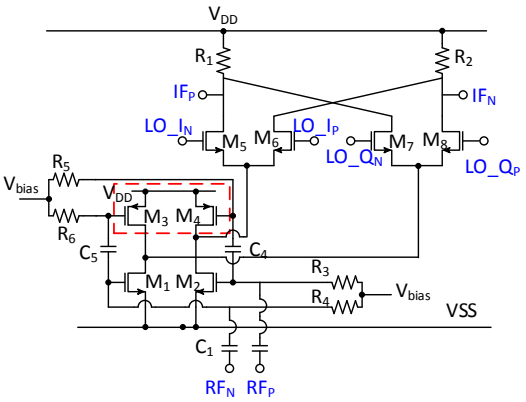


Fig 6: Downconversion Mixer

III. INPUT MATCHING DESIGN

Source inductance of the CSID LNA helps to remove effects of reactive part of the intrinsic input capacitance of the input transistor of LNA, which in turns makes the input matching process easier. However, if parasitic capacitances, mainly due to the wiring components from the structures such as electrostatic discharge (ESD) diodes and IO pads are not taken carefully into account, the LNA input impedance typically appears to be highly reactive resulting in high-Q impedance. That makes impedance matching over the wider BW very complicated. In [8], a method of matching the high-Q impedance for a wide BW of 1.2 GHz at 15 GHz (relative BW of 7%) using NUTL segments is presented. In this design, cancellation of reactive part of the input impedance was not implemented on-chip. In this work, we utilize the opportunity to use external wideband matching technique using NUTLs for matching relatively high-Q input impedance of phased array inputs. RF inputs of all eight elements are matched at 15 GHz using the NUTL segments topology, which are compact in size and provides additional benefits of bandpass filtering.

All eight elements placed next to each other are implemented in IC on the same edge. For PCB characterization, the chip is attached to PCB as a flip chip via solder bumps. Area of each pad is 100 um x 100 um and the pitch between two consecutive RF IO pads is 190 µm. A 0.1mm wide transmission line is needed to feed the signal to the input of the LNA. A four-layer PCB was used with the material characteristics of εr = 2.99 and losstan δ = 0.0017. Total thickness of PCB is 0.43 mm resulting in the linewidth of 230 um (50 Ω) with the top metal. Impedance matching of a single receiver at center frequency of 15 GHz is achieved in three steps, discussed as in details in [8].

A. Transformation of Capacitive Reactance

At the targeted centre frequency, the input impedance at input pad of LNA appears to be highly capacitive, as shown

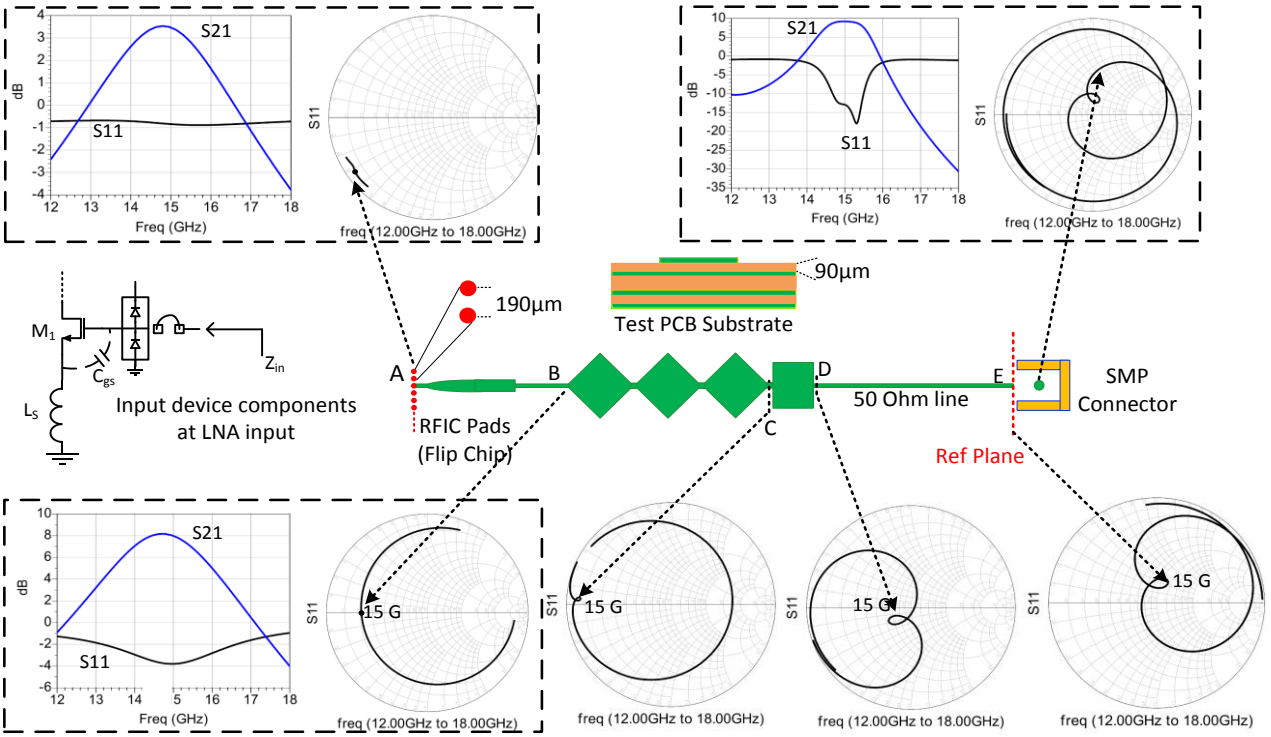


Fig 7: Schematic of input device with the design procedure of impedance matching line showing S11 and S21 (Simulations) graphs at key interfaces [8]

in Fig 7 by point 'A'. In order to cancel the reactance, the initial TL with the width of 0.1mm together with a tapered-line is provided. The long taper line at the beginning is mandatory as it spans out the inputs, providing sufficient space between them. The main goal of the initial transformer is to transform the reactive impedance close to low ohmic real plane on the Smith chart, shown in Fig 7: Schematic of input device with the design procedure of impedance matching line showing S11 and S21 (Simulations) graphs at key interfaces Fig 7 by graphs at point 'B'.

B. Taper-Line Diamond Segments for Multiple Resonances

This part is the core of the matching circuit. A λ/4 long single segment rotates the impedance of targeted bandwidth into a circle as shown by graphs at interface 'C' in Fig 7. By adding multiple sections, the impedance circle is narrowed so that it can be later on shifted to the center of the Smith chart. Three segments are used, which results in two rotations of impedance points in the Smith chart. One diamond-shaped segment is realized by combining two taper lines. The characteristic impedance of the segment varies linearly from 50 Ω to 8 Ω and again back to 50 Ω.

C. Impedance Transformer for Shifting Resonance

The purpose of this section is to transform the impedance response to the centre of the Smith chart. This is carried out with the impedance step transformers starting with a λ/8 line segment (Z0 of 10 Ω), which provides rotation in the impedance response at frequencies of interest (plot at interface 'D' in Fig. 1). A 50 Ω TL is used until interface 'E' (reference plane for connector model) in Fig 7, which rotates frequency impedance points in counter-clockwise direction, i.e. towards center. Finally, connector model is added (plots at connector interface in Fig 7. This rotation of S11 around center, provides bandpass-type response in S11 and S21 plots as shown in Fig 7 at connector interface.

IV. LO DISTRIBUTION AND I/Q PHASE GENERATION

Divide-by-two approach is used to generate I/Q signal at 15GHz. Each receiver has its local frequency divider and inverter based driver. Moreover, the distribution of LO is done at 30GHz as shown in Fig 8. External waveform generator provides single ended signal and on chip active balun (S2D) is implemented to have differential signal. Line drivers placed in distribution network to compensate the

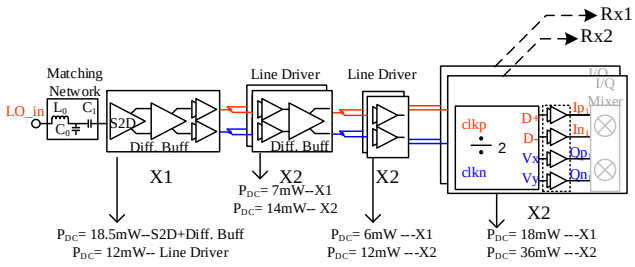


Fig 8: LO distribution block diagram

distribution losses. The strength of LO signal at 30GHz

depends on the minimum input voltage required to drive the frequency divider.

A. *LO Frequency Division*

Current-mode logic (CML) allows achieving the fastest operation speed, compared to e.g. true single-phase clocked (TSPC) or digital CMOS logic. The advantage of using static frequency divider, it can operate up to 40GHz without using LC load [11], [12]. Which allows using them for local generation of I/Q for each receiver and reduce the overhead of wiring.

The divided by two operation is realized using a D-type master-slave flip-flop, consisting of two cascaded D-latches shown in Fig 9. The cross connection between the output of the slave latch and the input of the master causes the clock frequency to be divided by two. During one half of the clock period the M1 and M2 are activated, and the voltage is "sampled". Simultaneously, in the first half of the clock period the latch transistors of the M9 and M10 are activated and the state of M7 and M8 is "held". In the second half of the clock period, the operation is inverted - the M7 and M8 are activated and "sample" the state presented by M3 and M4 that simultaneously "hold" the previous sampled state.

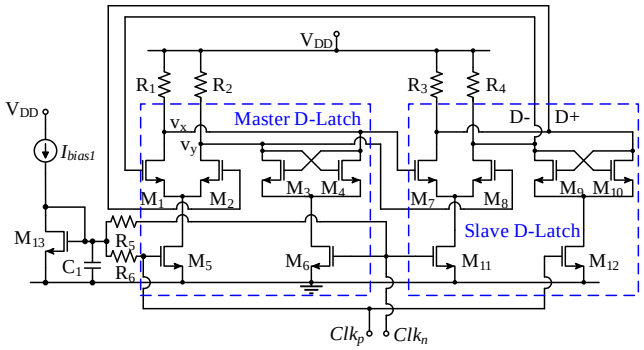


Fig 9: CML divide-by-2 frequency divider

The speed of operation strongly depends on input clock transistors (M5, M6, M11 and M12), as the size is made smaller, large differential voltage required at the input of differential pair (M1, M2, M7 and M8) for the current to be fully switched. The size of cross coupled pair (M3, M4, M9 and M10) determines whether divider will self-oscillate [13]. This depends upon the gm of cross-coupled pair, the divider will oscillate if gm R >1. In addition, smaller the size of cross-coupled pair, divider would achieve higher speed of operation. The sizes of transistors are selected according to the conditions as explained above. The size of differential pair transistors are 16.8µm, cross-coupled pair transistors are 12.6µm which gives gm = 10mS and input clock transistors are 21µm, using length L=56nm. The resistors R1-R4 are 170Ω.

The sensitivity curve of frequency divider gives the minimum input amplitude Vmin of the fclk, for which the divider functions properly. The simulated sensitivity curve shows in Fig 10, defines minimum 30mVp required at 30GHz for divide-by-two operation.

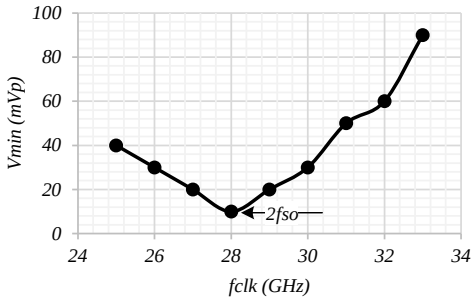


Fig 10: Sensitivity curve of frequency divider

The I/Q phase generation can be realized by taking the output from Vx, Vy (Ip and Im) and D+,D- (Qp and Qm) node. The generated I/Q signals swing is not rail-to-rail; to generate rail-to-rail signals inverter based buffer is implemented, shown in Fig 11. First stage of buffer is having feedback resistor to bias inverter at half of voltage supply (VDD =1Vdc), which ensure the switching of following inverter stages. The transistor sizing of buffer in Fig 11 are according to LO switching transistors of I/Q mixer. The sizes of PMOS and NMOS transistors in inverter stages are same and buffer for Ip and Im are same. M1 =4µm, M3 = 6µm, M5 = 9µm, M7 = 16µm and R1 = 5.8kΩ.

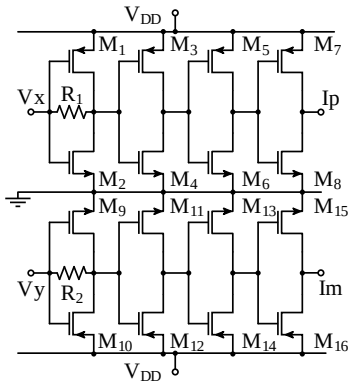


Fig 11: Buffer for driving I/Q mixer

The frequency divider combined with I/Q mixer buffer is simulated using I/Q mixer as load. The results shown in Fig 12 are post simulation results. Table 1 in Fig 12 shows the output parameters, when minimum input amplitude voltage Vmin is applied at 30GHz at clkp and clkn with the phase difference of 180°.

B. *Active Balun*

Frequency divider needs a differential input signal and external waveform generator provides single-ended output. Moreover, differential conversion at 30 GHz is rather easy when implemented on-chip. The configuration of balun circuits can be passive or active. The passive balun has the compact size at high frequency (e.g. 60GHz), but introduces signal loss at each differential path [14]. The active balun is

more attractive because it not only creates differential output but provides conversion gain.

Table 1: Divider Output parameters

Parameters	Value
I/Q (p)-Phase	88.92°
I/Q(m)-Phase	269.2°
Rise time	6.3psec
fall time	5.8psec
fout	15GHz
Duty cycle	49%
Output swing	1Vpp
Power	18mW

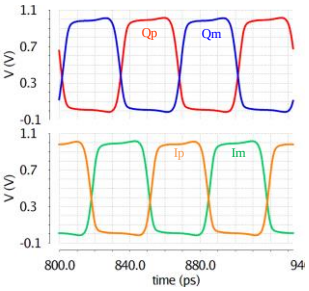


Fig 12: Transient waveforms and output parameters of frequency divider

Combination of common source-common gate amplifiers (CS-CG) amplifier, single transistor splitting (CS with degeneration), and differential amplifier with single-ended input are the conventional way to implement the balun circuit [14], [15] and [16]. The above mentioned topologies are very sensitive to parasitics at frequencies above 20GHz, which introduce high gain (±2dB) and phase error (180°±10°) [15]. In fact, the gain error and the phase errors are not independent [14], [15] and [16]. Therefore, gain and phase errors have to correct simultaneously.

Fig 13 shows the implemented active balun at 30GHz [16]. This topology used two balun circuits, balun-A consisting of transistor M1 and M2 followed by two balun-B circuits consisting of transistor M3, M5 and M4, M6. Balun-A (CS-CS amplifier) is used to create the differential signal and balun-B is used to correct the phase and gain error. The circuit can achieve the resonance tuning range 32.5 to 28.5GHz (see Fig 14)

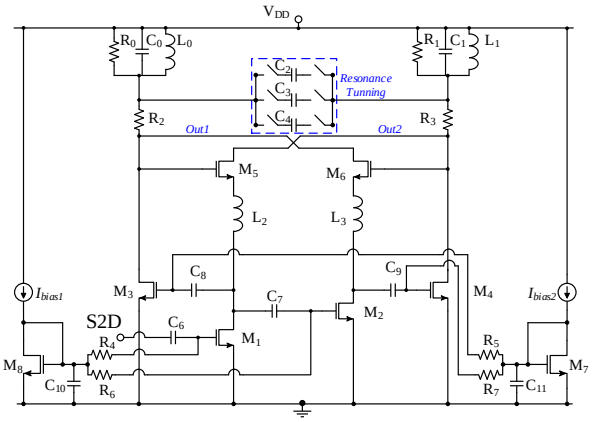


Fig 13: Active Balun Schematic

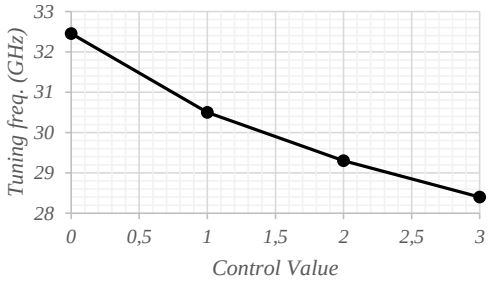


Fig 14: Tuning frequency range of resonance control of frequency divider

V. Experimental Results

Measurement setup to characterize the phased array IC is shown in Fig 15. IC is flip-chipped directly on the PCB using solder bumps to minimize parasitics. In an unpackaged flip-chip, the chip pad areas dictate the pitch of the PCB as well. IO pad pitch is 190 µm with the pad area of 80 um x 80 um. Due to PCB manufacturing limitations, a maximum width of 100 um wide transmission line can be used to feed the signal lines to the input of the LNA near the chip and afterwards can be tapered to wider widths. The four-layer PCB by Isola Astra MT77 was used with the material characteristics of ε_r = 2.99 and losstan(δ) = 0.0017. The total thickness of top layer of PCB is 0.09 mm resulting in the linewidth of 230 um (50 Ω) using the top metal. Test chip is manufactured using 45nm CMOS SOI technology. Fig 16 shows the micrograph of the manufactured chip of the complete 4 x 2 phased array, with all the RX inputs placed next to each other on the same edge of the IC. The core area is 3.95 x 1.44 mm^2 including pads.

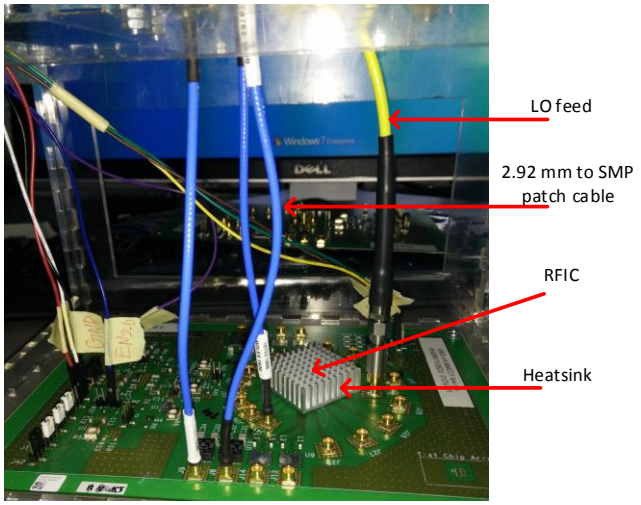


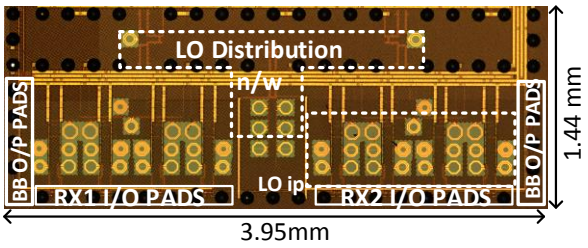
Fig 15: Measurement setup for the IC

Calibration of the measurement cable was performed using electronic calibration (N4694A ECal) module provided by Keysight Technologies. Effects of connectors and cables upto PCB connectors were calibrated out. Input impedance of each LNA feed is designed to 50 Ohm source impedance using NUTL segments [8], which provides the opportunity of simultaneously input match and band pass filtering. Measured input impedance matching (S11) of a single receiver at centre frequency of 15 GHz is less than -10 dB. Conversion gain measurements were performed using a vector network analyzer (VNA) using frequency converter option, which requires calibration of measurement setup at two different frequencies at the input and output of the receivers. Cold source method [17] using spectrum analyzer is used for measuring noise figure (NF) of a single RX chain while other chains are switched-off. A single RX element provides a maximum conversion gain of 23 dB at 14.9 GHz, which is 2 dB less than estimated in post-layout simulations. Single chain RF response and S11 curves are shown in Fig 17, while other branches are terminated to 50 Ω. Two-tones at 20 MHz frequency offsetwere used to perform IIP3 measurement, the results are shown in Fig 18. From Fig 18, it can be seen that

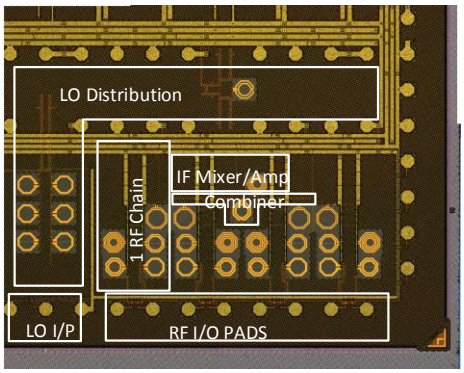
IIP3 is -28 dBm. IIP3 measurements were taken from the entire single channel with maximum gain settings of all active blocks, i.e. LNA, S2D, buffers and VGAs in phase shifter. From AC analysis in spectre simulation tool (Virtuoso), it has been found that at the input of phase shifter (as shown in Fig. 1), cumulative voltage gain from preceding stages is ~19dB, and phase shifter appears to be the dominant contributor for non-linearity.

Measured noise figure (NF) for a single channel at 14.9 GHz is 5.4 dB including PCB losses. Simulated PCB loss is 2 dB that corresponds to NF of 3.4 dB in the chip, which is within 0.2 dB of simulated value. Measurements of phase shifter constellation points are done with the help of IQ analyzer option of Keysight UXA N9040B and are shown in Fig 19. The RX chain showed some coupling from VM output to LNA input, and the points in Fig 19. are measured with LNA bypass. Measured power consumption of one 4-element receiver phased-array is 463 mW.

Table 2 shows comparison results of the work with the state of the art designs in cm-wave and mm-wave frequencies. As active configuration of phase shifter is used, therefore, this work outperforms in terms of area, but at the cost of power consumption and lower values of compression points.



(a)



(b)

Fig 16: Chip micrographs (a) Complete system, (b) Single phased array [6]

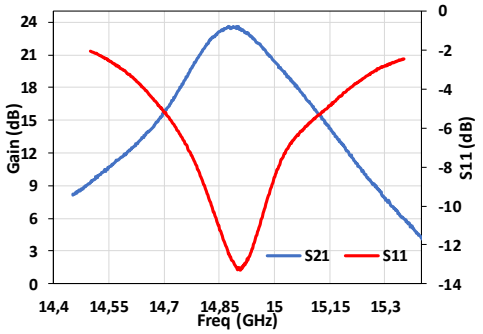


Fig 17: Measured S11 and S21 (Fixed IF=100MHz)

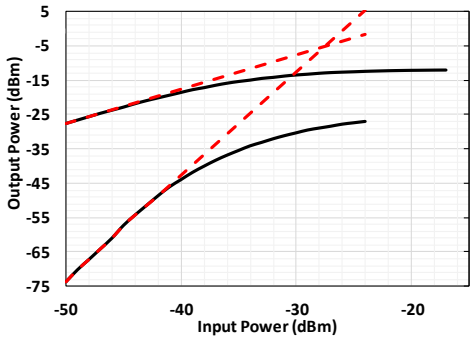


Fig 18: Measured IIP3

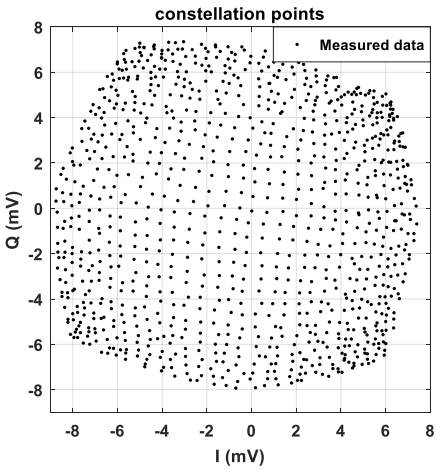


Fig 19: Phase shifter constellation points in all quadrants

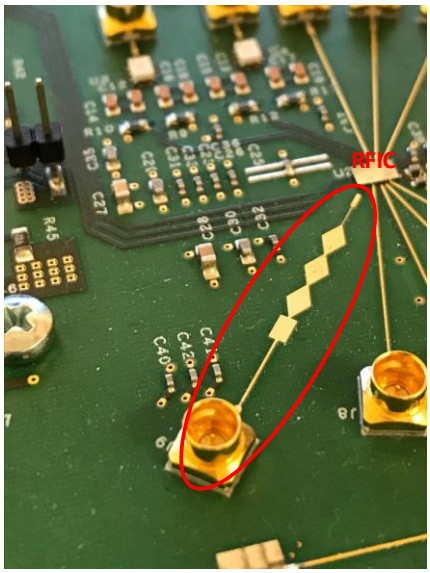


Fig 20: Designed trace implemented on PCB test board including test RFIC [8]

TABLE 2: PERFORMANCE COMPARISON [6]

	This work	[3]	[4]	[5]
Freq (GHz)	15	28	10	60
Array Size	4	32	4	16
Phase Shifter	Active	Passive	Passive	Active
Single path gain (dB)	23	34	10.1	58
NF (dB)	5.4[a]	3.7	3.4	7.4
1 dB Comp. (dBm)	-37	-22.5	-12.5	-16
IIP3 (dBm)	-28	N/A	-4	N/A
DC Power (mW)	463[b]	3300	144	1800[c]
Area (mm^2)	1.807[d]	165.3	7.25	37.7[c]
Technology	45nm CMOS SOI	0.13um SiGe BiCMOS	130nm CMOS	SiGe BiCMOS

[a] *Including 2 dB estimated PCB losses from chip-PCB interface*
[b] *4-element phased-array measurement*
[c] *Area and DC power consumption of both TX and RX*
[d] *Area of a 4 element RF phased-array excluding LO distribution network*

VI. CONCLUSIONS

A two-channel four-element phased array receiver was implemented using 45nm CMOS SOI technology. Input impedance of each LNA feed is matched to 50 Ohm source impedance using NUTL segments, which provides the opportunity of simultaneously input match and band pass filtering. A 15 GHz LO signal was distributed and divided from 30 GHz external LO. The chip was fabricated using 45nm CMOS SOI technology. Measured results from a single element show maximum gain and noise figure of 23 dB and 5.4 dB (3.4 dB without PCB losses), respectively, at 14.9 GHz. The two phased-arrays consumes small area compared to the state of the art designs. An IQ VM phase shifter was implemented at 15 GHz, which provides opportunity to fine tune the phase and amplitude of signal in each element. In addition to inherent gain controllability of VM, digital programmability is also implemented in different blocks which results in gain control range from 6 dB to 23 dB.

VII. ACKNOWLEDGEMENT

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Article Title Page

Article title: A Fully Integrated 4 x 2 Element CMOS RF Phased Array Receiver for 5G

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Abstract— This paper presents a fully integrated phased array receiver containing two four element Radio Frequency (RF) Beamforming (BF) receivers supporting two Multiple-Input Multiple-Output (MIMO) channels. The receivers are designed and fabricated using 45nm CMOS SOI technology. A 10 bit IQ vector modulator phase shifter (IQVM) is implemented in RF signal paths to control the phase and amplitude of the received signal before combining. Each IQVM provides 360 degree phase shift control and 17 dB gain variation. An off-chip, simultaneous high-Q impedance matching and bandpass filtering technique for each low-noise amplifiers (LNA) is presented using non-uniform transmission line (NUTL) segments. Measured downconversion gain at 100 MHz Intermediate Frequency (IF) and noise figure (NF) of a single path are 23 dB and 5.4dB, respectively, giving estimated 3.4 dB NF for a single element when simulated PCB and matching losses are taken into account. 1 dB compression point and Input third-order intercept point (IIP3) ~~points~~ are -37 dBm and -28 dBm, respectively. Each four-element receiver consumes 486 mW DC power from 1.2V power supply. Total area of two receivers is 5.69 mm^2.

Keywords: CMOS SOI, RF, mmWave, beamforming, receiver, input matching, phased array, LNA, phase shifter, mixer, vector modulator, wireless communication, 5G

A Fully Integrated 4 x 2 Element CMOS RF Phased Array Receiver for 5G

Rana A. Shaheen, Rehman Akbar, Alok Sethi, Janne P. Aikio*, Timo Rahkonen*, Aarno Pärssinen

Abstract— This paper presents a fully integrated phased array receiver containing two four element Radio Frequency (RF) Beamforming (BF) receivers supporting two Multiple-Input Multiple-Output (MIMO) channels. The receivers are designed and fabricated using 45nm CMOS SOI technology. A 10 bit IQ vector modulator phase shifter (IQVM) is implemented in RF signal paths to control the phase and amplitude of the received signal before combining. Each IQVM provides 360 degree phase shift control and 17 dB gain variation. An off-chip, simultaneous high-Q impedance matching and bandpass filtering technique for each low-noise amplifiers (LNA) is presented using non-uniform transmission line (NUTL) segments. Measured downconversion gain at 100 MHz Intermediate Frequency (IF) and noise figure (NF) of a single path are 23 dB and 5.4dB, respectively, giving estimated 3.4 dB NF for a single element when simulated PCB and matching losses are taken into account. 1 dB compression point and Input third-order Intercept Point (IIP3) ~~points~~ are -37 dBm and -28 dBm, respectively. Each four-element receiver consumes 486 mW DC power from 1.2V power supply. Total area of two receivers is 5.69 mm^2.

Keywords—CMOS SOI, RF, mmWave, beamforming, receiver, input matching, phased array, LNA, phase shifter, mixer, vector modulator, wireless communication, 5G

I. INTRODUCTION

Recently, introduction of new wireless concepts such as “internet of things (IoT)” and enhanced live stream videos (video on demand) has opened a need of exponential rise in wireless devices and spectrum need. Minimum peak data rate requirements for future wireless communication systems, i.e. 5G [1]~~[1]~~, are set to be 10 Gbps. Higher order modulation schemes, e.g. 64 QAM, 128 QAM or 256 QAM, are used to achieve high data rates, which poses tough requirements for signal to noise ratio (SNR). To achieve higher SNR, bandwidth of at least hundred MHz is required. Wireless spectrum lower than 6 GHz is highly crowded with existing standards and there is not enough bandwidth available. One practical solution is to occupy higher frequencies with less crowded spectrum, which can offer the required network capacity than currently available. Therefore, millimeter wave frequencies are being considered for future communication systems.

One of the many possible scenarios for 5G architectures is the combination of multi standard and multi band systems. For example, use of low frequencies system for wider area coverage, mm-wave frequency systems for higher data rate links. Multiple antenna systems or phased arrays can provide the benefit of improvements in link SNR, i.e. array gain is used for compensating path loss at mm-wave frequencies, as well as beam steering capability for directivity. A 32-element and 16-element fully integrated RF beamforming architectures are presented in [2] and [4], respectively. Higher number of antennas, helps to improve link quality and long range but only for a single user scenario. In a dense environment where multiple scatterers and multiple users are present, a system, that can handle multiple streams simultaneously from different users, is inevitable. A MIMO system is fully capable of handling different spatial streams in more dense environments. A hybrid architecture of MIMO techniques and beamforming together can benefit improvements in link SNR as well as spatial filtering for multi-user environment at the same time. In [2]~~[2]~~, future wireless system for MIMO and RF beamforming is suggested for different communication link scenarios. It has been shown that non-coded data rate of 3 Gbps can be achieved using higher-order modulation schemes such as 256 QAM, which requires at least 33 dB SNR for 500 MHz bandwidth. However, with the use of multiple independent streams, the SNR requirements can be relaxed, e.g. a 4-5 Gbps data rate can be achieved with two MIMO channels using only 64 QAM modulation scheme, which requires reduced SNR of 25 dB [2]~~[2]~~.

Based on the position of phase shifting of received signal, different types of beamforming architectures are realized, e.g. RF path, LO path or baseband path phase shifting. RF path phase shifting and combining technique has the advantage of less complexity and lower power consumption, therefore, becoming a typical choice for implementation of CMOS receiver phased arrays. Various phased array architectures at cm-wave and mm-wave frequencies have been reported in literature [3]~~[3]~~, [4]~~[4]~~, [5]~~[5]~~. In this paper, we present the implementation of integrated solution for RF beamforming receiver design supporting two MIMO channels in a single chip [6]~~[6]~~. In addition to capacity, future 5G networks are expected to provide traffic density and spectral efficiency far beyond current radio systems. Therefore spatial filtering and side-lobe reduction are essential design criteria and necessitates amplitude tapering in addition to phase. Vector modulator phase shifters provide efficient means to control both phase and amplitude thus allowing calibration that can be managed both at the same time.

This paper describes a complete design and characterization of two-channel RF phased-array receiver implemented in 45nm CMOS SOI process. In Section II, the receiver design topology and key circuit parameters are explained. Input matching of high-Q input impedance of LNA is described in section III. Local Oscillator signal generation and distribution is discussed briefly in section IV.

Measurement results and performance parameter tables are presented in section V. Section VI and VII include chip measurements and conclusions, respectively.

II. ARCHITECTURE AND CIRCUIT DESIGN

The proposed hybrid beamforming system consists of two identical RF beamforming receivers for digital MIMO processing [6]~~[6]~~. Each receiver supports four individual antenna elements with phase shifting and combining the received signals in the RF domain. Block diagram of the designed system is shown in Fig 1~~Fig 1~~. Each RF element consists of a low noise amplifier (LNA), an active single-ended-to-differential converter (S2D) and active phase shifter. Instead of power combining using very large Wilkinson combiners, current mode combining technique is utilized, before the RF signal is downconverted to baseband (BB) using a Gilbert cell mixer. An external 30 GHz local oscillator (LO) signal is used, which is divided by 2 locally to provide 15 GHz LO signal for IQ downconversion. Digital control provides extensive means to control different gain settings, bias control, RF response tuning, phase, etc. Simultaneous input matching and bandpass filtering of LNA is implemented off-chip using NUTL segments.

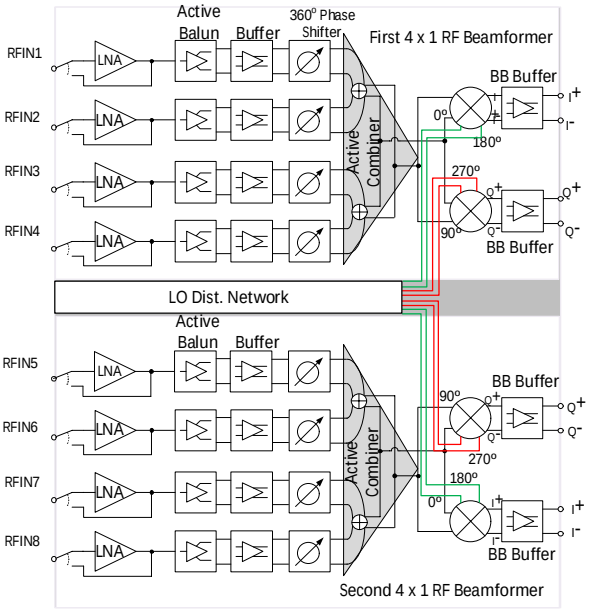


Fig 1: System Block Diagram

A. Low Noise Amplifier

LNA is the critical block in terms of total noise figure and sensitivity of the receiver. In phased array receiver systems~~s~~, ~~noise figure~~sensitivity of the complete system also gets benefit from the array gain of the phased array, which relaxes the requirements for achieving low noise figure [5]~~[5]~~. As a result, a tradeoff can be made in terms of noise figure, linearity, power consumption and filetring. Due to the fact of its built-in filtering and matching conditions, common-source cascoded inductively degenerated (CSID) source topology is utilized for LNA design [7]~~[7]~~, shown in Fig 2~~Fig 2~~. Source inductance of CSID LNA is selected such a way that it helps in canceling out the intrinsic capacitances of the input transistors, i.e. Cgs, and makes the input impedance of the transistor more real which can then be rotated to the centre of the smith chart to match with 50 Ohm source impedance. Parasitic capacitances from electrostatic discharge (ESD) diodes and input pads, introduce additional reactance at the input. This leads to relatively high Q impedance seen by 50 Ohm source port and needs additional gate inductance to cancel the parasitic capacitances. Instead of implementing gate inductance on-chip, external matching circuit is implemented with the help of NUTL segments ~~[8]~~ [8]~~[8]~~.

In case, if high blocker signal is received at the input, drain of an ~~nmos~~ NMOS transistor is connected in the signal path, which bypasses the input signal directly to next stage, hence reducing gain and improving linearity. Size of the switch is optimized for minimum off-capacitance to have minimal impact on actual input matching of the LNA. A resonance tuning control is realized with PMOS switches, which turn off/on unit capacitance to output load, changing the resonance of the load.

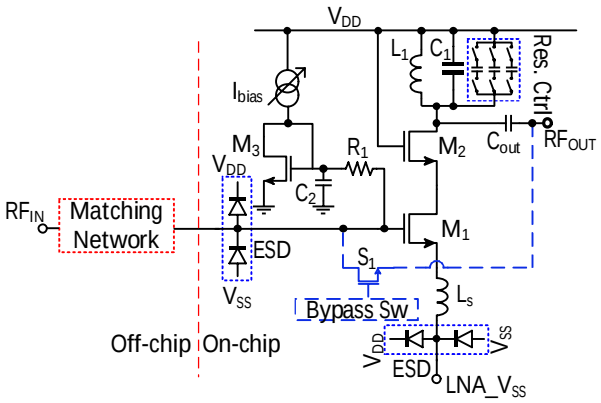


Fig 2 Common-source cascoded low noise amplifier

B. Single-ended to Differential Converter

Active balun circuit for low frequencies has been reported e.g. in [9]~~[9]~~. Parasitic components appearing at critical nodes makes the design more challenging at 15 GHz, with minimum phase and gain errors in the output signal. In this work, a gain-boosting current-balancing balun circuit topology [9] is selected as a baseline for single to differential signal converter as shown in Fig 3~~Fig 3~~.

S2D circuit is composed of two stages: common gate-common source (CG-CS) M1-M2 input stage for gain boosting and the output current is then balanced by CG devices M3 and M4 with cross coupled input also called differential current balancer (DCB). All the devices M1-M4 are of equal sizes. A resistive feedback inverter amplifier (X_1) is used to self-bias M1 and M2. A two-step resistive attenuator is implemented at the output. A center-tapped coil is used as a load and for tuning the frequency response at 15 GHz. Resonance tuning is also implemented in this block.

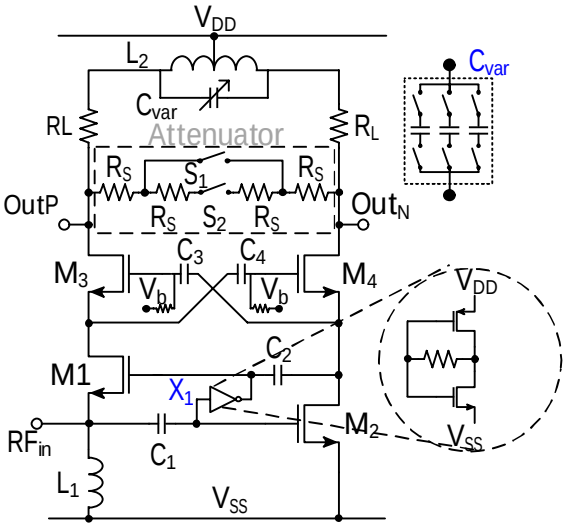


Fig 3: Single-ended to differential converter

C. IQ Vector Modulator Phase Shifter

RF phase shifter (PS) is the core block of RF phased arrays. Passive structures such as reflection-type PS and switched-line PS are demonstrated in [3] ~~[3]~~ and [5] ~~[5]~~, respectively. Passive phase shifters are linear and accurate in terms of phase error, but area can be large and loss is unavoidable. Active PS, such as, Vector modulator (VM) phase shifter provides compact size, better noise performance and opportunity to tradeoff with linearity using appropriate gain partitioning in internal amplifiers.

Active digitally controlled 10-bit vector-sum phase shifter topology is used in this work, which provides in total 1024 points in phasor plot in all four quadrants. Block diagram of the phase shifter is shown in Fig 4 ~~Fig 4~~. A differential signal is split into four quadrature signals with the help of passive poly-phase filter. Each quadrature differential signal is then weighted individually with the help of a Variable Gain Amplifier (VGA), and the output currents from I and Q branches are summed up to form a resultant vector with particular phase. A quadrature selector is used for switching the quadrants of the resultant vector to implement full 360°.

1) Quadrature signal generator

Quadrature distribution of the input signal has been the major and critical building block for different RF applications. There are few topologies for distributing the input signal into its quadrature signals, e.g. poly phase filter, quadrature hybrid, frequency dividers and quarter wave length transmission lines. Among these topologies, quadrature hybrid and quarter-wave transformer are passive structures which are used because of their linear behavior in the signal path, but they are lossy and very large in size at 15 GHz. Frequency dividers are used to generate quadrature signals in LO distribution circuits. They are completely nonlinear devices and cannot be used in the signal path for phase shift. A poly phase filter (PPF) topology is used in LO/RF IQ generation to support direct conversion receivers. They are compact in size and if layout is properly drawn show good performance in respect of amplitude and phase variation. A wider bandwidth can be achieved by using multiple cascaded stages of PPF. An RC poly-phase filter topology, shown in Fig 4 ~~Fig 4~~ (~~d~~c), is utilized for quadrature generation due to its compact area. To achieve balanced signal at the output careful symmetrical layout is implemented.

2) Vector Selector

Differential I and Q vectors can sweep the amplitude and phase of the input signal for 180° phase shift. To achieve the full 360° phase shift, a quadrature selector or differential sign inversion block is required. Circuit diagram of vector selector (VS) is shown in Fig 4 ~~Fig 4~~ (~~e~~d). NMOS devices are used as switches by biasing the sources and drains of the transistors with local ground connections. On-resistance of the switch contributes the loss but off-capacitance also contributes the resonance variation of the poly-phase filter. Switch sizes are optimized to achieve minimum on-resistance and off-capacitance. To isolate or minimize the switching behavior of the VS, a dc coupled differential amplifier is used between PPF and VS. A digital control bit is used to select the set of the transistors at a time, i.e. in Fig 4 ~~Fig 4~~ (~~e~~d), bit b1 turns on M1 and M4, while inverse of b1 is applied to completely turn off M2 and M3.

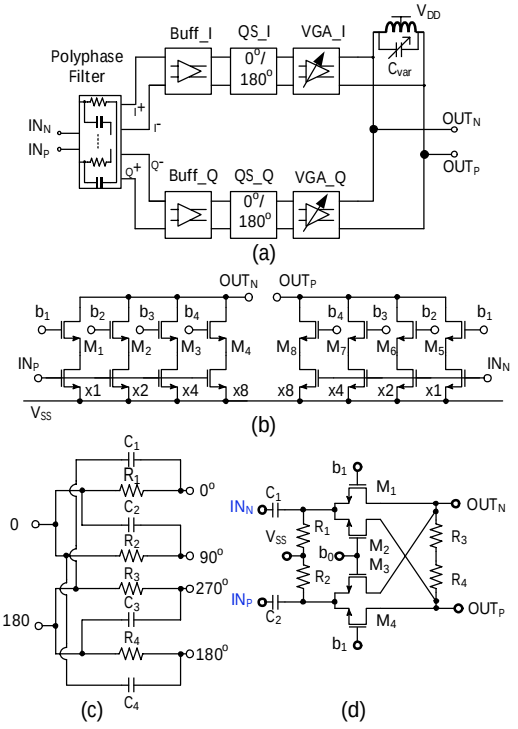


Fig 4: (a) Vector modulator architecture, (b) Variable gain amplifier (c) RC Polyphase filter ~~Quadrature selector (QS),~~ (d) ~~RC Polyphase filter~~Vector selector (VS)

1) Variable Gain Amplifier

Amplitudes of I and Q branches of the IQVM are controlled and combined to achieve desired resultant vector, which as a result provides a unique phase and amplitude set to the input signal. In [5], a phase inverting variable gain

amplifier is used in BiCMOS process at 60 GHz. A variable gain amplifier (VGA) is used to control the amplitudes of the I and Q branches individually, as shown in Fig 4~~Fig 4~~ (b). Because of limited supply voltage, i.e. 1.0 V, we used Common-source NMOS transistors as inputs with cascode connection of NMOS switches to digitally control RF current of binary weighted devices. The differential currents from both I and Q branch VGAs are combined with the help of center-tapped coil~~.~~ ~~with resonance control. is for summing the internal signal paths of the vector modulator at the output.~~

D. Antenna Signal Path Combining

Wilkinson combiner is commonly used at mm-wave frequencies. However, at 15 GHz, integrated λ/4 TLs are very large and therefore, impractical to implement on chip. In large phased array systems, architecture affects gain budget and thus linearity and NF of the whole receiver. Wilkinson power combiners were utilized in [4]~~—[4]~~, while a combination of a passive and active combiners were demonstrated in [5] for 16 elements.

Due to compact size at 15GHz operation a two-stage current combining is implemented in this work using first a parallel differential pair with fixed tail current topology, as shown in Fig 5 (b), which provides sufficient isolation from the other paths to avoid loading effects. In the second stage, output currents of the active combiners are summed using a narrowband LC load with low ohmic metal wires. A center-tapped coil is used for supplying DC power to these two combiners and resonate out the wiring capacitances at center node.

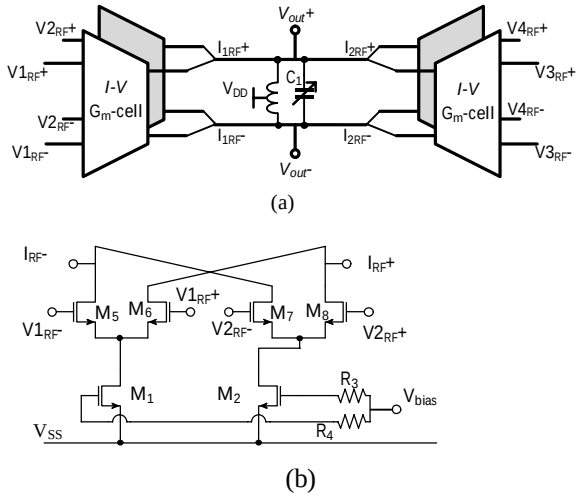


Fig 5: (a) 4 to 1 Active current combiner, (b) 2-1 V-I Gm-cells

E. Current Bleeding Mixer and IF Amplifier

Mixer schematic is shown in Fig 6~~Fig 6~~. A Gilbert cell type double balanced current reuse topology [10] is used for two mixers, i.e. for I and Q outputs. Mixer input part is composed of a NMOS and PMOS pair connected in cascode, biased separately from bias blocks. Input RF signal is AC coupled from previous stage and both input devices are also AC coupled from each other. Conventional divide-by-two approach is used to generate I/Q signal from externally generated 30GHz LO signal.

Differential amplifier with resistive feedback is used for buffering the output at baseband. Longer channel length of the output devices is possible due to limited BW up to few hundreds of MHz. The pull up coils of the baseband amplifier are placed off-chip with external balun package.

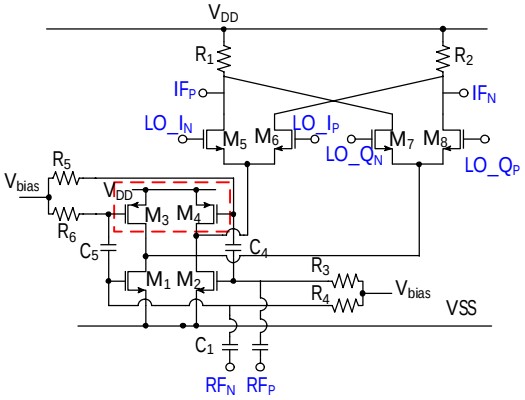


Fig 6: Downconversion Mixer

III. Input Matching Design

Source inductance of the CSID LNA helps to remove effects of reactive part of the intrinsic input capacitance of the input transistor of LNA, which in turns makes the input matching process easier. However, if parasitic capacitances, mainly due to the wiring components from the structures such as electrostatic discharge (ESD) diodes and IO pads are not taken carefully into account, the LNA input impedance typically appears to be highly reactive resulting in high-Q impedance. That makes impedance matching over the wider BW very complicated. In [8], a method of matching the high-Q impedance for a wide BW of 1.2 GHz at 15 GHz (relative BW of 7%) using NUTL segments is presented. In this design, cancellation of reactive part of the input impedance was not implemented on-chip. In this work, we utilize the opportunity to use external wideband matching technique using NUTLs for matching relatively high-Q input impedance of phased array inputs. RF inputs of all eight elements are matched at 15 GHz using the NUTL segments topology, which are compact in size and provides additional benefits of bandpass filtering.

All eight elements placed next to each other are implemented in IC on the same edge. For PCB characterization, the chip is attached to PCB as a flip chip via solder bumps. Area of each pad is 100 um x 100 um and the pitch between two consecutive RF IO pads is 190 μm. A 0.1mm wide transmission line is needed to feed the signal to the input of the LNA. A four-layer PCB was used with the material characteristics of εr = 2.99 and losstan δ = 0.0017. Total thickness of PCB is 0.43 mm resulting in the linewidth of 230 um (50 Ω) with the top metal. Impedance matching of a single receiver at center frequency of 15 GHz is achieved in three steps, discussed as in details in [8].

A. Transformation of Capacitive Reactance

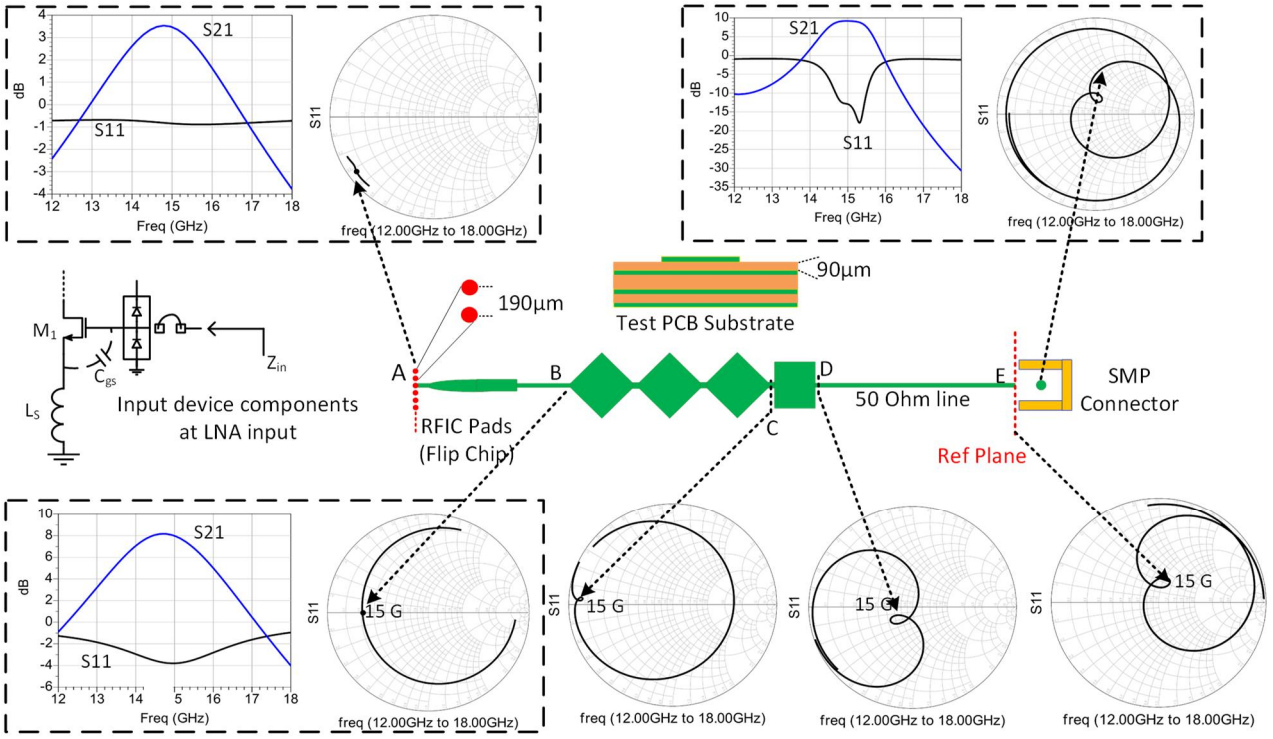


Fig 7: Schematic of input device with the design procedure of impedance matching line showing S11 and S21 (Simulations) graphs at key interfaces [8]

At the targeted centre frequency, the input impedance at input pad of LNA appears to be highly capacitive, as shown in Fig 7 by point 'A'. In order to cancel the reactance, the initial TL with the width of 0.1mm together with a tapered-line is provided. The long taper line at the beginning is mandatory as it spans out the inputs, providing sufficient space between them. The main goal of the initial transformer is to transform the reactive impedance close to low ohmic real plane on the Smith chart, shown in Fig 7: Schematic of input device with the design procedure of impedance matching line showing S11 and S21 (Simulations) graphs at key interfaces Fig 7 ~~Fig.1~~ by graphs at point 'B'.

B. Taper-Line Diamond Segments for Multiple Resonances

This part is the core of the matching circuit. A λ/4 long single segment rotates the impedance of targeted bandwidth into a circle as shown by graphs at interface 'C' in Fig 7. By adding multiple sections, the impedance circle is narrowed so that it can be later on shifted to the center of the Smith chart. Three segments are used, which results in two rotations of impedance points in the Smith chart. One diamond-shaped segment is realized by combining two taper lines. The characteristic impedance of the segment varies linearly from 50 Ω to 8 Ω and again back to 50 Ω.

C. Impedance Transformer for Shifting Resonance

The purpose of this section is to transform the impedance response to the centre of the Smith chart. This is carried out with the impedance step transformers starting with a λ/8 line segment (Z0 of 10 Ω), which provides rotation in the impedance response at frequencies of interest (plot at interface 'D' in Fig. 1). A 50 Ω TL is used until interface 'E' (reference plane for connector model) in Fig 7, which rotates frequency impedance points in counter-clockwise direction, i.e. towards center. Finally, connector model is added (plots at connector interface in Fig 7. This rotation of S11 around center, provides bandpass-type response in S11 and S21 plots as shown in Fig 7 at connector interface.

IV. LO DISTRIBUTION AND I/Q PHASE GENERATION

Divide-by-two approach is used to generate I/Q signal at 15GHz. Each receiver has its local frequency divider and inverter based driver. Moreover, the distribution of LO is done at 30GHz as shown in ~~Fig 8~~ Fig 8. External waveform generator provides single ended signal and on chip active balun (S2D) is implemented to have differential signal. Line drivers placed in distribution network to compensate the

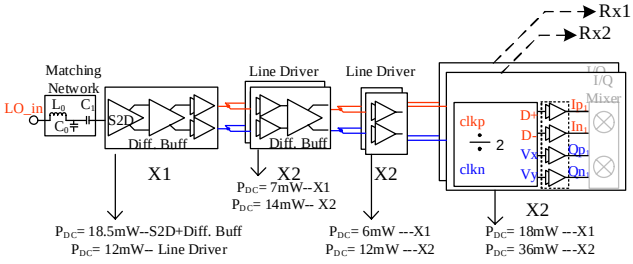


Fig 8: LO distribution block diagram

distribution losses. The strength of LO signal at 30GHz depends on the minimum input voltage required to drive the frequency divider.

A. *LO Frequency Division*

Current-mode logic (CML) allows achieving the fastest operation speed, compared to e.g. true single-phase clocked (TSPC) or digital CMOS logic. The advantage of using static frequency divider, it can operate up to 40GHz without using LC load [11][~~11~~], [12][~~12~~]. Which allows using them for local generation of I/Q for each receiver and reduce the overhead of wiring.

The divided by two operation is realized using a D-type master-slave flip-flop, consisting of two cascaded D-latches shown in Fig 9~~Fig 10~~. The cross connection between the output of the slave latch and the input of the master causes the clock frequency to be divided by two. During one half of the clock period the M1 and M2 are activated, and the voltage is “sampled”. Simultaneously, in the first half of the clock period the latch transistors of the M9 and M10 are activated and the state of M7 and M8 is “held”. In the second half of the clock period, the operation is inverted - the M7 and M8 are activated and ”sample” the state presented by M3 and M4 that simultaneously ”hold” the previous sampled state.

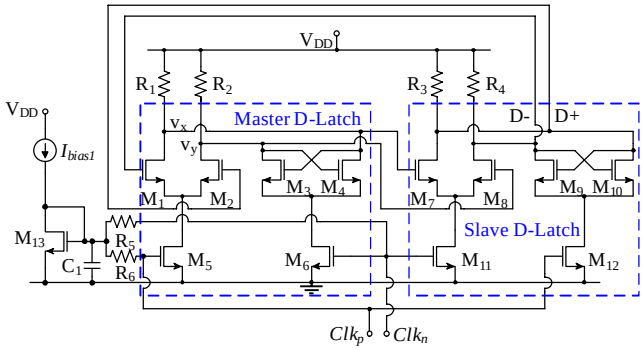


Fig 9: CML divide-by-2 frequency divider

The speed of operation strongly depends on input clock transistors (M5, M6, M11 and M12), as the size is made smaller, large differential voltage required at the input of differential pair (M1, M2, M7 and M8) for the current to be fully switched. The size of cross coupled pair (M3, M4, M9 and M10) determines whether divider will self-oscillate [13] ~~[13]~~. This depends upon the gm of cross-coupled pair, the divider will oscillate if gm R >1. In addition, smaller the size of cross-
coupled pair, divider would achieve higher speed of operation. The sizes of transistors are selected according to the conditions as explained above. The size of differential pair transistors are 16.8µm, cross-coupled pair transistors are 12.6µm which gives gm = 10mS and input clock transistors are 21µm, using length L=56nm. The resistors R1-R4 are 170Ω.

The sensitivity curve of frequency divider gives the minimum input amplitude Vmin of the fclk, for which the divider functions properly. The simulated sensitivity curve shows in Fig 10~~Fig 11~~, defines minimum 30mVp required at 30GHz for divide-by-two operation.

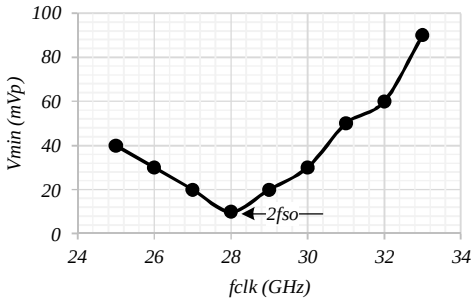


Fig 10: Sensitivity curve of frequency divider

The I/Q phase generation can be realized by taking the output from Vx, Vy (Ip and Im) and D+,D- (Qp and Qm) node. The generated I/Q signals swing is not rail-to-rail; to generate rail-to-rail signals inverter based buffer is implemented, shown in Fig 11~~Fig 12~~. First stage of buffer is having feedback resistor to bias inverter at half of voltage supply (VDD =1Vdc), which ensure the switching of following inverter stages. The transistor sizing of buffer in Fig 11~~Fig 12~~ are according to LO switching transistors of I/Q mixer. The sizes of PMOS and NMOS transistors in inverter stages are same and buffer for Ip and Im are same. M1 =4µm, M3 = 6µm, M5 = 9µm, M7 = 16µm and R1 = 5.8kΩ.

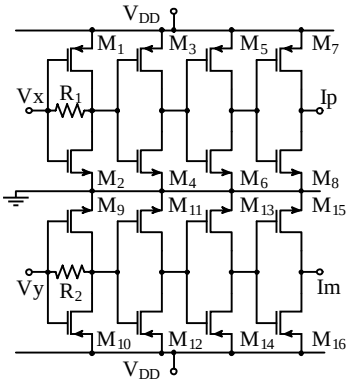


Fig 11: Buffer for driving I/Q mixer

The frequency divider combined with I/Q mixer buffer is simulated using I/Q mixer as load. The results shown in Fig 12~~Fig 13~~ are post simulation results. Table 1 in Fig 12~~Fig 13~~ shows the output parameters, when minimum input amplitude voltage Vmin is applied at 30GHz at clkp and clkn with the phase difference of 180°.

B. *Active Balun*

Frequency divider needs a differential input signal and external waveform generator provides single-ended output. Moreover, differential conversion at 30 GHz is rather easy when implemented on-chip. The configuration of balun circuits can be passive or active. The passive balun has the compact size at high frequency (e.g. 60GHz), but introduces signal loss at each differential path [14][~~14~~]. The active balun

is more attractive because it not only creates differential output but provides conversion gain.

Table 1: Divider Output parameters

Parameters	Value
I/Q (p)-Phase	88.92°
I/Q(m)-Phase	269.2°
Rise time	6.3psec
fall time	5.8psec
fout	15GHz
Duty cycle	49%
Output swing	1Vpp
Power	18mW

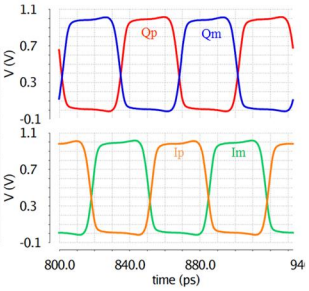


Fig 12: Transient waveforms and output parameters of frequency divider

Combination of common source-common gate amplifiers (CS-CG) amplifier, single transistor splitting (CS with degeneration), and differential amplifier with single-ended input are the conventional way to implement the balun circuit [14]~~[14]~~, [15]~~[15]~~ and [16]~~[16]~~. The above mentioned topologies are very sensitive to parasitics at frequencies above 20GHz, which introduce high gain (±2dB) and phase error (180°±10°) [15]~~[15]~~. In fact, the gain error and the phase errors are not independent [14]~~[14]~~, [15]~~[15]~~ and [16]~~[16]~~. Therefore, gain and phase errors have to correct simultaneously.

Fig 13~~Fig 14~~ shows the implemented active balun at 30GHz [16]~~[16]~~. This topology used two balun circuits, balun-A consisting of transistor M1 and M2 followed by two balun-B circuits consisting of transistor M3, M5 and M4, M6. Balun-A (CS-CS amplifier) is used to create the differential signal and balun-B is used to correct the phase and gain error. The circuit can achieve the resonance tuning range 32.5 to 28.5GHz (see Fig 14~~Fig 15~~)

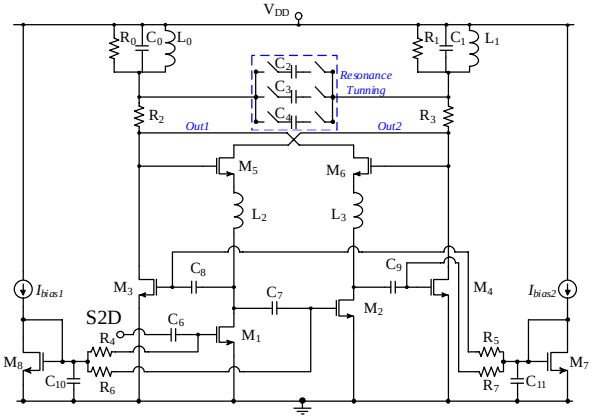


Fig 13: Active Balun Schematic

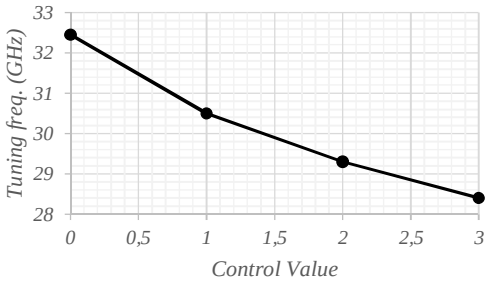
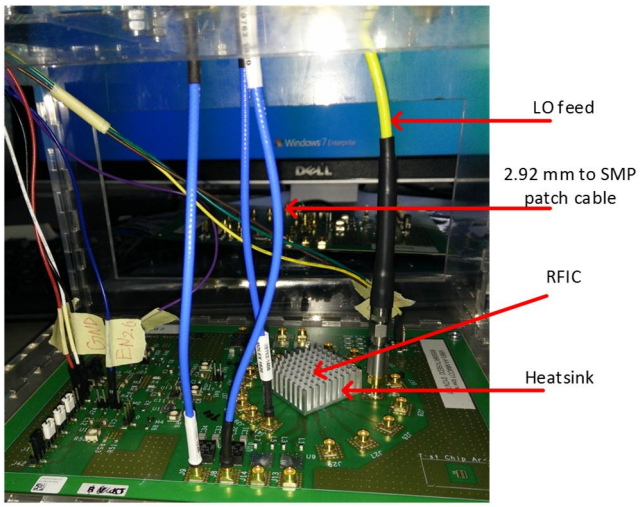


Fig 14: Tuning frequency range of resonance control of frequency divider

V. Experimental Results

Measurement setup to characterize the phased array IC is shown in Fig 15~~Fig 16~~. IC is flip-chipped directly on the PCB using solder bumps to minimize parasitics. In an unpackaged flip-chip, the chip pad areas dictate the pitch of the PCB as well. IO pad pitch is 190 µm with the pad area of 80 um x 80 um. Due to PCB manufacturing limitations, a maximum width



of 100 um wide transmission line can be used to feed the signal lines to the input of the LNA near the chip and afterwards can be tapered to wider widths. The four-layer PCB by Isola Astra MT77 was used with the material characteristics of ε_r = 2.99 and losstan(δ) = 0.0017. The total thickness of top layer of PCB is 0.09 mm resulting in the linewidth of 230 um (50 Ω) using the top metal. Test chip is manufactured using 45nm CMOS SOI technology. Fig 16~~Fig 17~~ shows the micrograph of the manufactured chip of the complete 4 x 2 phased array, with all the RX inputs placed next to each other on the same edge of the IC. The core area is 3.95 x 1.44 mm^2 including pads.

Fig 15: Measurement setup for the IC

Calibration of the measurement cable was performed using electronic calibration (N4694A ECal) module provided by Keysight Technologies. Effects of connectors and cables upto PCB connectors were calibrated out. Input impedance of each LNA feed is designed to 50 Ohm source impedance using NUTL segments [8]~~[8]~~, which provides the opportunity of simultaneously input match and band pass filtering. Measured input impedance matching (S11) of a single receiver at centre frequency of 15 GHz is less than -10 dB. Conversion gain

measurements were performed using a vector network analyzer (VNA) using frequency converter option, which requires calibration of measurement setup at two different frequencies at the input and output of the receivers. Cold source method [17]~~[17]~~ using spectrum analyzer is used for measuring noise figure (NF) of a single RX chain while other chains are switched-off. A single RX element provides a maximum conversion gain of 23 dB at 14.9 GHz, which is 2 dB less than estimated in post-layout simulations. Single chain RF response and S11 curves are shown in Fig 17~~Fig 18~~, while other branches are terminated to 50 Ω. Two-tones at 20 MHz frequency offset~~test for I~~were used to perform IIP3 measurement, the results are shown in ~~is performed at 20MHz frequency offset and extrapolated curve gives IIP3 = -28 dBm (see~~ Fig 18~~Fig 19)~~. From Fig 18, it can be seen that IIP3 is -28 dBm. IIP3 measurements were taken from the entire single channel with maximum gain settings of all active blocks, i.e. LNA, S2D, buffers and VGAs in phase shifter. From AC analysis in spectre simulation tool (Virtuoso), it has been found that at the input of phase shifter (as shown in Fig. 1), cumulative voltage gain from preceding stages is ~19dB, and phase shifter appears to be the dominant contributor for non-linearity.

Measured noise figure (NF) for a single channel at 14.9 GHz is 5.4 dB ~~without~~ including PCB losses. Simulated PCB loss is 2 dB that corresponds to NF of 3.4 dB in the chip, which is within 0.2 dB of simulated value. Measurements of phase shifter constellation points are done with the help of IQ analyzer option of Keysight UXA N9040B and are shown in Fig 19~~Fig 20~~. The RX chain showed some coupling from VM output to LNA input, and the points in Fig 19~~Fig 20~~. are measured with LNA bypass. Measured power consumption of one 4-element receiver phased-array is 463 mW.

Table 2 shows comparison results of the work with the state of the art designs in cm-wave and mm-wave frequencies. As active configuration of phase shifter is used, therefore, this work outperforms in terms of area, but at the cost of power consumption and lower values of compression points.

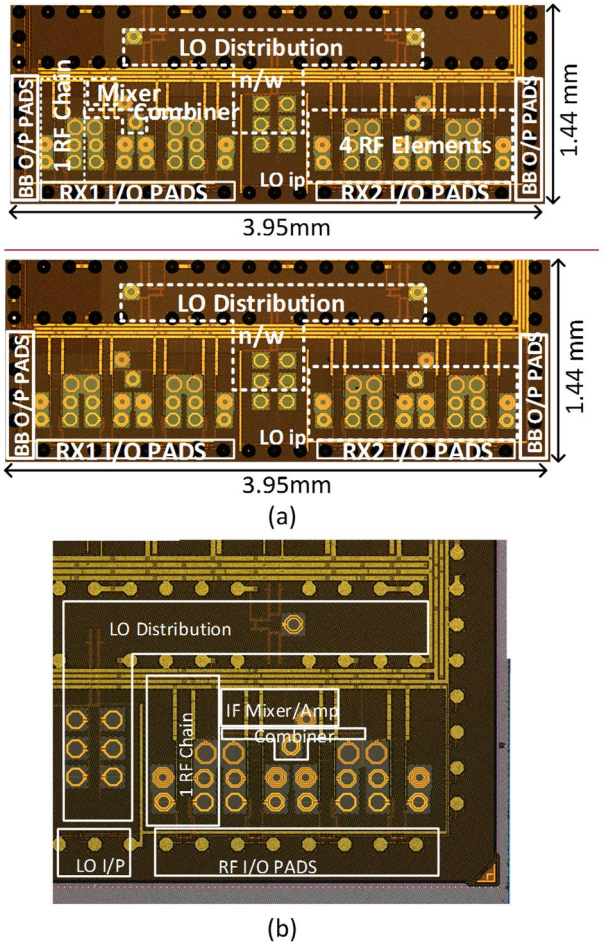


Fig 16: Chip micrographs (a) Complete system, (b) ~~of a two channel phased ar~~Single phased array [6]

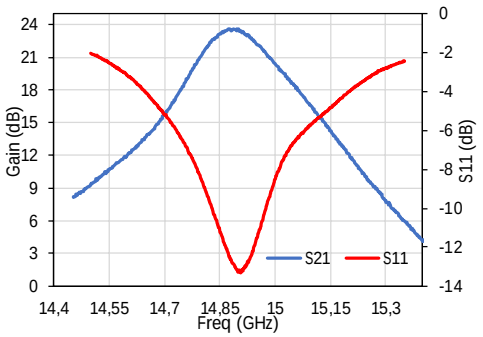


Fig 17: Measured S11 and S21 (Fixed IF=100MHz)

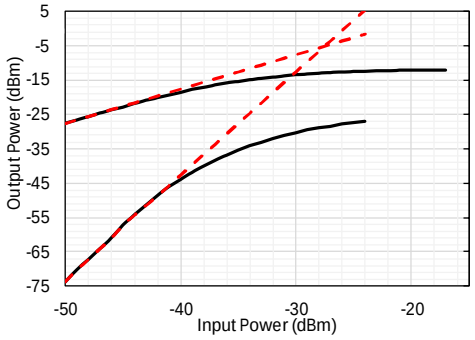


Fig 18: Measured IIP3

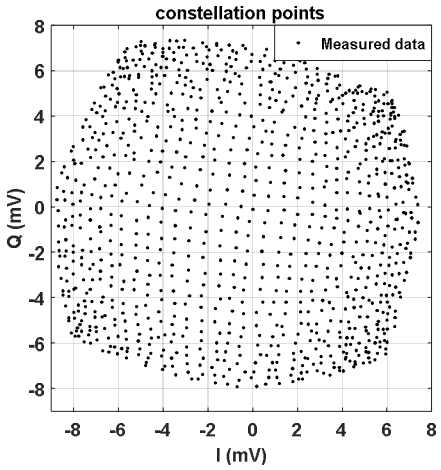


Fig 19: Phase shifter constellation points in all quadrants

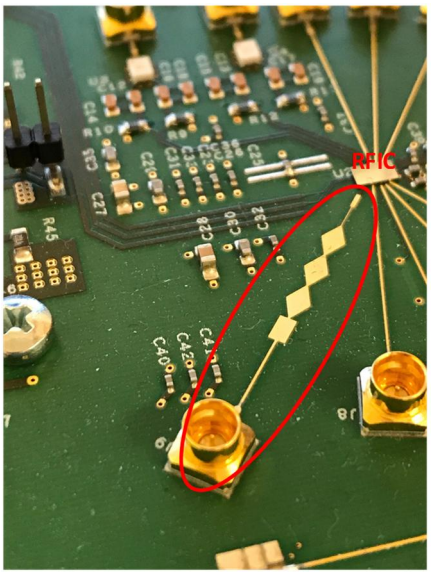


Fig 20: Designed trace implemented on PCB test board including test RFIC [8] ~~[8]~~

TABLE 2:

~~TABLE I.~~ PERFORMANCE COMPARISON ~~[8]~~ [6]

	This work	[3]~~[3]~~	[4]~~[4]~~	[5]~~[5]~~
Freq (GHz)	15	28	10	60
Array Size	4	32	4	16
Phase Shifter	Active	Passive	Passive	Active
Single path gain (dB)	23	34	10.1	58
NF (dB)	5.4[a]	3.7	3.4	7.4
1 dB Comp. (dBm)	-37	-22.5	-12.5	-16
IIP3 (dBm)	-28	N/A	-4	N/A
DC Power (mW)	463[b]	3300	144	1800[c]
Area (mm^2)	1.807[d]	165.3	7.25	37.7[c]
Technology	45nm CMOS SOI	0.13um SiGe BiCMOS	130nm CMOS	SiGe BiCMOS

[a] *Including 2 dB estimated PCB losses from chip-PCB interface*
[b] *4-element phased-array measurement*
[c] *Area and DC power consumption of both TX and RX*
[d] *Area of a 4 element RF phased-array excluding LO distribution network*

VI. CONCLUSIONS

A two-channel four-element phased array receiver was implemented using 45nm CMOS SOI technology. Input impedance of each LNA feed is matched to 50 Ohm source impedance using NUTL segments, which provides the opportunity of simultaneously input match and band pass filtering. A 15 GHz LO signal was distributed and divided from 30 GHz external LO. The chip was fabricated using 45nm CMOS SOI technology. Measured results from a single element show maximum gain and noise figure of 23 dB and 5.4 dB (3.4 dB without PCB losses), respectively, at 14.9 GHz. The two phased-arrays consumes small area compared to the state of the art designs. An IQ VM phase shifter was implemented at 15 GHz, which provides opportunity to fine tune the phase and amplitude of signal in each element. In addition to inherent gain controllability of VM, digital programmability is also implemented in different blocks which results in gain control range from 6 dB to 23 dB.

VII. ACKNOWLEDGEMENT

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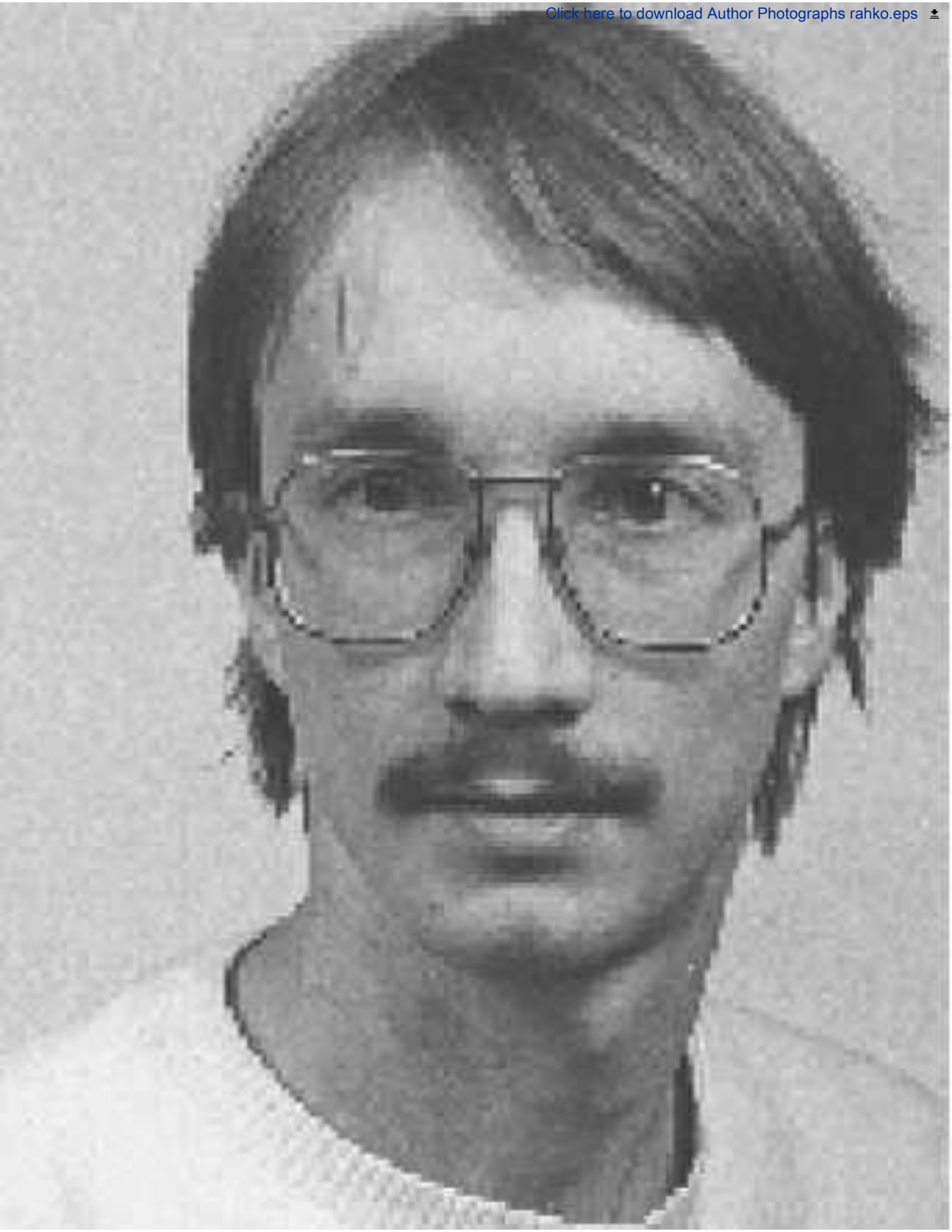

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