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A Four Channel Phased Array Transmitter using an Active RF Phase Shifter for 5G Wireless Systems

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Abstract This paper presents a four channel phased array transmitter at 15 GHz aimed for the upcoming 5G wireless systems. The circuit is designed and fabricated using 45 nm CMOS silicon on insulator (SOI) technology. The design is programmable with exhaustive digital controls available for parameters such as bias voltage, resonance frequency, and gain. The phase shift required for the phased array is provided at RF using an IQ vector modulator (IQVM) topology, which provides both amplitude and phase control. Based on the measurement results, the IQVM provides 360 degree of phase shift and 15 dB of gain variation. Both phase and amplitude information are encoded in a 10 bit control word. The mean angular separation provided by the IQVM is 3 degree at optimum amplitude levels. Active area occupied is 2.88 square millimeter. Total DC power consumed by one transmit channel from 1 V and 2.6 V supply is 268 mW. The maximum RF output power from one transmit channel is 1 dBm. Measured EVM for a 256 QAM modulated signal is as low as 2.0%. All results include the impact of printed circuit board (PCB) traces and pad parasitics. Based on the achieved results, the proposed architecture is well suited for the next generation of the wireless systems.

Keywords CMOS · SOI · beamforming · RF · phase shifting · phased arrays · wireless communications · 5G · IQVM

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1 Introduction

5G is the next major milestone of wireless communication standards and is also referred to as wireless technologies beyond 2020. The expectations of achievable data rates in 5G are approximately a 1000 fold higher compared to current 4G data traffic standard. Furthermore, 5G wireless systems should also be compact, allow for denser deployments (small cells), and power efficient (green communications) [1, 2]. To achieve higher data rates in both uplink and downlink directions, wider band channels with multiple spatial streams are required. One way to achieve this is by utilizing Multiple-input Multiple-output (MIMO) technology with frequencies beyond 6 GHz i.e., centimeter or millimeter wave (mmWave) MIMO. Greater ease in allocating wider channels at higher frequencies along with the relatively sparse usage of these bands [3], further supports this transition. An additional advantage of higher carrier frequencies is smaller antennas and directive transmission. Unfortunately, the environmental path loss increases as the carrier frequency increases. Thus, in order to maintain the required signal-to-noise ratio (SNR) at the receiver while keeping the cell size constant, we need either higher transmit power per antenna or a larger amount of antennas with smaller transmit power per antenna. Due to difficulties in designing modules with higher output power at mmWave frequencies [4], increasing the number of antennas is the only viable solution.

One feasible way to utilize a massive number of antennas is to provide a complete RF transmitter chain i.e., a digital-to-analog converter (DAC), an analog transmitter and the required passive components, for each antenna [5]. This architecture relies solely on digital baseband processing while keeping the analog RF sim-

ple. An approximate dual of this is to construct highly directive beams at RF using phased arrays [6, 7] and allocate different beams to individual users in order to achieve capacity and data rate. As this design generates narrow beams in analog domain, it requires a complex digital baseband in order to track users, achieve capacity and mitigate fading. Both of these approaches are extremely cost prohibitive due to the required massive parallelism and can be considered as a viable solution where there are very relaxed constraints on the available electrical power. A more pragmatic approach is to utilize smaller number of RF transmitters while making them more intelligent and integrating them tightly with the digital baseband. This approach yields an architecture called as hybrid beam-forming massive MIMO system [8], where the number of RF transmitters is significantly less as compared to the number of antennas.

Beamforming is the common theme in the architectures discussed above, i.e., instead of radiating power equally all over the sector, the transmission is highly directive. One property of beamforming is that it creates a sinc like pattern in the spatial domain i.e., besides one global maxima there will be multiple sidelobes that contain a significant amount of transmitted power [9, 10]. Thus, in order to have denser deployments, sidelobe level reduction to minimize out-of-beam interference is essential. To achieve that, 10 dB of RF amplitude control range is typically required.

In this paper, we describe a four channel phased array transmitter targeted towards 5G communication systems. The phased array is tuned to operate at 15 GHz, which is appropriate for prototyping, although recent interests in 5G are at 28 GHz, or above. The phased array uses an IQ vector modulator (IQVM) at RF to generate the required phase variation. The 10 bit control word of the IQVM encodes both phase and amplitude information and provides 10 dB of RF amplitude control, which is required for amplitude tapering applications. The maximum RF power transmitted by one channel of the phased array is 1 dBm and the DC power consumed is 268 mW. Measured EVM for a 256 QAM modulated signal is as low as 2.0%.

The IC implementation of a four channel phased array transmitter presented in this paper is based on our previous work on the IQVM [11] and with new results. Depending on the value of the resonance control word, it is possible to change the center frequency of the IQVM presented in [11] from 13.75 GHz to 14.45 GHz. Furthermore, it has an RF bandwidth of 2.5 GHz at a fixed resonance control word. Thus, by changing the resonance control word, the IQVM can operate from 12.5 GHz to 15.7 GHz. The IQVM is based on vector summing of two phase shifted versions of the input RF signal. The phase difference between the two versions is approximately 90°. The mean angular separation provided by the IQVM is 1.5° at optimum amplitude levels. The minimum rms phase error provided by the IQVM over the frequency band is 0.8° and occurs at 15.0 GHz.

The organization of the paper is as follows, architecture related choices are discussed in Section 2. In Section 3, circuit design for all the related blocks is described, followed by the measurement results in Section 4. Conclusions are drawn in Section 5.

2 Architecture

Basic components of a transmit phased array are distribution network, phase shifter, and a driver matched to 50 Ω impedance. One way to provide phase shifts is to generate phase shifted versions of the local oscillator (LO) itself [12]. This design choice reduces linearity requirements but it increases the overhead of routing and power consumption. A complementary approach is to provide the phase shifts at the RF in the signal path, which is followed in this work. The selected architecture is built around a digital controlled IQVM that combines phase and amplitude control in a compact area and provides means for effective tapering schemes using a single control point.

The IQVM operates by vector summing of two basis vectors as shown in Fig. 1. Here, A_I and A_Q are the rotated I and Q basis vectors with θ being the initial phase and ϕ being the generated rotation. By changing the magnitude and the relative sign of the basis vectors, different phase shifts can be generated according to the following equation

$$\angle \mathrm{RF_{out}} = \angle \mathrm{RF_{in}} + \begin{cases} 0^\circ + \arctan \frac{|A_Q|}{|A_I|} & A_Q \geq 0, A_I \geq 0 \\ 180^\circ - \arctan \frac{|A_Q|}{|A_I|} & A_Q \geq 0, A_I \leq 0 \\ 180^\circ + \arctan \frac{|A_Q|}{|A_I|} & A_Q \leq 0, A_I \leq 0 \\ 360^\circ - \arctan \frac{|A_Q|}{|A_I|} & A_Q \leq 0, A_I \geq 0. \end{cases}$$

There are multiple techniques to generate the basis vectors from the original RF signal, for example, polyphase filter, branch line couplers, hybrid couplers, etc., to name a few [13, 14]. Here, a polyphase filter is used for basis vectors generation in order to keep the occupied active area small.

A block diagram of the transmitter phased array is shown in Fig. 2. Input baseband signal is up-converted to RF by using an image canceling Gilbert cell based mixer. A divide-by-two approach is used to generate the I and Q LO signals for the mixer. Input LO signal frequency is 30 GHz that is divided to generate a 15 GHz LO. The mixer output is a differential signal

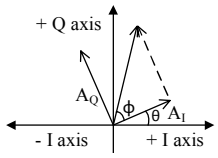

Fig. 1 Principle of operation of an IQVM [11].

which is fed to a polyphase filter, where it is split into two differential quadrature signals that form the basis vectors for the IQVM. After some amplification, these differential quadrature signals are then distributed to four independent IQVMs, where each IQVM is capable of providing phase shifts of 360° and up to 15 dB of variable RF gain for amplitude tapering in beam synthesis. Each IQVM is followed by a driver and a PA[15] that is matched to 50 Ω impedance. Serial shift registers with 20 bit parallel latches were used to tune bias voltage, resonance frequencies, and gain settings, and to control parameters like turning branches on/off and setting IQVM control words. In order to keep the complexity of address decoder low, the address space of the IC was limited to 32 registers. This address space limit however did not impact the available control words because multiple shift registers were cascaded together to form bigger registers wherever required.

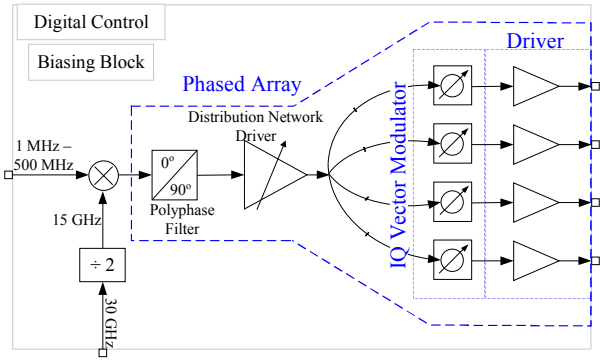

Fig. 2 System architecture of the developed phased array.

3 Circuit Design

3.1 Mixer

The mixer topology chosen is a standard Gilbert cell image canceling mixer. The Gilbert cell is dimensioned to achieve the highest linearity at the cost of the conversion gain. The baseband inputs for the mixer are taken from an off-chip source and are fed to long channel (112 nm) MOS devices. Four LO signals are generated by the divider and are fed to the regular MOS devices. The biasing is done using a controllable current source, a diode connected MOS, and a filtering capacitor. This biasing scheme is used throughout the complete transmitter block, details of which are seen in Fig. 3.

3.2 Polyphase Filter

Polyphase filter can be understood as a combination of low pass and high pass filter. Based on the manner in which the input signal is fed to the polyphase filter, it can be classified into two types; Type-I which has a constant phase difference and Type-II which has a constant amplitude [16]. Here, a constant phase topology is used. As the capacitance needed was in the order of few femto Farads (C ≈ 4 fF, R ≈ 2 KΩ), MOS transistors are used as a capacitive element instead of the traditional interdigitated metal finger capacitors. The benefit of using MOS transistors as a capacitive element is that they are easy to control via digital logic and small capacitance values can be realized more accurately with lower parasitic capacitance. In order to effectively work as a capacitor, MOS needs a bias voltage and this is provided by DC coupling the polyphase filter with the previous stage common source amplifier. In order to reduce losses, a one stage polyphase filter was implemented at the cost of bandwidth of the filter. However, even the one stage filter is extremely lossy. There are two possible design choices to partially reduce the loss of the polyphase filter,

- using a differential inductor at the output to have a resonance peak [17],
- using unsymmetrical low pass and high pass branches i.e., different resistance and capacitance values for the two branches.

As the inductors are colossal compared to the MOS at these frequencies, using the differential inductors would have made the layout impractical. Furthermore, it puts a limit on the bandwidth of the filter. An unsymmetrical low pass and high pass branch can reduce the loss by approximately 4 dB, however this requires careful layout design with unit elements to minimize the asymmetry in the layout.

The complete structure of the implemented polyphase filter is shown in Fig. 3. Transistor M_1 and M_2 are used in a common source topology and provide DC bias to M_3–M_6. The DC bias for M_1 and M_2 is provided by using a variable current source along with a diode connected transistor M_7. The variable current is provided by a three bit controllable current mirror. To filter out

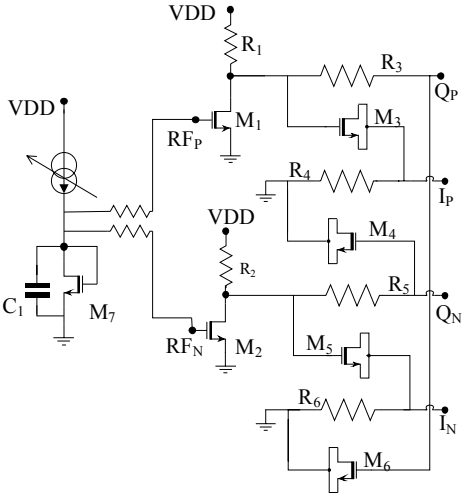

Fig. 3 Polyphase filter with a variable digitally controlled DC biasing [11].

any AC signal from the bias voltage, filtering capacitor (C_1) between ground and diode connected MOS is used.

As the bias point of the common source stage can be digitally controlled, this inherently gives control over the realized capacitance value. Thus, by changing the bias, the corner frequency of the polyphase filter can be digitally controlled.

3.3 Variable g_m Amplifier

Fig. 4 shows the schematic of a controllable gain amplifier consisting of two DC coupled common source amplifiers. The first stage is biased using a variable current source and a diode connected MOS. The DC coupling provides the bias for the second stage. To provide some bias variability for the second stage, a variable current source is also fed at the same node. This arrangement provides an independent variability of about 50 mV in the bias. The gain control consists of three unit g_m elements. The switching MOS are connected to the source terminal of the g_m MOS, as this provides some additional DC headroom to the g_m MOS, and improves the linearity a bit at the expense of gain.

3.4 Differential Amplifier

In order to cancel out signal path dominant common mode signals, a true differential pair is needed in the chain. The common mode signal here is the LO leakage from the mixer. Fig. 5 shows the schematic of the differential amplifier along with the biasing scheme. To generate different voltage levels for biasing, different sizes of the diode connected MOS are used.

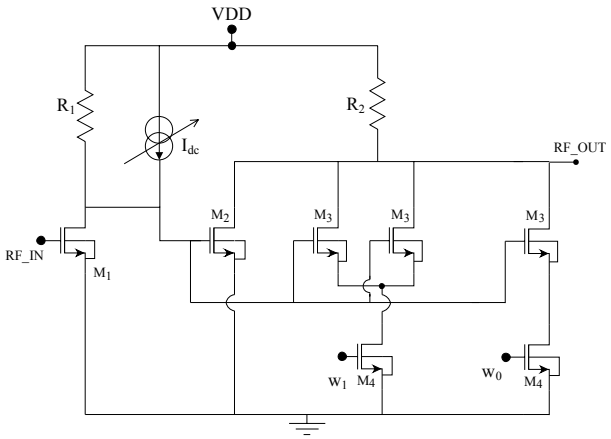

Fig. 4 Schematic of the DC coupled variable gain amplifier.

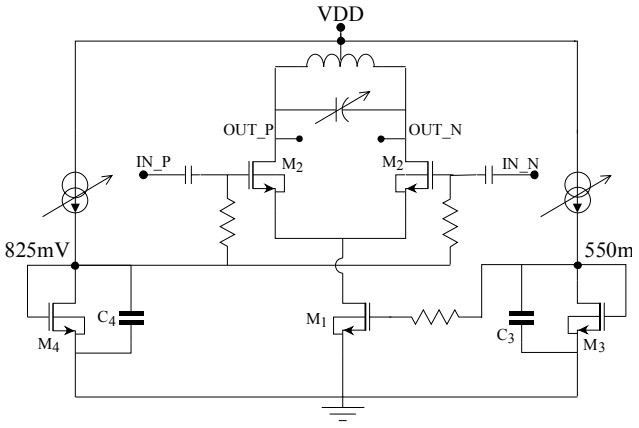

Fig. 5 Schematic of the differential amplifier.

The differential amplifier consists of two input MOS (M_2) devices, a constant tail current provided by M_1 and an LC tank load. To provide variability of the resonance frequency, a variable three bit binary weighted load capacitor is used in the LC tank, where the unit capacitor has a value of 14 fF.

3.5 Distribution Network Block

Schematic of the distribution network is shown in Fig. 6. It is responsible for splitting the RF signal into four branches where each branch is connected to an IQVM. It is a pseudo differential structure, consisting of a variable common source amplifier with resistive load and an LC tank circuit. The inductor is used to resonate the capacitance of the long wiring. The center tap of the inductor provides a bias voltage to the quadrant selection block of the IQVM.

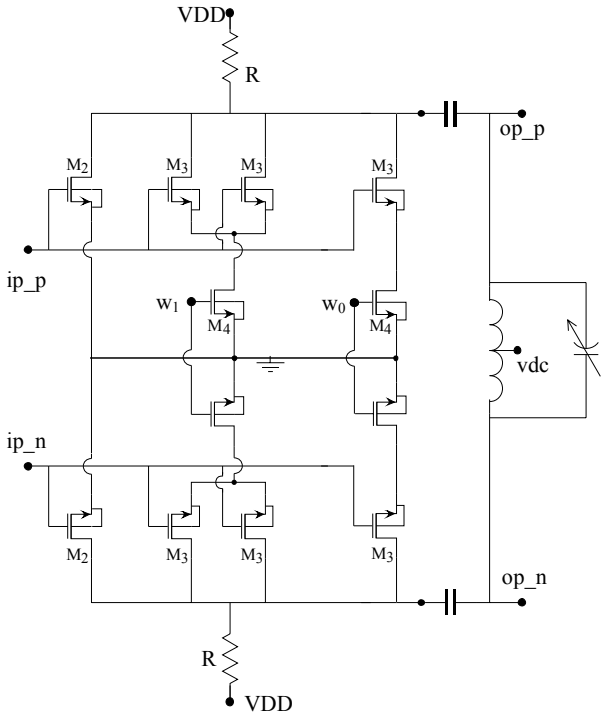

Fig. 6 Schematic of the distribution network.

3.6 IQ Vector Modulator

At block level, the IQVM consists of two sub blocks, the first one is for selecting the sign of the basis vector. The second block is a pseudo differential voltage controlled current source (VCCS), which performs the vector addition, as shown in Fig. 7. In order to change the sign of a vector, cross connected PMOS switches are used. Thus, in total, two bits out of ten are for selecting the appropriate quadrant. As resistive load is used in the summing node, dimensioning for four bits of binary weighted pseudo differential tree becomes difficult because of the limited available voltage swing. To circumvent it, the least significant bit for both I and Q branch is implemented with a unit element, which bleeds only half of the current from the load resistor, with the other half coming directly from the supply. Thus, rather than using 1X, 2X, 4X and 8X size elements, 1X, 1X, 2X and 4X size elements are used in the binary weighted tree. The schematic of the positive side of the binary weighted tree is shown in Fig. 8.

3.7 Driver

The schematic of the driver stage without the biasing structures is shown in Fig. 9. The differential output of the IQVM is converted to single ended using a pseudo-differential amplifier consisting of M_4 to M_7. Transistor

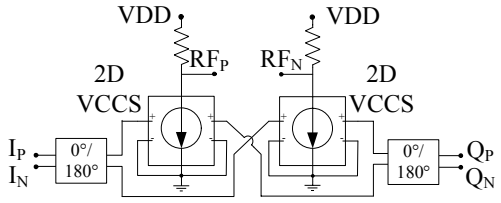

Fig. 7 IQ vector modulator block diagram [11].

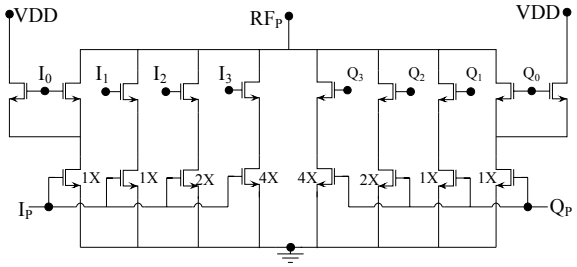

Fig. 8 Positive side of the binary tree used for realizing the VCCS structure used in IQVM. Control bits are numbered from I_0–I_3 and Q_0–Q_3 for I and Q branch respectively [11].

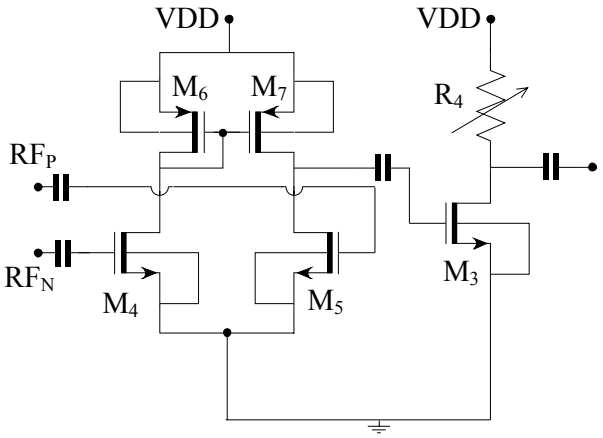

Fig. 9 Simplified schematic of the driver stage.

M_3 is in a common source topology with a variable resistive load, implemented by connecting digitally controlled MOS in parallel to a fixed resistor. The main purpose of it is to provide a coarse gain control. The driver stage is finally followed by a PA implementation, the results of which are shown in [15].

4 Experimental Results

The developed phased array integrated circuit (IC) was fabricated using 45 nm CMOS SOI technology and its micrograph is shown in Fig. 10. The DC power consumed by one channel was measured to be 268 mW and the total power consumed by the four channels was measured to be 1017 mW. The DC power consumed by the LO divider, LO distribution network, and up-conversion block is included in the above mentioned

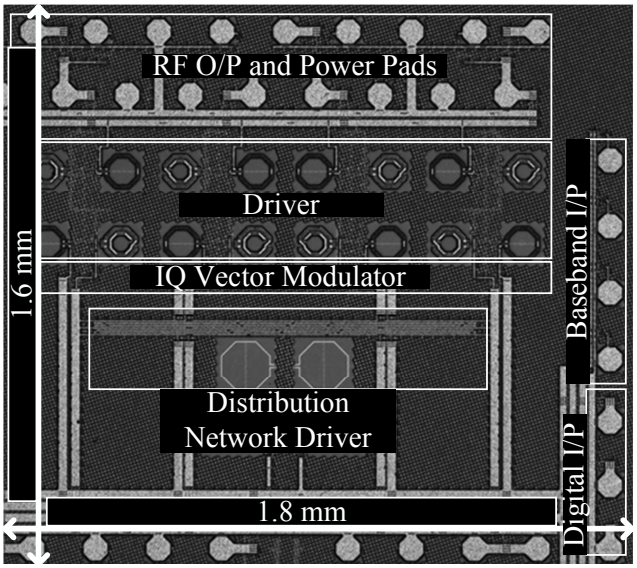

Fig. 10 Chip photograph of the fabricated phased array system.

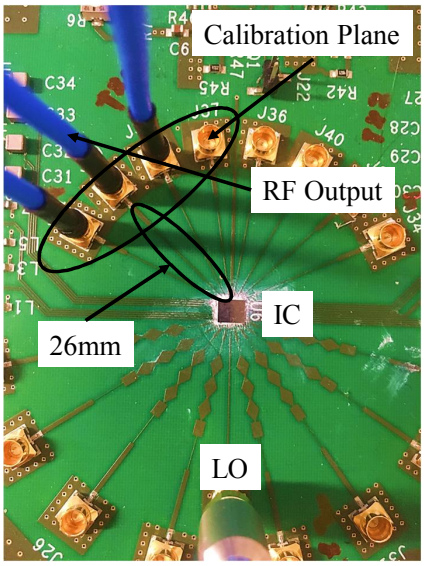

Fig. 11 Photograph of the fabricated PCB.

power results. Excluding PA, which is powered from a 2.6 V source, the IC is powered from 1V supply. The maximum RF power output by one transmit chain was 1 dBm. The dimensions of the phased array, including the input and output pads, is 1.8 mm × 1.6 mm. The IC is flipped and bonded directly onto the printed circuit board (PCB) via solder bumps. The four layer PCB was manufactured using Isola Astra MT77. Due to the lack of on-chip and on-PCB calibration standards, it was not possible to move the calibration plane at the edge of the IC or after the solder bumps, thus for the measurements the calibration plane was at the end of RF cables. As a result , all measured RF results include the impact of PCB traces, ESD diodes, and pad parasitics. The manufactured PCB along with the location of the calibration plane is shown in the Fig. 11.

Two different methodologies were used to measure the phase shift provided by the fabricated devices. For the standalone IQVM [11], as both the input and output were at RF, vector signal measurements were done using Keysight PNA-X N5247A. However, in case of the phased array IC, as the input was at baseband and the output was at RF, direct vector measurements using a vector network analyzer was not possible. Thus, in order to measure the phase shift provided by the device under test (DUT), a fixed sinusoid was sent to the DUT using Rhode & Schwarz vector signal generator. The output signal was analyzed using the Keysight UXA N9040B. The DUT output signal was down converted to an I and Q waveform from which phase information was calculated. An external 10 MHz clock source was used to keep the different instruments in sync. In both cases, no external absolute phase reference was available, thus, a fixed digital control word of the DUT was considered as a reference for all phase measurements. Hence, no calibration was applied to the phase measurements. Since only relative phase and magnitude information was required, the lack of calibration was not a hindrance.

Raw data showing all the 1024 different phase and amplitude points as provided by the standalone IQVM is shown in Fig. 12 [11]. It can be seen from Fig. 12 that available phase constellation is marginally skewed, which implies that the phase difference between the I and Q basis vectors is not 90° but rather close to 85°.

The similar measurement was repeated on one channel of the phased array i.e., control word for the IQVM in one channel was varied without modifying the other three channels. The resulting phase constellation is shown in Fig. 13. It can be seen from Fig. 13 that the measured phase constellation is different compared to the standalone IQVM. Furthermore, it seems that the phase difference between the I and Q basis vectors is now close to 70°. Given that the baseband to RF measurement setup was more complicated compared to RF to RF measurements and the setup was prone to slow phase drifting; it is difficult to gauge how much of the seen impairments are due to the measurement technique. However, the result show a clear indication of coupling from PA and other channels. Hence, the isolation between the channels and from the PA still needs to be improved.

The skew in the basis vectors along with other factors cause the merging of phase constellation points, i.e., points, with similar magnitude have phase differ-

ence less than 1°. After merging these practically indistinguishable points, the normalized phase constellation, i.e., constellation having a maximum amplitude of unity or 0 dB, of all the four IQ vector modulators is plotted on a polar plot in Fig. 14. As the constellation is normalized, the concentric circles in the polar plot represent fixed gain with the outermost circle representing a gain of 0 dB and the innermost a gain of −15 dB.

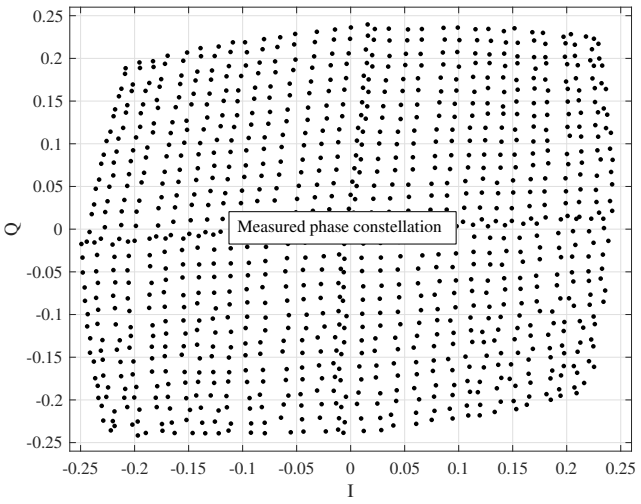

Fig. 12 RF to RF phase constellation measurement data [11].

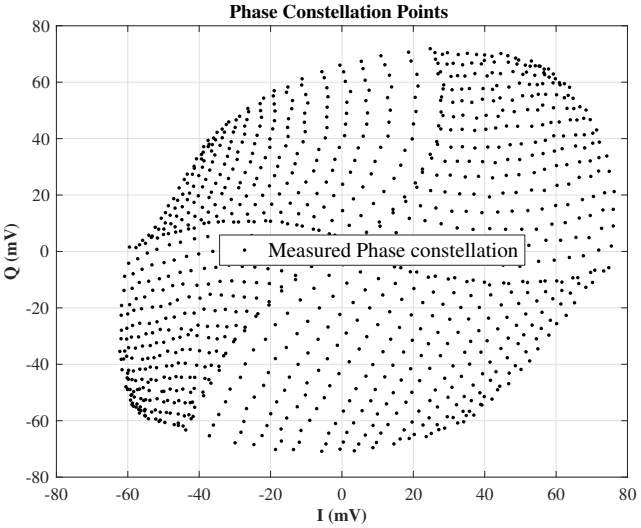

Fig. 13 Baseband to RF phase constellation measurement data from one channel of the phased array.

A key observation from Fig. 14 is that the outer circles have a higher concentration of available phase points as compared to the inner circles, i.e., at lower gain settings, the available phase resolution is limited and the converse is true at higher gain settings. The same behavior is also observed in the ideal IQVM. One must note that although the result shows some imbalance and quadrant dependent phase warping, this is not a detrimental factor for generating phase shifts for a phased array system because the phase resolution is still good and thus, can be calibrated out without major loss of phase resolution.

The available number of unique phase points as a function of their normalized magnitude is plotted in Fig. 15. It also depicts the mean angular separation as a function of normalized gain. To quantify the reduction in control space, the number of effective bits is defined as $\log_2 N_u$, where N_u is the total number of unique phase points over the complete magnitude range. It can be seen from Fig. 14 and Fig. 15 that the behavior of four IQVMs is similar. Compared to an idle IQVM, i.e., one which does not suffer from issues like component mismatch, gain mismatch, or compression, the realized IQVMs suffer marginally in terms of effective number of available control bits.

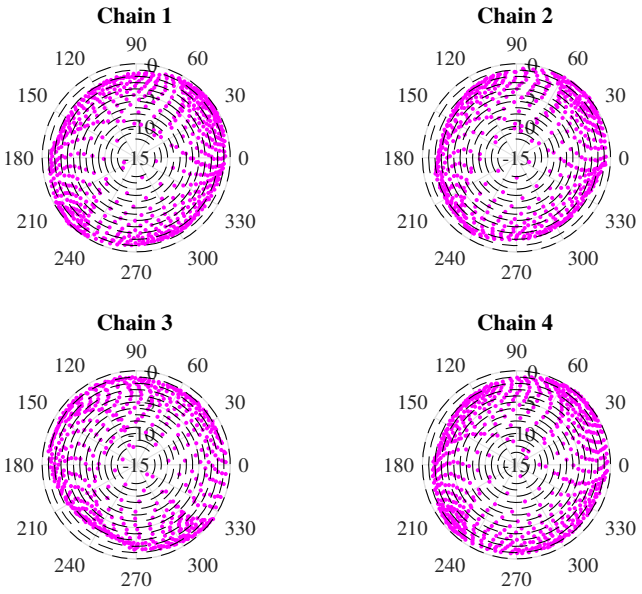

Fig. 14 Phase constellations measured from all four channels of the phased array.

Finally, Fig. 16 depicts the EVM measurements for a single carrier IF signal with the symbol rate of 100 MBd wherein each symbol is modulated with a 256 QAM constellation. The measured EVM for the setup without the DUT is bounded to 1.2% (−38 dB) and with the DUT, the EVM degrades to 2.0% (−34.1 dB). The measurements were done at the output power of −4 dBm. The IQVM itself was configured to provide the maximum signal out. A summary of the key performance parameters is shown in Table 1.

Table 1 Summary of the important performance parameters and comparison with related works.

	This work	[18]	[19]	[20]
Frequency (GHz)	15	70–100	57–64	84–102
Array Size	4	16	16	16
Area (mm^2)[a]	2.8	24.5	16	38.9
Total DC Power (W)	1.0	5.5	1.2	2.2
P_{sat} (dBm)	1[b]	8[b]	8[c]	–5[b]
Constellation	256 QAM	QPSK	64 QAM	-
Technology	45 nm CMOS SOI	SiGe BiCMOS	40 nm LP CMOS	SiGe BiCMOS

[a] Total area of the reported IC. It is a function of the array size.
[b] Saturated RF power transmitted by one channel of the phased array.
[c] Saturated RF power of only the PA.

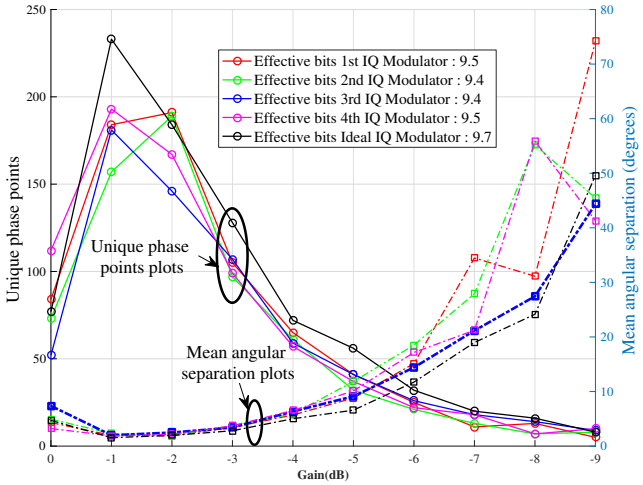

Fig. 15 Number of available unique phase points and angular separation between them at each gain step.

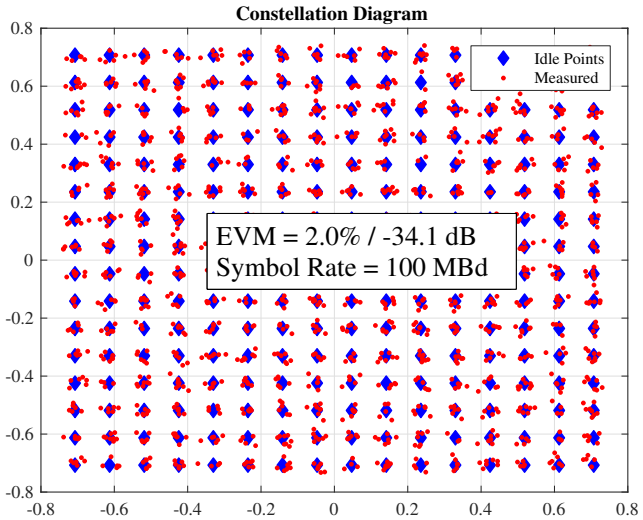

Fig. 16 EVM results for a 256 QAM signal measured at a fixed phase point.

5 Conclusion

This work demonstrates a flip-chip die-on-PCB mounted four channel phased array transmitter IC targeted toward 5G communication systems. The transmitter is operating at a frequency of 15 GHz and is linear enough to support dense constellations like 256 QAM. The phase shift for the phased array is provided at RF frequency using an IQ vector modulator. It provides full 360° phase shift along with 15 dB of gain variation, which is required for beam tapering. The mean angular separation between phase points is 3° at optimum amplitude levels. Each channel is capable of transmitting 1 dBm of output power. The phase shift and EVM measurements were done at a back-off of 5 dB.

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