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COMMUNICATIONS

TRANSFER LOGIC GATES WITH ELECTRICAL AND OPTICAL INPUTS FOR LARGE AREA ELECTRONICS

Zsolt J. Horváth *

A new type of transfer logic gates with both electrical and/or optical inputs and electrical outputs are proposed, which can be prepared by thin film technology. The possible realization of different logic functions and non-volatile memory logic arrays are demonstrated. The possible application fields are briefly discussed.

K e y w o r d s: thin films, organic electronics, transfer logic gates and arrays, electrical and optical inputs, non-volatile memory

1 INTRODUCTION

Nowadays signal and information processing are performed mainly with logic integrated circuits (ICs), analog ICs are applied mainly for sensors, actuators, power electronics and special purposes. On the other hand, optical data transmission and processing take wider and wider part in information technology. So, the possibility of combination of electrical and optical signals inside an electronic device or circuit can provide a great advantage.

The research of organic logic devices and arrays is an intensely developing field either. Not only device structures and discrete devices are widely studied [1, 2], but logic arrays are developed either [3, 4].

In this paper a new type of logic gates with both electrical and/or optical inputs and electrical outputs is proposed for possible application in large area thin film and organic electronics. The basic element of the proposed gates is a transfer gate. Using such gates logic arrays for different logic functions can be constructed with parallel electrical and optical inputs and non-volatile memory arrays can be built as well.

2 DEVICE STRUCTURE

The proposed logic gates and circuits are based on a semiconductor active layer with high resistivity grown on an isulating or semiinsulating substrate. The active layer can act as a conductive channel between source and drain electrodes, similarly to thin film transistors or photoresistors, as shown in Fig. 1.

The active layer is covered by an insulator layer, which is transparent for input optical signals (light beams). Free charge carriers are generated in conductive channels by the optical signals with appropriate photon energy. The spots of adjacent light beams overlap and beam spots form a geometrical band, which determine the width of the conductive channel. But the second adjacent spots are far from each other, more far, than the diffusion length of the generated charge carriers.

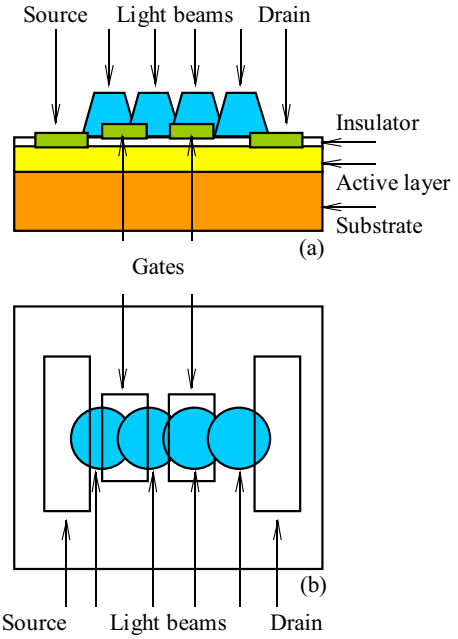

Fig. 1. The structure of proposed devices: (a) — schematic cross-section, (b) — topology of a transfer gate with 4 optical and 2 electrical inputs

Metal gates, which are electrically conductive and transparent or semitrasparent for optical signals, are formed on the top of the upper insulator layer. Gates overlap the whole width of the conductive channel of the device. (If the substrate is transparent for optical signals, they can be introduced from bottom side. In this case gates should not be transparent for light.) Conduc-

* Óbuda University, Kandó Kálmán Faculty of Electrical Engineering, Institute of Microelectronics and Technology, Tavaszmező u. 17, Budapest, H-1084 Hungary; Hungarian Academy of Sciences, Centre for Energy Research, Institute for Technical Physics and Materials Science, Budapest, PO Box 49, H-1525 Hungary, horvath.zsolt@kvk.uni-obuda.hu

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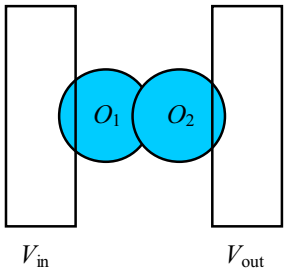

Fig. 2. Transfer AND gate with two optical inputs

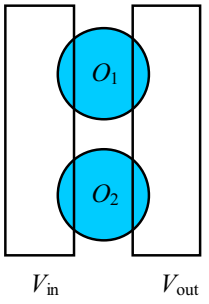

Fig. 3. Transfer OR gate with two optical inputs

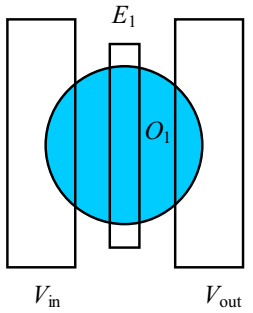

Fig. 4. Transfer AND gate with one optical and one electrical inputs

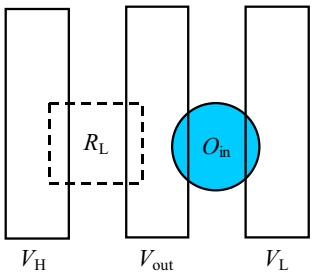

Fig. 5. The realization of inverter requires the formation of a load resistor R_L. V_H and V_L are the High and Low logic

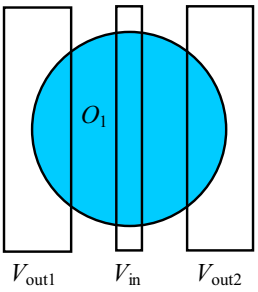

Fig. 6. Transfer gate with one optical input and two electrical outputs

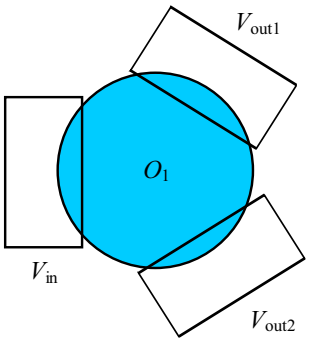

Fig. 7. Another possible topology of a transfer gate with one optical input and two electrical outputs

tive channels can be closed under the gates by an appropriate voltage value applied to a gate. So, gates are input ports for electrical signals. In principle, the device can be formed on a Metal-Semiconductor (MS) structure without an upper insulator layer as well instead of a Metal-Insulator-Semiconductor (MIS) structure described above. In this case Schottky gates can be used for electical inputs.

Another possibility is to form electrical gates below the conductive channel on the back side of substrate. In this case gates should not be transparent optically either.

The channel is conductive between source and drain only, if all optical signals are switched on and such a potential is applied to all electrical gates, which does not close the channel. Different logic gates can be constructed with both electrical and/or optical inputs and electrical outputs. It should be underlined that the output signal is always electrical.

If the top insulator (mono- or multi)layer can store electrical charge (Si_3N_4, Al_2O_3, SiO_2/Si_3N_4, *etc*), the channel can be closed by the appropriate charge amount stored in the top insulator layer. This charge can be injected into the top insulator layer by voltage pulses applied to one or more gates. The charge can be erased by voltage pulses of opposite sign and the channel will be conductive again under light radiation. As the injected charge can be stored for a long time, non-volatile memories can be constructed, which can be programmed electrically and read optically with electrical output signal. Further on, logic functions can be realized as well by these non-volatile memory devices.

3 LOGIC GATES AND ARRAYS

Different logic gates and arrays can be realized by using the proposed device idea and structure. A few examples are presented below, but the number of possible logic arrays built up on the basis of the proposed structure is much higher.

The structure presented in Fig. 1 is a transfer AND gate, which realizes the logic function $V_{out} = O_1 * O_2 * O_3 * O_4 * \underline{E}_1 * \underline{E}_2 * V_{in}$ where O_1, O_2, O_3, and O_4 are the optical input signals, and $\underline{E}_1$ and $\underline{E}_2$ are the inverted electrical signals. For non-inverted electrical signals that potential is considered, which closes the channel.

In the case of two optical inputs two simple logic functions can be realized: transfer AND gate $V_{out} = O_1 * O_2 * V_{in}$ (see Fig. 2) and transfer OR gate $V_{out} = (O_1 + O_2) * V_{in}$ (Fig. 3).

In the case of one optical and one electrical inputs transfer NAND gate, *ie*, $V_{out} = O_1 * \underline{E}_1 * V_{in}$ logic function can be realized only (Fig. 4).

Unfortunately, the realization of inverter, which is the basic element of the MOS logic circuits, is difficult using the proposed structure. It requires the formation of a load resistor R_L, and it is possible for optical input signal only, as shown in Fig. 5. The realized logic function is $V_{out} = \underline{O}_{in}$, *ie*, the gate inverts the input optical signal. But, the formation of a load resistor requires additional technological steps. However, an external load resistor can also be applied, which is connected in series to the power voltage. The load resistance should be much higher than that of the open channel, but much lower, than that of

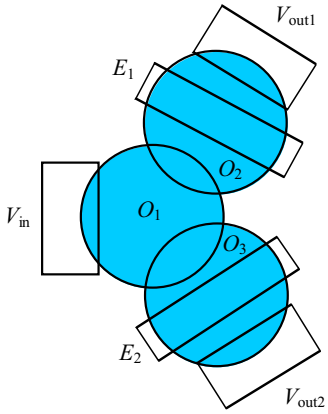

Fig. 8. Transfer gate with three optical and two electrical inputs and two electrical outputs

the closed channel. It is optimal, if the load resistance equals the geometric mean value of resistances of open and closed channel. As a resistance ratio between the open and closed channel of 1 : 100 can be easily reached, the deviation of output High and Low logic levels from their nominal values is less or about 10 %.

Controlled signal branching to more outputs can be realized either. Two possible topologies of a transfer gate with one optical input and two electrical outputs are presented in Figs. 6 and 7. The O_1 optical signal opens the channel from the input to both outputs. The input signal can be transferred to one or to the other output separately as well, if two optical signals are used to open the channels between V_{in} and V_{out1} or V_{in} and V_{out2}, respectively.

The topology of a transfer gate with three optical and two electrical inputs and two electrical outputs is shown in Fig. 8. The logic functions are as follows: $V_{out1} = O_1 * O_2 * \underline{E}_1 * V_{in}$ and $V_{out2} = O_1 * O_3 * \underline{E}_2 * V_{in}$. So, the input signal can be transferred to one or to the other output or to both of them.

Due to voltage drop on channel the number of optical inputs connected in series is limited. The power voltage value (which is usually used as logic high level) should be higher, than the gate voltage, which is necessary to close the channel. Its value depends on the number of optical inputs connected in series.

In general, the logic high level can be recovered between two logic gates connected in series by inserting two series inverters. The output of the second inverter is the recovered right logic value of the output signal of the preceding logic gate. But, unfortunately, this method cannot be used in the proposed structures, as inverters with electrical input cannot be realized in a reasonable way. A main advantage of the proposed structures is their realization by a simple technology. The realization of inverters with electrical input requires a more complicated technology.

4 POSSIBLE APPLICATIONS

As the response time between the optical input signals and the electrical output signals is relatively long (it depends on the generation/recombination rates), and the minimum channel width is expected in μm range (a few optical wavelengths of input signals), the proposed logic devices and arrays can find application in such special fields only, where the optical input signals are necessary or advantageous in thin film or wide band gap semiconductor circuits. Possible fields of application are the large area thin film and/or organic electronics, *eg*, control circuits for solar cell arrays, where the operating speed and device dimensions are not critical, but the price is very important.

5 CONCLUSION

A new type of transfer logic gates with both electrical and/or optical inputs and electrical outputs has been proposed that can be realized by thin film technology. They are based on a semiconductor active layer with high resistivity grown on an isulating or semiinsulating substrate. The active layer can acts as a conductive channel between source and drain electrodes, similarly to thin film transistors or photoresistors. The possible realization of different logic functions has been demonstrated. The possible application fields have been briefly discussed.

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Zsolt J. Horváth graduated from the Kiev Politechnik Institute (Technical University) as electrical engineer in 1973. He received PhD degree from the Budapest Technical University in 1994 and degree of Doctor of the Hungarian Academy of Sciences in 2009. At present he is a professor at the Óbuda University, Budapest. His scientific activity covered the physics and electrical characterization of different semiconductor structures and devices. The two main areas have been the research of Schottky junctions and non-volatile semiconductor memories.