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Frequency limitation of an optimum performance class-E power amplifier

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Abstract: Class-E power amplifiers have found widespread application because of their design simplicity and high-efficiency operation. The nonlinear characteristic of the switching device significantly affects the power amplifier performance, although this is often neglected in theoretical analyses. In this paper, a class-E power amplifier with a shunt capacitance composed of nonlinear and linear capacitance has been mathematically analyzed to obtain the frequency limitation that governs maximum efficiency operation. The analytical method is presented to determine the effective operating frequency for any model of MOSFET device. The practical power amplifier circuit, using a MRF282 MOSFET, was implemented to verify the validity of the theoretical analysis.

Keywords: class-E, high efficiency, power amplifier (PA), nonlinear shunt capacitance, frequency limitation

Classification: Electron devices, circuits, and systems

References

[1] N. O. Sokal: IEEE MTT-S Int. Microw. Symp. Dig. (1998) 1109. DOI:10.1109/MWSYM.1998.705187

[2] N. O. Sokal and A. D. Sokal: IEEE J. Solid-State Circuits **SC-10** (1975) 168. DOI:10.1109/JSSC.1975.1050582

[3] A. Grebennikov and N. O. Sokal: *Switchmode RF Power Amplifiers* (Newnes, 2007) 2nd ed. 179.

[4] Y. Park and H. Yoon: J. Electromagn. Eng. Sci. **15** [1] (2015) 53. DOI:10.5515/JKIEES.2015.15.1.53

[5] M. J. Chudobiak: IEEE Trans. Circuit Syst. I, Fundam. Theory Appl. **41** (1994) 941. DOI:10.1109/81.340867

[6] H. V. Nam and C. Seo: IEICE Electron. Express **11** (2014) 20140682. DOI:10.1587/elex.11.20140682

[7] P. Alinikula, K. Choi and S. I. Long: IEEE Trans. Circuit Syst. II, Analog Digit. Signal Process. **46** (1999) 114. DOI:10.1109/82.752911

[8] X. Wei, H. Sekiya, S. Kuroiwa, T. Suetsugu and M. K. Kazimierczuk: IEEE Trans. Circuits Syst. I, Reg. Papers **58** (2011) 2556. DOI:10.1109/TCSI.2011.2123490

[9] A. Mediano, P. M. Gaudó and C. Bernal: IEEE Trans. Microw. Theory Techn.

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Copyedited April 10, 2016

55 (2007) 484. DOI:10.1109/TMTT.2006.890512
[10] T. Suetsugu and M. K. Kazimierczuk: IEEE Trans. Circuits Syst. I, Reg. Papers **51** (2004) 1261. DOI:10.1109/TCSI.2004.830695

1 Introduction

Power amplifier (PA) systems are required to reduce power consumption significantly so as to maximize the system performance. Power added efficiency (PAE) is the most important factor by which such performance is validated. The switch-mode amplifier structure has been proposed for obtaining high efficiency; the switch-mode class-E amplifier with a shunt capacitor produced by Sokal has an efficiency that, theoretically, reaches up to 100% [1, 2, 3, 4]. However, the operation of the linear shunt-capacitance class-E amplifier in theoretical analysis is different from that of an actual class-E amplifier. The parasitic drain-to-source capacitance of the switch device is nonlinear, which contributes significantly to the overall shunt capacitance in the operation [5, 6, 7]. Therefore, it is necessary to take into account the nonlinear behavior of this capacitance.

In this paper, the class-E power amplifier circuit is analyzed, and its design is based of the composition of nonlinear and linear shunt capacitance. The zero-voltage-switching (ZVS) and zero-derivative-switching (ZDS) conditions are satisfied, which ensure zero switching loss and improve component tolerances [8, 9]. Furthermore, in order to design an accurate power amplifier circuit, it is necessary to consider adequately the frequency limitation of an active device. As such, the metal-oxide-semiconductor field-effect transistor (MOSFET) possesses an intrinsic output capacitance, and together with the given dc supply voltage and output power, the operating frequency limitation should be determined if the amplifier is to maintain maximum efficiency operation. If the operating frequency exceeds the limited value, the class-E amplifier cannot satisfy the ZVS and ZDS conditions. The objective of this paper is to present an expression for the frequency limitation of the MOSFET class-E power amplifier composed of linear and nonlinear shunt capacitances. In addition, an example design has been implemented to validate the influence of the frequency selection on the optimized performance.

2 Frequency limitation of class-E amplifiers

In [10], Tadashi Suetsugu proposed an analysis method and design for class-E amplifiers with both linear and nonlinear shunt capacitances. The supporting figures and tables that contain results of a numerical analysis of the design equations are used to extract the component values for the class-E amplifier. However, the design equations of an arbitrary MOSFET depend on its own parameters, such as the output capacitance, the reverse transfer capacitance of the transistor, etc. Therefore, in order to design such a class-E power amplifier, the equations should be solved for a certain MOSFET. In this section, we re-analyze the circuit mathematically to derive the parameters for the class-E amplifier, and extract the component values and the highest operation frequency.

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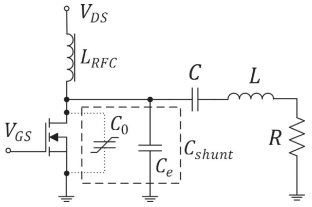

Fig. 1. Basic circuit of the class-E PA.

A conventional circuit of the class-E amplifier with a shunt capacitance is illustrated in Fig. 1. This circuit includes a dc-supply drain voltage a V_{DS}, a gate voltage V_{GS}, a choke inductor L_{RFC}, a MOSFET as a switch device, the series resonant RLC circuit, the shunt capacitance consisting of the MOSFET drain-to-source capacitance C_0, and the external linear capacitance C_e. The total shunt capacitance of the class-E power amplifier circuit is described by:

$$C_{shunt} = C_0 + C_e = \frac{C_{j0}}{\sqrt{1 + \dfrac{v_S}{V_{bi}}}} + C_e \tag{1}$$

where C_{j0} is the shunt capacitance at the drain-to-source voltage $v_S = 0\,\mathrm{V}$ and V_{bi} is the built-in potential of the MOSFET body diode.

The switch voltage is supposed to satisfy the ZVS condition at the turn-on period. Because the dc voltage across the choke inductor L_{RFC} is zero, the average value of the switch voltage is equal to the dc supply voltage V_{DS}:

$$V_{DS} = \frac{1}{2\pi}\int_0^{2\pi} v_S(\theta)d\theta \tag{2}$$

where v_S is the drain-to-source voltage. When the switch is off (i.e., for $0 < \theta = \omega t \leq \pi$), v_S can be extracted from the integration of the drain current equation:

$$\omega\int_0^{v_S}\left(\frac{C_{j0}}{\sqrt{1 + \dfrac{v_S}{V_{bi}}}} + C_e\right)dv_S = \int_0^{\theta} i_C d\theta \tag{3}$$

Substituting v_S into Eq. (2), then, partly expanding as follows, yields:

$$\begin{aligned}\frac{V_{DS}}{V_{bi}} = \frac{\alpha}{\pi}\left[\pi(\alpha + \beta\sin\phi\cos\phi + 1) + \beta\left(\frac{\pi^2}{2} + 2\right)\sin^2\phi\right] \\ - \frac{\alpha}{\pi}\int_0^{\pi}[\alpha^2 + 2\alpha + 1 + 2\alpha\beta\sin\phi\cos\phi \\ + 2\alpha\beta\theta\sin^2\phi - 2\alpha\beta\sin\phi\cos(\theta + \phi)]^{\frac{1}{2}}d\theta\end{aligned} \tag{4}$$

where:

$$\alpha = \frac{C_{j0}}{C_e} \tag{5}$$

$$\beta = \frac{(\pi^2 + 4)P_o}{16\pi f_o C_{j0} V_{bi} V_{DS}} \tag{6}$$

and ϕ is the phase difference between input and output signals.

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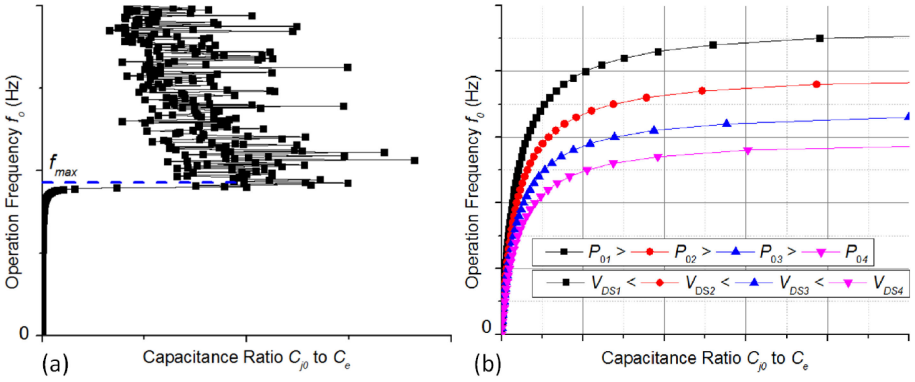

Fig. 2. (a) Operation frequency as a function of capacitance ratio; (b) The dependence of operation frequency f_o on various V_{DS} and P_o values.

The relation between the frequency f_o and the given parameters, including the capacitance ratio α of C_{jo} to C_e, the dc supply voltage V_{DS}, and the output power P_o is demonstrated in Eq. (4), which could not be integrated to obtain an analytical solution. The solution is plotted in Fig. 2(a), which depicts the dependence of the operating frequency f_o upon α for the given values of V_{DS} and P_o. It is obvious that the dependence of f_o on α is represented in two regions: the linear dependence region and the *perturbation* dependence region. In the former region, each value of α corresponds to only one frequency f_o, which satisfies the boundary conditions for maintaining the optimized performance of a class-E amplifier. Consequently, the external capacitance C_e can be obtained from the capacitance ratio α by calculating the junction capacitance C_{j0}, as in the following equation [10]:

$$C_{j0} = (C_{oss} - C_{rss})\sqrt{1 + \frac{25}{V_{bi}}} \tag{7}$$

where C_{oss} and C_{rss} are the output capacitance and reverse transfer capacitance of the transistor, respectively, and which are often provided in the manufacturer catalogs of power MOSFETs. In Eq. (4), the junction capacitance C_{j0} is a variable of β, which depends on the parasitic parameters of the specific transistor. Therefore, the solution of Eq. (4) is only derived for the specific transistor, which has the extracted junction capacitance C_{j0}.

In contrast, the dependence between f_o and α is extraordinary in the perturbation region. It is conducive to the irrelevant determination of accurate operation frequency. The separation of these regions is distinguished by the maximum frequency, f_{max}, which is the frequency limitation for the MOSFET class-E power amplifier. It may be seen that the decline in the value of C_{jo} leads to the increment of f_{max} with the same conditions and vice versa. Therefore, based on the highest operation frequency derived for the given MOSFET, the frequency can be chosen to provide the highest efficiency within the methodology of class-E design.

In addition, it is shown that the maximum operating frequency of the class-E power amplifier can be changed by varying the given supply voltage and the given output power. Fig. 2(b) shows the relation between the frequency f_o and the various V_{DS} and P_o values. The increased drain voltage results in the decrease of

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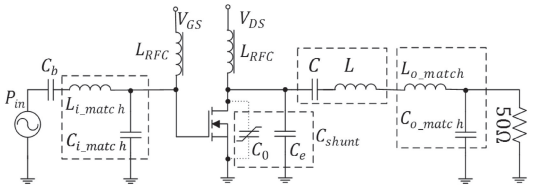

Fig. 3. Completed class-E power amplifier circuit.

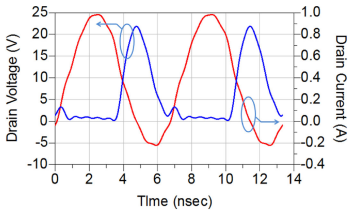

Fig. 4. Drain current and voltage simulation waveforms of a class-E power amplifier circuit.

the maximum frequency; whereas, the latter will increase if the output power increases. Based on these relations, the output power and supply voltage need to be properly appointed so that the drain-to-source current, $I_{DS} = P_o/V_{DS}$, does not surpass through the active device. A high I_{DS} value leads to an increase in the thermal effects caused by the parasitic saturation resistances of the transistor.

3 Circuit design and measurement

The proposed techniques for finding the operation frequency limitation were validated by fabricating a class-E PA using a MRF282 MOSFET. From the analysis in the previous section, the schematic of the completed class-E PA circuit is modeled in Fig. 3. The class-E PA circuit is implemented with a selected operation frequency, f_o, lower than the maximum frequency, f_{max}. Moreover, the highest operation frequency, f_{max}, of approximately 170 MHz is derived by substituting the appropriate parameters into Eq. (4). The designed class-E PA at an operating frequency, f_o, of 150 MHz has a high PAE of 85.3% for a supply voltage of 6 V and an output power of 2 W.

The voltage and current simulation waveforms are depicted in Fig. 4 under the optimum operation; they overlap each other slightly, resulting in a minimized power dissipation by the transistor. The voltage across the switching device is presumed to satisfy the ZVS and ZDS conditions. Fig. 5(a) presents the experimental fabrication for the proposed circuit. Fig. 5(b) shows the comparison between the simulated and experimental results of the gain and PAE, which are in good agreement. The power gain and PAE of the experimental results are slightly lower than the simulation results.

A design of the class-E PA circuit with an operation frequency higher than the maximum frequency was fabricated to compare its performance with the proposed circuit, as shown in Table I. From these values, it is clear that the class-E PA with a high frequency of 180 MHz is achieves low efficiency and low output power. Using the same given parameters as before, the output power in this case is insufficient as the expected power, followed by the low efficiency of 72% PAE. In addition, the

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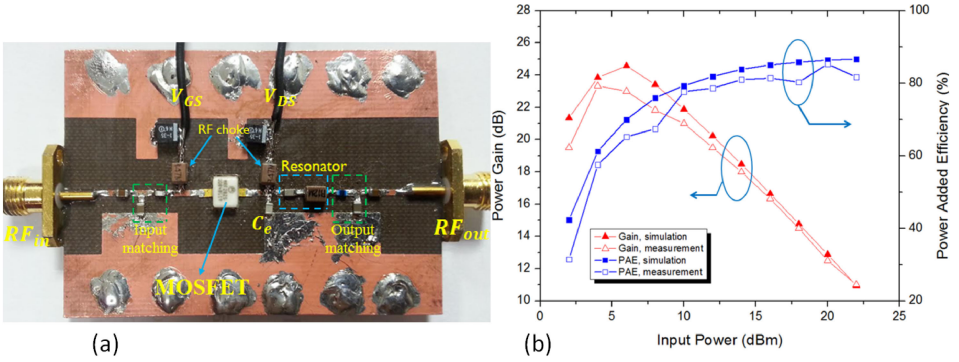

Fig. 5. (a) The fabrication of the class-E power amplifier; (b) Gain and PAE results in simulation and measurement.

Table I. Comparison results

Parameters	Proposed Design	Compared Design
V_{DS} (V)	6	6
V_{GS} (V)	3.2	3.2
I_{DS} (mA)	368	440
I_{GS} (mA)	0	0
C_e (pF)	3.3	0.5
f_o (MHz)	150	180
P_{in} (dBm)	20.5	20.5
P_o (dBm)	33	32.5
PAE (%)	85.3	72

drain-to-source current increases strongly, which is conducive to the dissipation of power by thermal loss from the parasitic saturation resistance. Consequently, the operating frequency for a class-E PA using a MOSFET should be appointed restrictively to achieve the high performance with the composition of linear and nonlinear shunt capacitances.

4 Conclusion

This paper has presented the analytical method for deriving the maximum operation frequency for a MOSFET class-E PA with linear and nonlinear shunt capacitance composition. The relation between the operation frequency and the given parameters, including supply voltage and output power, is taken into account in detail. The practical class-E PA circuit was fabricated to verify the accurate frequency selection for the arbitrary MOSFET.

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