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Research Article

Signal Integrity Analysis in Single and Bundled Carbon Nanotube Interconnects

Manoj Kumar Majumder, Nisarg D. Pandya, B. K. Kaushik, and S. K. Manhas

Microelectronics and VLSI Group, Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee, Roorkee, Uttarakhand 247667, India

Correspondence should be addressed to Manoj Kumar Majumder; manojbesu@gmail.com

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Carbon nanotube (CNT) can be considered as an emerging interconnect material in current nanoscale regime. They are more promising than other interconnect materials such as Al or Cu because of their robustness to electromigration. This research paper aims to address the crosstalk-related issues (signal integrity) in interconnect lines. Different analytical models of single- (SWCNT), double- (DWCNT), and multiwalled CNTs (MWCNT) are studied to analyze the crosstalk delay at global interconnect lengths. A capacitively coupled three-line bus architecture employing CMOS driver is used for accurate estimation of crosstalk delay. Each line in bus architecture is represented with the equivalent *RLC* models of single and bundled SWCNT, DWCNT, and MWCNT interconnects. Crosstalk delay is observed at middle line (victim) when it switches in opposite direction with respect to the other two lines (aggressors). Using the data predicted by ITRS 2012, a comparative analysis on the basis of crosstalk delay is performed for bundled SWCNT/DWCNT and single MWCNT interconnects. It is observed that the overall crosstalk delay is improved by 40.92% and 21.37% for single MWCNT in comparison to bundled SWCNT and bundled DWCNT interconnects, respectively.

1. Introduction

Advancement of VLSI technology leads to the development of high-speed complex integrated circuits (ICs) in current nanoscale regime. Due to shrinking feature sizes and increasing clock frequency, interconnect plays an important role in determining the overall circuit performance. Therefore, in recent technology, interconnect delay dominates over the gate delay. The global interconnects are widely employed to distribute data, clock, power supply, and ground throughout the entire area of an IC. At global interconnect, most materials (such as Al or Cu) are susceptible to electromigration due to higher current density. This electromigration problem substantially affects the reliability of high-speed VLSI circuits. To avoid such problems, researchers are forced to find an alternative solution for global VLSI interconnects.

Carbon nanotubes (CNTs) can be considered as alternative interconnect material in current nanoscale regime. After discovery in 1991 [1], CNTs have received tremendous research interest for their unique mechanical [2], electrical [3], thermal [4], and chemical properties [5]. The sp_2 bonding in graphene is even stronger than the sp_3 bonds in diamond that gives CNTs extremely high mechanical strength [6]. The unique electrical and thermal properties are primarily due to the movement of electrons in one-dimensional (1D) systems. Due to the 1D movement, electrons can be scattered only in backward direction [5]. Therefore, mean free path (*mfp*) in high-quality nanotubes is in the range of micrometer. This is in contrast to a three-dimensional (3D) metallic wire in which electrons can be backscattered by a series of small-angle scatterings, and therefore, *mfps* are in the range of few tens of nanometers [7]. Due to long *mfp*, CNTs can exhibit the ballistic transport phenomenon which is responsible for their outstanding electrical and thermal behaviour. Moreover, an isolated CNT can carry current densities up to 10^9 A/cm^2 at an elevated temperature of

250°C [7], thereby eliminating electromigration reliability concern. Due to these extraordinary properties, CNTs are suitable for a variety of applications in the areas of microelectronics/nanoelectronics [8], spintronics [9], optics [10], material science [11], and mechanical [12] and biological fields [13].

CNTs, known as allotropes of carbon [1], are cylindrically rolled-up sheets of graphene. Graphene is a two-dimensional sheet of graphite that exhibits honeycomb lattice arrangement among the carbon atoms [6]. Based on the number of rolled-up graphene sheets, CNTs are classified into single- (SWCNT) and multiwalled CNTs (MWCNT). Double-walled CNT (DWCNT) is a special type of MWCNT wherein only two concentrically rolled-up graphene sheets are present. Due to structural simplicity, SWCNTs have attracted more attention than DWCNTs and MWCNTs. Significant progress has been achieved in the characterization of interconnect performances of SWCNT bundle and MWCNT [7, 14]. For example, compact physical models were developed for MWCNTs and bundled SWCNTs for different number of conducting channels [15], and performance prediction of bundled SWCNTs for on-chip interconnects was demonstrated in [16]. Diameter-dependent model was analyzed for bundled SWCNT and MWCNT interconnects in [17], and their performances were compared [18] against Cu/low-k wires for future high-performance ICs. Performance in terms of crosstalk is an important design concern in current nanoscale VLSI interconnects. Crosstalk in coupled lines can be broadly classified into two categories: (1) functional and (2) dynamic crosstalk [19, 20]. Under functional crosstalk category, victim line experiences a voltage spike when an aggressor line switches [21]. On the other hand, dynamic crosstalk is observed when aggressor and victim line switches simultaneously. A change in signal propagation delay is experienced under dynamic crosstalk when adjacent line (aggressor and victim) switches either in phase or out of phase. Using parallel SWCNTs or single MWCNT, crosstalk-induced delay and peak voltages were first observed by Rossi et al. [14] in three-line bus architecture. Again, in 2009, Chen et al. [22] reported that at high biasing voltages, SWCNT interconnect arrays were significantly affected by dynamic crosstalk delay.

Based on the interconnect geometry predicted by ITRS 2012 [23], propagation delay under the influence of dynamic crosstalk is analyzed for equivalent *RLC* models of MWCNT and bundled SWCNT/DWCNT at global interconnect lengths. Using a capacitively coupled three-line bus architecture employed by metallic nanotube, it is observed that crosstalk delays are significantly improved in MWCNT as compared to the bundled SWCNT/DWCNT interconnects. The organization of this paper is as follows. Section 1 introduces the recent research scenario and briefs about the works carried. Based on the geometry and bundle arrangements, Section 2 describes the equivalent *RLC* models of bundled SWCNT/DWCNT and single MWCNT interconnects. A detailed description about the three-line bus architecture is provided in Section 3 whereas Section 4 analyzes the crosstalk delays for different single and bundled CNT interconnects. Finally, Section 5 draws a brief summary of this paper.

2. Geometry and Equivalent *RLC* Models

This section presents the geometry and equivalent *RLC* models of bundled SWCNT, bundled DWCNT, and single MWCNT interconnects. Figure 1(a) shows a bundled SWCNT (height = h and width = w) that consists of numbers of SWCNTs with diameter d and spacing S_p. The total number of SWCNTs in a bundle can be calculated as [7, 24]

$$n_{\mathrm{CNT}} = n_W n_H - \left(\frac{n_H}{2}\right), \qquad n_{\mathrm{CNT}} = n_W n_H - \left(\frac{n_H - 1}{2}\right) \quad (\text{if } n_H \text{ is an even and odd number, resp.}), \tag{1}$$

where

$$n_W = \left\lfloor \frac{w - d}{S_p} \right\rfloor + 1, \qquad n_H = \left\lfloor \frac{h - d}{S_p} \right\rfloor + 1. \tag{2}$$

n_H and n_W are number of rows and columns, respectively, n_{CNT} is the total number of CNTs in bundle, and $\lfloor N \rfloor$ indicates the largest integer which is less than or equal to N. Similarly, Figure 1(b) exhibits the arrangement of bundled DWCNT that considers n number of DWCNTs and are calculated using (1) and (2). DWCNT can be considered as the simplest geometry of an MWCNT. An MWCNT consists of n number of shells with different diameters of $D_1, D_2, D_3, \ldots, D_n$, where D_1 and D_n are the inner and outer shell diameters, respectively, as shown in Figure 1(c). In current fabrication process, the intershell spacing of MWCNT can be calculated as [14]

$$S_i = \frac{D_n - D_{n-1}}{2} \approx 0.34\,\mathrm{nm}. \tag{3}$$

Based on geometry and bundle arrangements, the equivalent *RLC* models of bundled SWCNT, bundled DWCNT and single MWCNT are shown in Figures 2, 3, and 4, respectively. The total bundle resistance can be divided into two categories: R_{l-b} and R_{d-b}, depending on and independent of the bundle lengths, respectively. Thus, R_{l-b} and R_{d-b} can be expressed as [7]

$$R_{l-b} = \frac{(R_C + R_Q)}{n_{\mathrm{CNT}}}, \qquad R_{d-b} = \frac{R_Q}{n_{\mathrm{CNT}}}, \tag{4}$$

where R_C is the metal nanotube contact resistance with a typical value of 3.2 KΩ and R_Q is the fundamental quantum resistance that can be expressed as [25]

$$R_Q = \frac{h}{4e^2} \approx 6.45\,\mathrm{K\Omega}. \tag{5}$$

Additionally, the bundled DWCNT and single MWCNT consider intershell tunneling conductance (G_t) which is primarily due to the electron tunnel transport phenomenon between two shells [26]. Apart from this, the total bundle

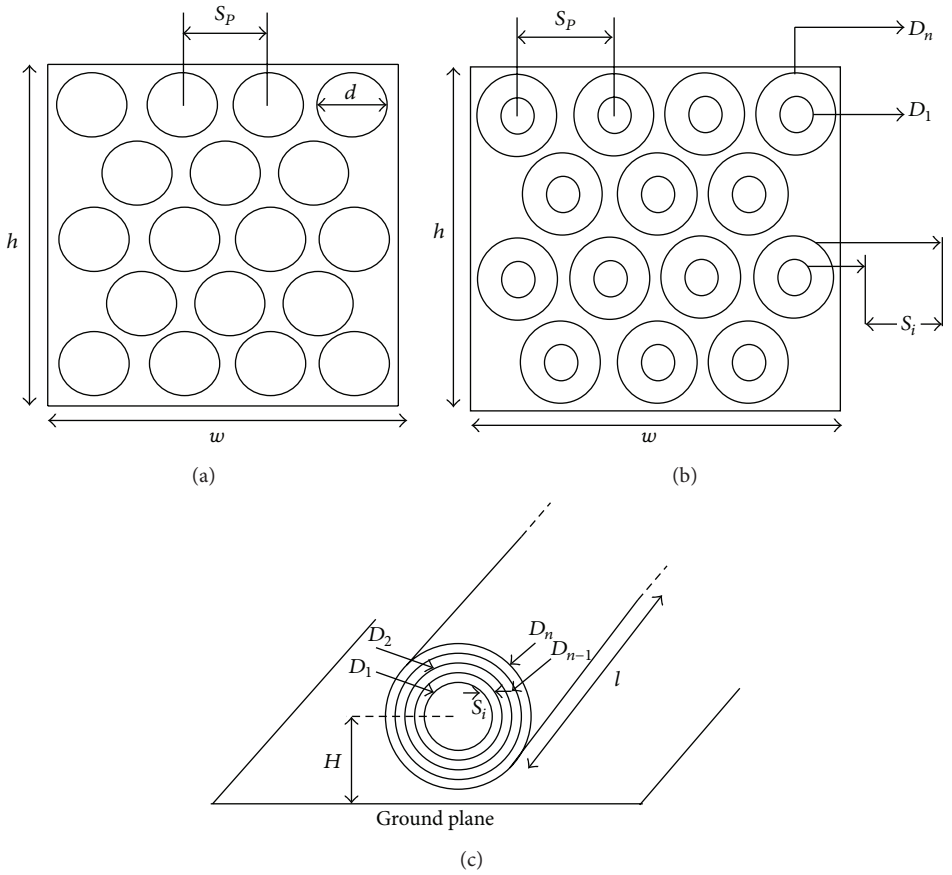

Figure 1: Geometry of (a) bundled SWCNT, (b) bundled DWCNT, and (c) single MWCNT.

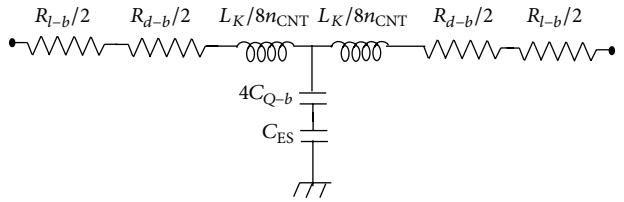

Figure 2: Equivalent *RLC* model of bundled SWCNT interconnects.

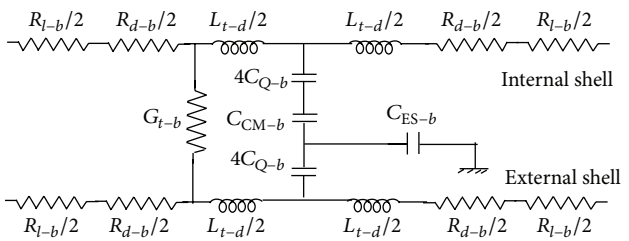

Figure 3: Equivalent *RLC* model of bundled DWCNT interconnects.

inductance (L_{t-d}) is the summation of mutual and kinetic inductance of CNTs. Magnetic or mutual inductance is measured from magnetic field of an isolated current carrying wire having some distance "h" from the ground plane, whereas kinetic inductance is mainly due to the charge carrier inertia [25, 27]. Due to the unique band structure [5], kinetic inductance of CNTs dominates over the mutual inductance. Therefore, the equivalent model of Figure 4 consists of only kinetic inductance that appears as $L_K/4$ due to four conducting channels in CNTs. The total bundle inductance (L_{t-d}) can be formulated as [25]

$$L_{t-d} = \frac{(L_M + L_K)}{n_{\mathrm{CNT}}}; \quad \text{where } L_K = \frac{h}{2e^2 v_F}, \tag{6}$$

where $v_F \approx 8 \times 10^5$ m/s is the Fermi velocity of CNT and graphene. The equivalent capacitance in CNT can be divided into (1) electrostatic capacitance (C_{ES}) that appears between the CNT and ground plane and (2) quantum capacitance (C_Q) that exists due to the finite density of states of electrons. Additionally, a coupling capacitance (C_{CM}) occurs between each shell in bundled DWCNT and single MWCNT interconnects (Figures 3 and 4). C_{CM} primarily depends on the diameter of adjacent shells and can be expressed as [14]

$$C_{\mathrm{CM}} = \frac{2\pi\varepsilon}{\ln(D_n/D_{n-1})}, \qquad C_{\mathrm{CM}-b} = C_{\mathrm{CM}} \cdot n_{\mathrm{CNT}}. \tag{7}$$

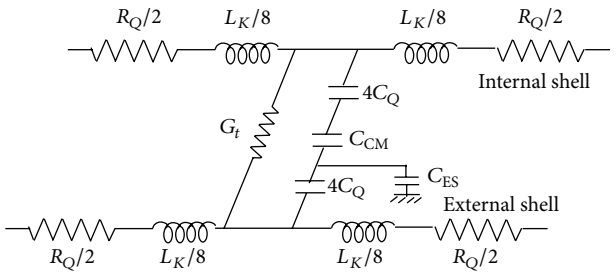

Figure 4: Equivalent *RLC* model of single MWCNT interconnects.

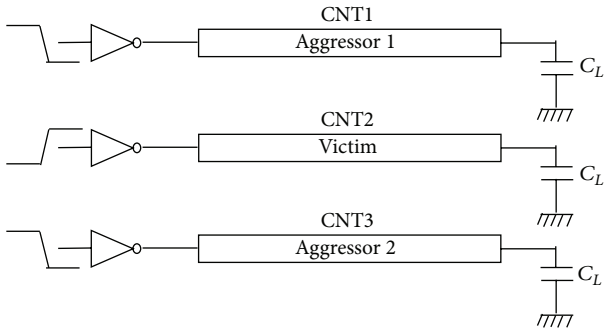

Figure 5: Three-line bus architecture made of three parallel CNTs (bundled SWCNTs/bundled DWCNTs/single MWCNTs).

3. Three-Line Bus Architecture

Propagation delay under the influence of dynamic crosstalk is analyzed for bundled SWCNT/DWCNT and single MWCNT interconnects using capacitively coupled three-line bus architecture [14] as shown in Figure 5. Out of these three lines, the middle one is referred to as victim while the other two as aggressors. Each interconnect line in bus architecture is represented using the equivalent *RLC* models of bundled SWCNT (Figure 2), bundled DWCNT (Figure 3), and single MWCNT (Figure 4). A CMOS driver with supply voltage 1 V is used to drive the interconnect line. The primary characteristics of CMOS driver is that it operates partially in linear region and partially in saturation region during switching. But a transistor can be modeled by a resistor only in the linear region. In saturation region, the transistor is more accurately modeled as a current source with parallel high resistance [19, 28].

HSPICE simulations are performed for similar transition at aggressor lines when victim line experiences an opposite signal transition. Using the model parameters suggested by ITRS 2012 [23], crosstalk delay is performed for different interconnect lengths ranging from 800 μm to 2000 μm.

4. Signal Integrity in Bus Architecture

This section analyzes the crosstalk delay (signal integrity) for bundled SWCNT/DWCNT and single MWCNT using capacitively coupled three-line bus architecture. For global interconnects, such as clock line, interconnect lengths can reach up to several millimeters. Using 22 nm, 32 nm, and 45 nm technology nodes, Figures 6, 7, and 8 demonstrate the crosstalk delay for bundled SWCNT, bundled DWCNT, and single MWCNT interconnects, respectively. It is observed that the crosstalk delays of different single and bundled CNTs are considerably reduced for lower technology nodes. The primary reason is the reduced capacitive effect that has major impact on the dynamic crosstalk delay. As technology scales down, bundle width and height are reduced

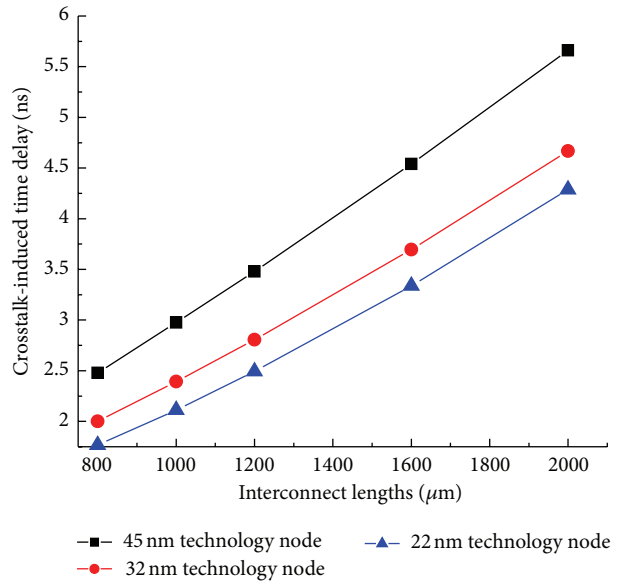

Figure 6: Crosstalk delay at different technology nodes for bundled SWCNT interconnects.

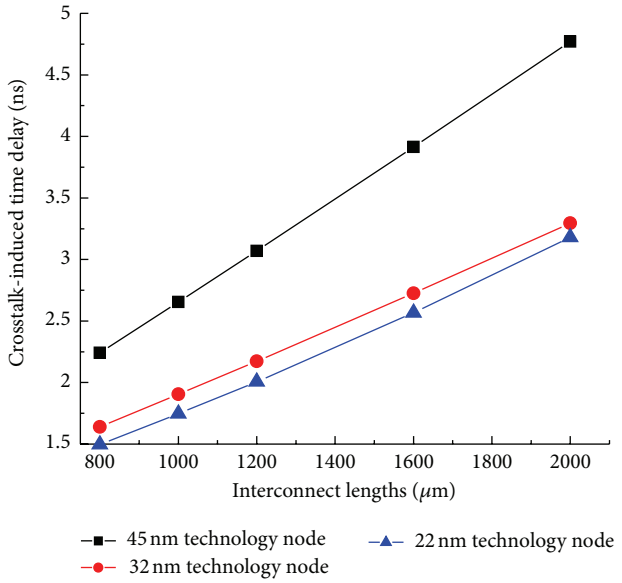

Figure 7: Crosstalk delay at different technology nodes for bundled DWCNT interconnects.

Table 1: Crosstalk delays for different CNT structures at 45 nm technology node.

Interconnect lengths (μm)	Crosstalk delay (ns) for			Percentage improvement for single MWCNT with respect to	
	Bundled SWCNT	Bundled DWCNT	Single MWCNT	Bundled SWCNT	Bundled DWCNT
800	2.4793	1.9411	1.5541	37.32	19.94
1000	2.9758	2.4539	1.8295	38.53	25.45
1200	3.4801	3.0701	2.1088	39.41	31.31
1600	4.5406	4.1137	2.6315	42.04	36.03
2000	5.6611	4.9714	3.0421	46.26	38.81

Table 2: Crosstalk delays for different CNT structures at 32 nm technology node.

Interconnect lengths (μm)	Crosstalk delay (ns) for			Percentage improvement for single MWCNT with respect to	
	Bundled SWCNT	Bundled DWCNT	Single MWCNT	Bundled SWCNT	Bundled DWCNT
800	2.0011	1.6396	1.3777	31.15	15.97
1000	2.3925	1.9046	1.5977	33.22	16.11
1200	2.8063	2.1725	1.6818	40.07	22.58
1600	3.6958	2.7259	2.0910	43.42	23.29
2000	4.6674	3.2954	2.3423	49.81	28.92

Table 3: Crosstalk delays for different CNT structures at 22 nm technology node.

Interconnect lengths (μm)	Crosstalk delay (ns) for			Percentage improvement for single MWCNT with respect to	
	Bundled SWCNT	Bundled DWCNT	Single MWCNT	Bundled SWCNT	Bundled DWCNT
800	1.7654	1.4955	1.3225	25.08	11.56
1000	2.1123	1.7474	1.5203	28.02	12.99
1200	2.4924	2.0064	1.6252	34.79	18.99
1600	3.3366	2.5674	2.0198	39.46	21.32
2000	4.2875	3.1796	2.2960	46.44	28.63

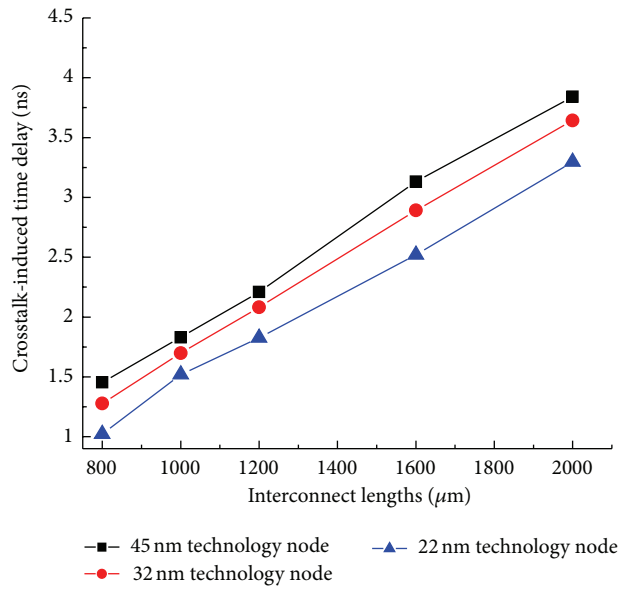

Figure 8: Crosstalk delay at different technology nodes for single MWCNT interconnects.

which results in lesser number of CNTs and shells in bundled SWCNT/DWCNT and single MWCNT, respectively. The value of capacitive parasitic primarily depends on the number of CNTs in bundle and shells in MWCNT. Thus, the crosstalk delay is effectively reduced for lesser number of SWCNTs/DWCNTs in bundle and shells in MWCNTs at global interconnect lengths as indicated in Figures 6, 7, and 8.

Tables 1, 2, and 3 summarize the crosstalk delay for different single and bundled CNTs at 45 nm, 32 nm, and 22 nm technology nodes, respectively. It is observed that the overall crosstalk delay is improved by 40.97% and 21.37% in single MWCNT as compared to bundled SWCNT and bundled DWCNT interconnects, respectively. Irrespective of technology nodes, crosstalk delay is significantly reduced for MWCNT at higher interconnect lengths. The reason behind this reduction is the lower value of capacitive parasitic, that effectively reduces for single MWCNT in comparison to bundled SWCNT/DWCNT interconnects at specified technology node. Therefore, it can be concluded that a single MWCNT is more promising than bundled SWCNT/DWCNT in current nanoscale technology.

5. Conclusion

This research paper analyzed the crosstalk delay for bundled SWCNT/DWCNT and single MWCNT interconnects by using coupled three-line bus architecture. The *RLC* models of single and bundled CNTs have been extended to address the geometry of the bus architecture and the CMOS driver is used to drive the interconnect lines. Dynamic crosstalk delay has been analyzed for worst-case scenario when the victim line is switched in opposite direction with respect to the aggressors. It has been observed that MWCNT exhibits a lower parasitic capacitance as compared to bundled SWCNT/DWCNT. Thus, the overall crosstalk delay is reduced by 40.92% and 21.37% for single MWCNT interconnects as compared to the bundled SWCNT and bundled DWCNT, respectively. Therefore, MWCNTs can be predicted as one of the most promising materials for the future global VLSI interconnects.

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