Layout Extraction and Verification Methodology for CMOS I/O Circuits*

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ABSTRACT

This paper presents a layout extraction and verification methodology which targets reliability-driven I/O design for CMOS VLSI chip, specifically to guard against electrostatic discharge (ESD) stress and latchup. We propose a new device extraction approach to identify devices commonly used in CMOS I/O circuits including MOS transistors, field transistors, diffusion and well resistors, diodes and silicon controlled rectifiers (SCRs), etc. Unlike other extractors, our extractor identifies circuit-level netlist based on the specified ESD stress condition. In addition, novel techniques are proposed for the identification of parasitic bipolar junction transistors (BJTs).

I. Introduction

I/O circuits provide protection against external hazards such as electrostatic discharge (ESD). ESD is a high current (in excess of 1 A) event [1]. On-chip I/O protection circuits often consist of parasitic devices and the layout of these devices does not conform to normal design rules. Layout extraction of I/O circuits is critically important for design validation since it provides a link between layout and circuit analysis. The hitherto emphasis of computer-aided design has been on the chip core circuitry, whereas the design and layout of I/O cells have heavily relied on design expertise and guidelines. Commercial layout extraction programs are only capable of performing limited extraction and verification of the I/O layout. The limitations of commercial extraction tools stem from the following:

- They perform device extraction based on *boolean* operations of layout masks. The tools can not extract parasitic devices such as field devices, SCRs or the parasitic BJTs which are often unintended side effects of the layout and not recognized by designers. But they may play an important role during ESD stress events.
- They only extract circuit schematics under normal operating condition, i.e. when the chip is powered up. However, the circuit is typically not powered during ESD events. An ESD event can generate stress current in excess of 1 A. The normal device models are not applicable because devices are operating in high current regimes or are biased differently from normal operating modes. Therefore, the schematic for circuit simulation must be determined according to the ESD stress condition.

The proposed extraction and verification methodology for CMOS I/O is outlined in Fig. 1. The program takes layout input in CIF or GDSII format and generates the input decks for the circuit simulator iETSIM [2]. The extraction program consists of three major parts:

- **Device Extraction**: A generic device extraction approach is employed to extract all devices used in I/O circuits.
- **Stress Annotation**: Given a specified ESD stress condition, the device bias conditions are identified and the circuit schematic is extracted. The ESD stress condition is defined by specifying an I/O pad zapped positively or negatively with respect to another pad (V_{dd}, V_{ss}, or any other I/O pad).
- **BJT Extraction**: The program extracts parasitic BJTs and detects *critical* ones. A critical BJT is defined as a BJT which is unintended byproduct of the layout. A critical BJT's turning-on can induce circuit failures.

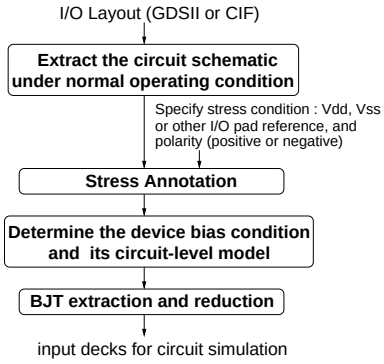

Figure 1: The extraction flow diagram.

The presentation of this paper is organized as follows. Section 2 describes the intermediate representation for the layout. Section 3 presents the device extraction and layout verification approach. Section 4 describes the circuit stress annotation and the extraction of the circuit schematic for a specified ESD stress condition. Section 5 describes the extraction of parasitic BJTs. Section 6 demonstrates the effectiveness of the methodology using industrial layout examples and presents circuit simulation results. Section 7 describes the extraction strategy for the full chip I/O frame. Finally, we present summary.

II. Intermediate Representation

The typical representation of a VLSI layout is the geometrical description of masks, such as CIF format. Additional abstractions are needed for extracting complex device structures. The

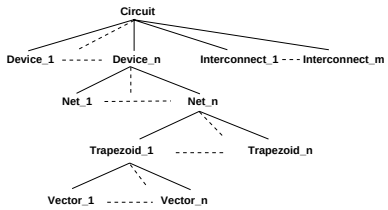

Figure 2: The hierarchical representation for a circuit.

general structure of a circuit is mapped into the hierarchical form shown in Fig. 2. A circuit contains devices and interconnect nets. A device is made up of a set of nets. A net is composed of connected trapezoids, and vectors make up trapezoids.

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The hierarchy represents the layout at different abstraction levels. Vector and trapezoid belong to geometrical domain. Net is the structural representation. Device and circuit are functional abstractions. Such a hierarchical representation is geometry-conserving. In other words, the geometrical information for any level of abstraction is retained through the hierarchical structure.

For device extraction, the mask layer data must be transformed into new layer representations. We use an edge-based scan line algorithm to perform *boolean* operations on the masks

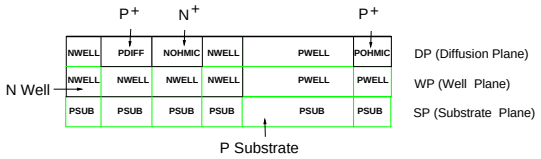

Figure 3: Substrate represented by non-overlapping trapezoids.

[3][4]. As the trapezoid representation is needed for net abstraction, vectors for a polygon are decomposed into trapezoids [4]. The silicon substrate is divided into non-overlapping trapezoids as shown in Fig. 3.

Next, connected trapezoids are grouped into nets to provide a structural abstraction for geometrical layout. The scan line algorithm extracts nets according to a *connectivity matrix* which specifies the connectivity relationships between different layers. The device is composed of nets. There are three kinds of nets, namely *substrate net, interconnect net,* and *contact net.* An interconnect net is a set of connected interconnect layer trapezoids. The substrate net is composed of adjacent substrate layer trapezoids of the same kind.

The extraction of contact nets is handled differently from interconnect nets and substrate nets, because contacts do not abut each other. Contacts which are connected to the same substrate and the same interconnect net make up one contact net. In Fig. 4, there are two substrate nets Sub1(NDIFF) and Sub2(POHMIC) and three interconnect nets Inter1, Inter2 and

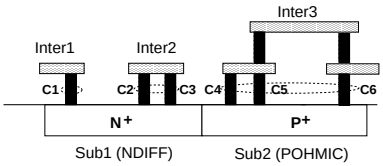

Figure 4: Extraction of contact net.

Inter3. Three contact nets, which are denoted by dashed circles, are extracted, namely CN1, CN2 and CN3. CN1 consists of C1. CN2 is composed of C2 and C3. CN3 consists of C4, C5, and C6.

III. Device Extraction and Layout Verification

A. Device Extraction

To help explain the device extraction approach, we introduce the concept of *device graph* (DG). Each device graph is used to describe one type of device. The basic structure of the device graph is defined as $DG = (N, R, s)$, where N is the set of nets in the device, R represents the set of relationships between the nets, and s is the *seed* net of the graph. The relationships in R can be categoried as below

- R1: Adjacency
- R2: Electrical connectivity
- R3: Geometrical position

The device graph proposed in this work is more general than the one introduced in [5] for analog bipolar verification. Fig. 5 depicts device graphs for PMOS transistor (the extraction of well contacts is necessary for the PMOS circuit model covering the snapback regime) and n-diffusion resistor. In graphical notation, a net is represented by a filled circle, and multiple nets by double circles. A solid line or dashed lines indicate the adjacency relationship between two nets. A contact net is connected with dashed lines when it is considered optional. The seed net is marked by an arrow. It is the location from which the DG can be constructed by the breadth-first neighbor searching.

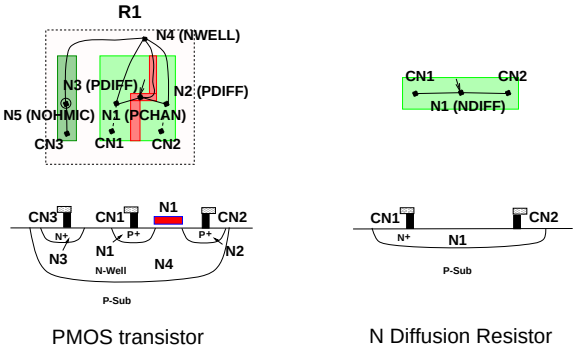

Figure 5: Device graphs for the PMOS transistor and the n-diffusion resistor.

MOS transistors and diffusion resistors can be completely specified with the adjacency relationship R1. However, specifications for R2 and R3 are necessary for identification of other types of devices. The device graph for the thick field device (TFD) is illustrated in Fig. 6. R2 specifies that nets N2 and N3 can not be at the same electrical potential, and they can not belong to one MOS transistor if they are associated with MOS transistors. In addition, either of the two interconnect nets connected to N2 or N3 must be exposed to ESD stress. R3 specifies that the distance between net N2 and N3 must be less than or equal to 2 μm. The distance is process technology dependent. The device graph for an LVSCR (low-voltage trig-

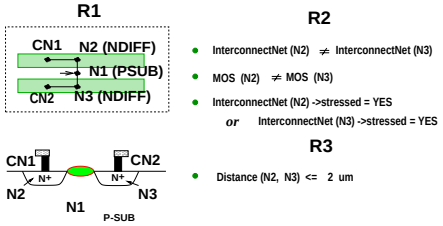

Figure 6: Device graph for the thick field device.

gered SCR) is given in Fig. 7. The LVSCR is a commonly used protection device in deep submicron CMOS technologies [6].

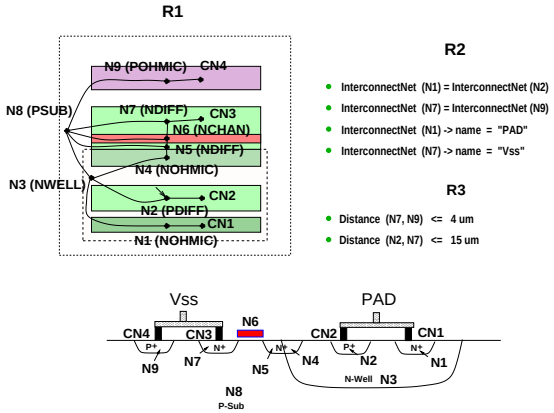

Figure 7: Device graph for the LVSCR.

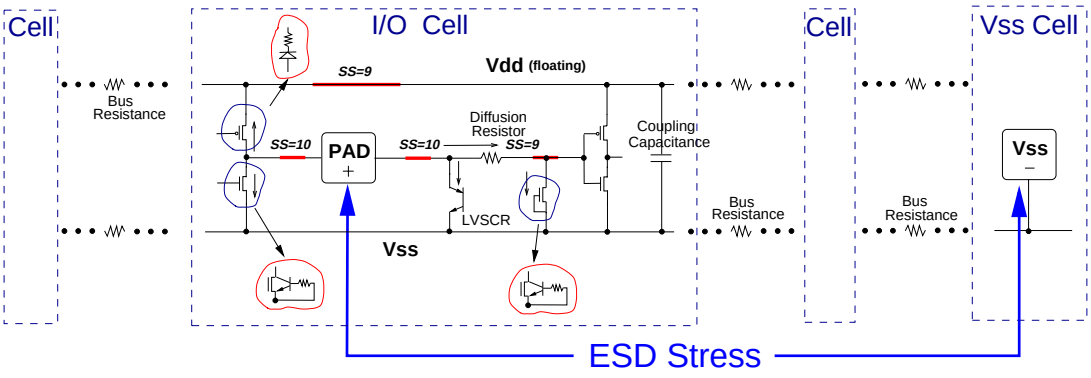

Figure 8: Stress annotation to identify the device's bias condition, and determine its circuit model.

B. Layout Verification

Normal design rules can often be described by geometrical relationships between mask layers. Since I/O layout does not conform to normal design rules, a different set of rules is often developed for I/O circuits [7]. The descriptions of I/O rules often involve specification of layout geometries associated with layout structures and electrical circuit properties. I/O layout verification using commercial tools is limited and often resort to extensive use of user-defined marking layers. This requires that circuit designers and layout engineers have in-depth understanding of protection circuits. Still, the majority of I/O design rules can only be checked by expert's visual inspection. I/O rules may not be fully verified in industrial products because of the lack of CAD tools.

With device graph, I/O design rule checking can be easily performed by searching for *error devices*. A design rule can be described by an error device graph. For instance, the error device graph for a latchup path can be defined similarly as the DG for an LVSCR. The detection of an error device will signal a design or layout error. Layout verification using device graphs can check the design rules described by both electrical and geometrical properties. Typical I/O rule examples are guard ring rules and driver contact rules (the contact-to-gate spacings for protection devices are often more than the minimum spacing) [7]. Most of the I/O rules can be checked by detecting error devices, one exception being the parasitic BJT detection. The detection of critical parasitic BJTs is very important for I/O verification. However, it requires knowledge of ESD stress conditions. Thus a different treatment is needed and will be described in section 5.

C. Cluster Extraction

Extracted I/O circuit schematics can often be simplified by clustering devices. For example, merging of multifinger MOS transistors into a single MOS transistor results in a simplified circuit topology and thus faster electrical simulation. Similarly, clustering can also be done at the circuit level. Subcircuits after clustering form a subcircuit cluster. In Fig. 9, circuit schematic of a typical output protection circuit is simplified by performing device clustering and subcircuit clustering. Clustering not only

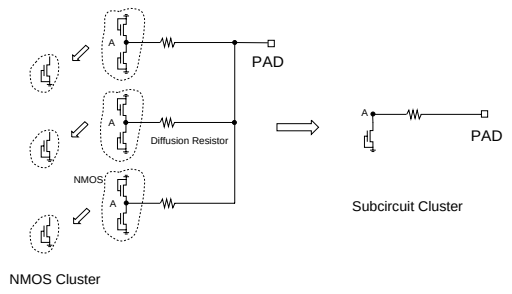

Figure 9: An example for device and subcircuit clustering. All nodes labeled A are considered at the same electrical potential.

can facilitate device reduction but also identify critical devices among peers, such as the lateral BJT reduction which will be discussed in section 5.

IV. Stress Annotation

Under ESD testing the chip is not powered up. According to the Mil Standard 883C method 3015.7 [8], a Human Body Model (HBM) test should zap all possible pin combinations of a chip for both positive and negative stresses, and the chip must pass 2KV HBM-ESD level for all stresses. When the ESD zapping is performed between two pads, all other pads are kept floating. Each I/O cell must pass the required protection level with respect to V_{dd}, V_{ss} and any other pad for both polarities.

Since the behavior of a device is bias-dependent, its circuit model should be determined according to its operating condition. We propose a static analysis technique, called *stress annotation*, to determine each device's applicable circuit model. Fig. 8 illustrates the stress annotation performed on an output circuit for a specified stress condition, i.e. positive stress on the pad with respect to V_{ss}. First, the circuit schematic for the layout at the normal operating condition is extracted. Then, the stress annotation is conducted using a breadth-first search to propagate the stress current from the stressed pad. The stress current passes through forward-biased pn junctions and semiconductor resistors. The search stops when a reverse-biased pn junction is reached. Each interconnect net in the current path is annotated with its *stress strength* (SS). The relative voltage levels between two interconnect nets can be compared by checking their stress strengths. In addition, stress annotation will help identify parasitic BJT devices, which will be discussed in the next section. Starting with an initial value, such as 10 used in Fig. 8, the stress strength is reduced by one whenever the stress current passes through a resistive device.

After the bias condition is determined from the stress annotation, each device's circuit model can be determined. When a device is under ESD current stress, a high current model must be used, such as an NMOS model which covers the snapback regime [9] and a resistor model which considers velocity saturation effect [10]. When a pn junction in a transistor is forward-biased under ESD stress, it operates as a diode. When the junction formed between the drain diffusion of the driver PMOS transistor and the n-well is forward biased, the n-well is charged up and the high current is propagated to the V_{dd} power line via the well contact. For this case, we substitute the PMOS transistor with the serial combination of a forward-biased diode and a well resistor. This is the applicable circuit model for the PMOS transistor under this specific bias condition.

V. BJT Extraction

In CMOS technologies, all devices are laid out in a single substrate and affected by substrate currents. During an ESD event, the currents injected into the silicon substrate can propagate far from the source and be collected. The substrate coupling effects can be modeled by parasitic BJTs and substrate resistance networks.

A. Lateral BJT Extraction

Ideally, the ESD current should be conducted through intentionally designed protection devices such as TFDs, LVSCRs or NMOS transistors. However, parasitic BJTs often come into

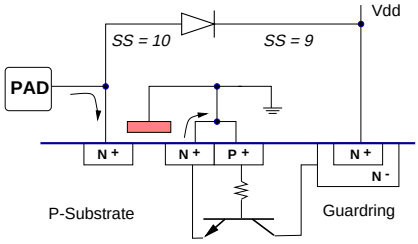

Figure 10: Extraction of lateral parasitic BJTs. The source of NMOS transistor (emitter) and guard ring (collector) form a parasitic BJT.

being as the side effects of the layout or design. The turn-on of lateral BJTs has been a common cause of chip ESD failures [1][12][15]. The extraction of parasitic BJTs requires knowledge of electrical relationships. Without electrical relationships, any two diffusions or wells can potentially form a BJT. The total possibilities for BJTs to occur can be $2\binom{n}{2}$, where n is total number of diffusions or wells within a single cell, $\binom{n}{2}$ denotes the possible number of pairs and the constant 2 accounts for both polarities (emitter and collector). However, with the known device bias conditions and interconnect potentials from the stress annotation, the number of possible BJTs can be much less. An example of parasitic BJT identification is shown in Fig. 10. Once the stress annotation has been performed, the forward-biased pn junctions are identified as possible emitters of BJTs. Those diffusions or wells which are stressed with high voltages are identified as possible collectors (checking the lower voltages for the extraction of lateral PNPs). Note that different BJTs will be extracted for different stress conditions. If there are p emitters and q collectors, the number of possible BJTs is pq. However, not all of them will conduct significant currents. Further reduction is needed to detect active BJTs among them. The gain, β, of the parasitic BJT is the most important parameter in the BJT models, such as the Gummel-Poon model. Hence, it is used as a criterion for reduction. β is inversely proportional to the square of the base width W. The set of reduction rules is listed below while the referenced configurations are illustrated in Fig. 11.

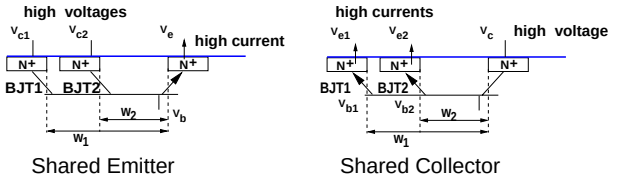

Figure 11: Configurations of parasitic BJTs for reduction.

1. Shared emitter rule:
   (a) If $V_{c1} \leq V_{c2}$, and $\beta_1 < \beta_2$, remove BJT1.
   (b) If $V_{c1} < V_{c2}$, and $\beta_1 \leq \beta_2$, remove BJT1.
   (c) Otherwise, no reduction.
2. Shared collector rule:
   (a) If $V_{e1} \geq V_{e2}$, and $\beta_1 < \beta_2$, remove BJT1.
   (b) If $V_{e1} > V_{e2}$, and $\beta_1 \leq \beta_2$, remove BJT1.
   (c) Otherwise, no reduction.
3. Minimum β rule (technology dependent):
   (a) If $\beta < \beta_{threshold}$ ($W > W_{threshold}$), no BJT.

Note that the reduction rules consider V_{cb}. To the first order, the collector current is independent of the value V_c. In the shared emitter configuration, there exist two current paths, from C2 to C1 then to the shared emitter, or from C2 to the emitter. $V_{c1} < V_{c2}$ and $\beta_1 \leq \beta_2$ indicates that the path from C2 to the emitter is less resistive, so that the current is shunted through C_2. The minimum β rule is technology dependent.

B. Vertical BJT Extraction

Vertical BJTs can also impact the ESD circuit performance. Current injected by vertical BJTs into the substrate will raise the substrate potential and may change the substrate bias conditions of all other devices. When a diffusion in a well is forward-biased, a vertical BJT will be extracted under either of the two situations, i.e. the diffusion is at high potential while the substrate is grounded, or the diffusion is grounded while the substrate is under the negative stress. The diode in Fig. 8 is replaced by the vertical BJT Q1 as shown in Fig. 12. The lateral BJT Q2 formed by the drain and source of the PMOS

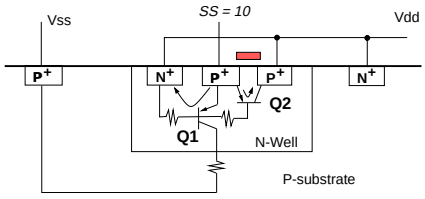

Figure 12: BJTs formed by the PMOS transistor in Fig. 8.

transistor is extracted according to the lateral BJT extraction method. There are two current paths from PMOS drain diffusion to V_{dd}, i.e. through Q1 and Q2. When the well resistance is high, Q2 conducts a significant amount of current [11]. If the size of PMOS transistor is small and can not sustain the high current, circuit failure will occur.

VI. Walk-Through Examples

In this section, three industrial layout examples from the literature are used to illustrate the proposed extraction methodology.

A. An Input Protection Circuit

A typical input protection circuit consists of two stages, namely, the primary protection and the secondary protection. The secondary protection is provided by gate-grounded NMOS (GGNMOS) transistors to protect the gate oxide of the input transistor. The circuit uses a TFD as the primary protection and a diffusion resistor as the isolation resistor. Two different layouts for the input protection circuit are given in Fig. 13 and 14. Although both layouts have the same circuit schematic under

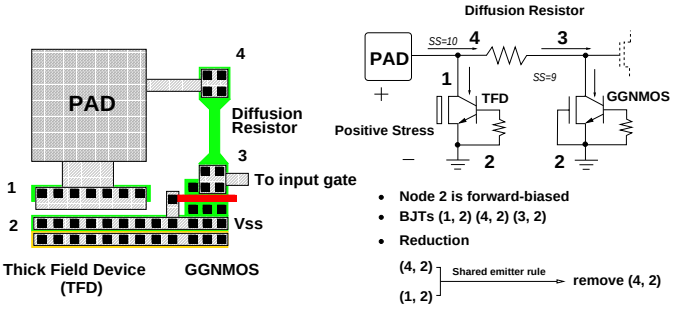

Figure 13: Analysis of layout 1.

the normal operating conditions, it has been found experimentally that there exists a lateral parasitic BJT in layout 2 under the positive stress condition from the pad w.r.t. V_{ss} [12][13]. The nodes in the device graphs are numbered in the layout. A lateral BJT is denoted by the node numbers of its collector

and emitter. For example, (1, 2) represents the BJT formed by node 1 as its collector and node 2 as its emitter.

First, the stress annotation is conducted on the circuit schematic. Since the drains of TFD and GGNMOS are under positive stress, the high current models including the bipolar action must be used. Next, the BJTs are extracted for the two layouts as explained below.

- Layout 1: As shown in Fig. 13, diffusion 2 is forward-biased after the TFD or GGNMOS is triggered, while diffusions 1, 3 and 4 are under high voltage stress. Therefore, three lateral BJTs may be formed. They are denoted as (1, 2) (3, 2) and (4, 2). To perform the BJT reduction, BJTs (4, 2) and (1, 2) are clustered to form the shared emitter configuration. BJT (4, 2) is eliminated according to the shared emitter rule. Since BJTs (3, 2) and (1, 2) have already been included in the TFD and NMOS high current models, **no extra parasitic BJT exists in layout 1**.

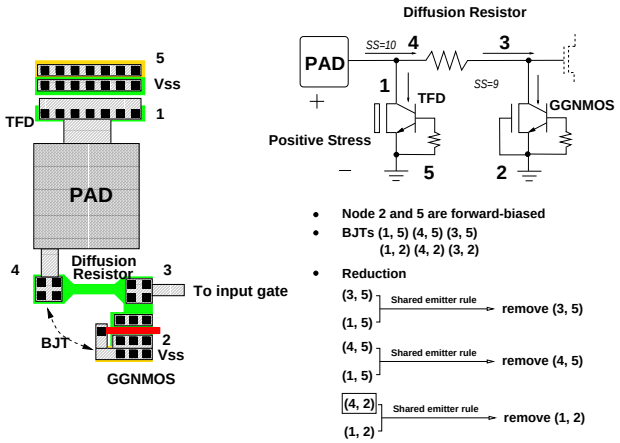

Figure 14: Analysis of layout 2. Lateral BJT (4, 2) is detected under the positive stress to pad w.r.t. V_{ss}.

- Layout 2: As illustrated in Fig. 14, diffusions 2 and 5 are forward-biased. They become the sources for minority carrier injection into the substrate. Since diffusions 1, 3 and 4 are stressed with high voltages, there are six possible lateral BJTs, namely (1, 5) (4, 5), (3, 5), (1, 2), (4, 2) and (3, 2). The BJTs are reduced similar to layout 1. Because the TFD and NMOS high current models include BJTs (1, 5) and (3, 2), **parasitic BJT (4, 2) is detected in layout 2**.

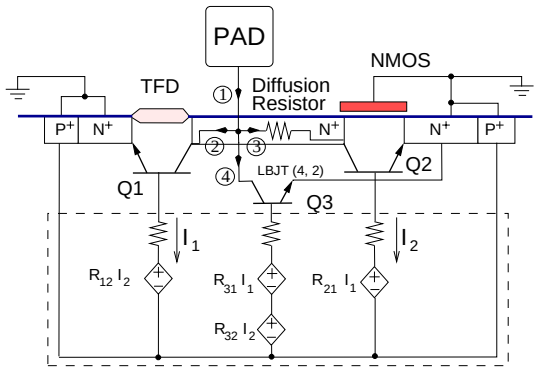

Figure 15: The circuit schematic with the substrate resistance network under positive stress.

The circuit schematic for layout 2 is drawn in Fig. 15 along with the cross-section of silicon substrate. The substrate resistance network model has been developed in [14]. Circuit simulation results in Fig. 16 indicate that there is indeed a significant amount of stress current conducting through the lateral

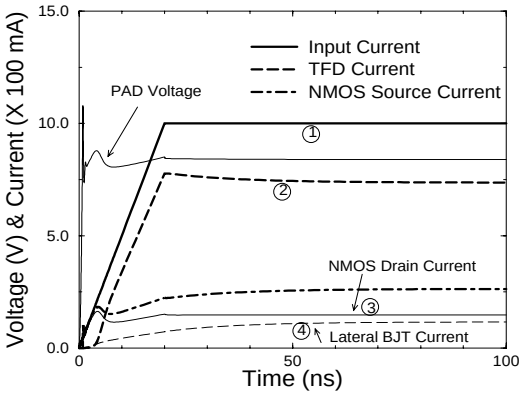

Figure 16: Simulation results under a ramped current input. Most of the stress current flows through the TFD. Part of the source current is collected at the junction connected to pad through the lateral BJT (4, 2).

parasitic BJT. This confirms the experimental and failure analysis results reported in [12][13].

B. An Input Protection Circuit – II

The circuit layout and details of extraction are shown in Fig. 17. It uses an LVSCR instead of a TFD as the primary protection device. Although the circuit schematic is same as the one in the previous example, the circuit failure mechanism is different. The failure site is circled in the layout when the pad is stressed negatively with respect to V_{dd} [15]. It indicates that a parasitic BJT (5, 2) turns on and collector failure occurs.

The negative current is propagated from the pad to perform the stress annotation. The GGNMOS is now stressed negatively so that the drain becomes the emitter of its associated BJT. Under negative stress conditions, the diffusion resistor to substrate junction is forward-biased and injects minority carriers into the substrate. We divide the diffusion resistor into three segments. The n-well denoted by node 5 is at high potential. Therefore, there may exist six BJTs (5, 4) (5, 3) (5, 2) (5, 1) (7, 4) (6, 1). After the reduction process, BJT (5, 2) is finally detected. The circuit simulation can be performed similarly as for example 1.

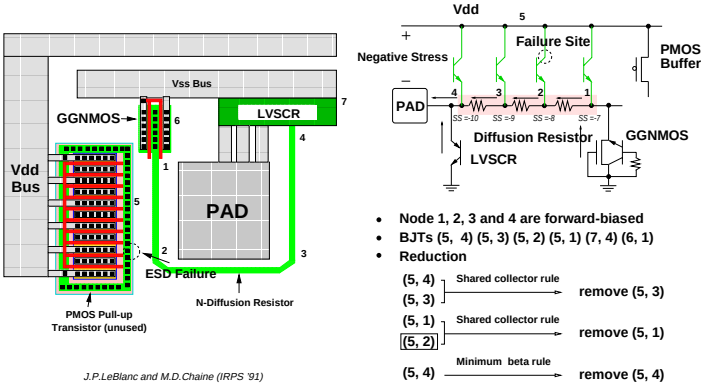

Figure 17: Analysis of the input protection circuit – II.

C. An I/O Protection Circuit

The last example illustrates the extraction of vertical BJTs and its role for accurate simulation. The circuit is composed of a gate-coupled NMOS device (consists of NMOS transistors, an NMOS capacitor and a well resistor) and a lateral diode

Circuit Layout	Stress [1] Condition	No. of Lateral BJTs				No. of Vertical BJTs		
		(-, -, -)	(c, -, -)	(c, a, -)	(c, a, r) [2]	(-, -, -)	(c, -, -)	(c, a, -)
Ex1 (layout 1)	V_{ss} (+)	12	12	3	**0**	0	0	**0**
Ex1 (layout 2)	V_{ss} (+)	20	20	6	**1**	0	0	**0**
Ex2	V_{dd} (−)	42	30	6	**1**	6	1	**0**
Ex3	V_{ss} (+)	210	42	3	**0**	4	1	**1**

(c, a, r) stands for (clustering, annotation, reduction). A dash denotes that the corresponding operation is not performed.
[1] The stress is from pad to the reference node.
[2] The number of critical parasitic BJTs. The intentionally designed BJTs are excluded.

Table 1: Summary of the BJT extraction results.

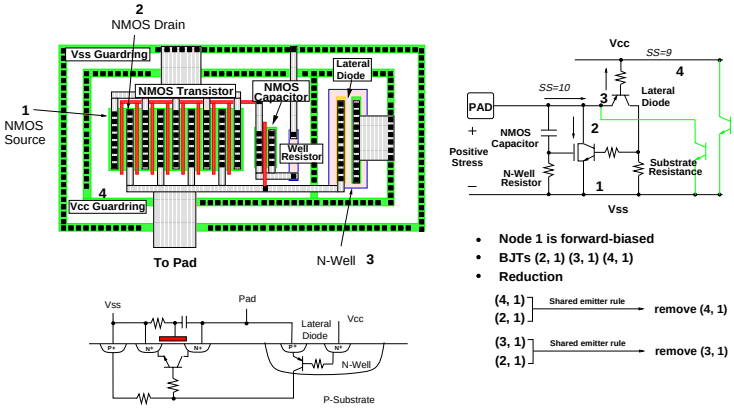

Figure 18: Analysis of the I/O protection circuit. Lateral BJT (2, 1) is included in NMOS snapback model. Therefore, no parasitic lateral BJT is detected.

connected to V_{cc} [16]. The circuit schematic is extracted for the positive stress from pad with respect to V_{ss}. After we have performed the stress annotation, we proceed to extract lateral BJTs and perform reduction as shown in Fig. 18. Finally, we extract the vertical BJTs. As the pn junction in the lateral diode is forward-biased and resides in the n-well, the diode is replaced by a vertical BJT to consider the substrate coupling effect. The work on substrate coupled simulation using iETSIM was published in [16].

The extraction results for the above three examples are summarized in Table 1. The BJT extraction procedure involves three major operations, namely device clustering, stress annotation and BJT reduction. As we can see, each step can greatly reduce the number of BJTs, and eventually the procedure pinpoints to the critical ones which are printed in bold. By using the proposed systematic procedure, we can automatically extract the I/O circuits for full ESD analysis.

VII. Full Chip Frame Extraction

The ESD standard requires the protection level to be verified for the full chip. This is due to the fact that reliable individual I/O cells do not guarantee the full chip reliability [1]. Therefore, verification using simulation must also be performed at the I/O frame level. The program employs a hierarchical approach for the extraction of the chip I/O frame. First, each I/O cell is extracted once and its intermediate representation shown in Fig. 2 is stored in an object-oriented database. The extraction of the full chip I/O frame only utilizes the interconnect relationships among I/O cells. It identifies the bus architecture (single bus or separate internal and external buses, the power bus protection structure) and extracts bus resistances and power bus coupling capacitances shown in Fig. 8. Then, stress annotation is performed on the extracted I/O frame circuit. The extraction of possible parasitic BJT devices must be done for every two adjacent cells.

VIII. Summary

We have presented a novel extraction and verification methodology for CMOS I/O cell and chip frame. To our knowledge, the layout extractor presented in this paper is the first comprehensive layout extractor developed for reliability-driven CMOS I/O design. With short turn-around time, extensive ESD protection circuit simulations can be performed by using our extractor and simulator. Thus the design and layout flaws such as the existence of a critical parasitic BJT can be detected before the design and layout are committed to silicon.

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