Josephson tunneling devices—A new technology with potential for high-performance computers

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INTRODUCTION

Superconducting thin film devices which exploit the Josephson effect and Giaever type tunneling have been observed to switch very fast while dissipating extremely little power. They show, therefore, good promise for high-performance computer circuits since the low power dissipation permits dense packaging with attendant short intercircuit signal delays, a prerequisite for effective utilization of fast switching circuits.

The devices are based on two discoveries of the early 60's. B. Josephson[1] predicted in 1962 that supercurrent can flow through nonsuperconducting and even insulating layers without causing voltage drops if these layers are thin enough. I. Giaever[2] discovered in 1960 that the tunnel characteristics of metal-oxide-metal sandwiches changes markedly when the metal electrodes become superconducting.

The possibility of building superconductive computers has been of interest ever since D. Buck[3] reported in 1956 on the operation of his "cryotron" switching device and demonstrated that this device is capable of performing logic and memory functions.

Efforts in several laboratories over the years to bring the cryotron technology to fruition have, however, met with failure. The main reason for the lack of success was that semiconductor technology has proved itself to be not only competitive but superior in switching speed and adaptability to large scale integration, facts which made it illogical to try to overcome technological problems of the cryotron technology which were unsolved at the time.

The basic difference between cryotron and Josephson tunneling circuits is that the latter have been shown to be orders of magnitude faster in switching operations than the former. In fact, it appears to date that Josephson tunneling devices have good potential to surpass semiconductor circuitry with respect to switching speed and system performance since packaging limitations due to heat removal problems already encountered in advanced semiconductor circuit networks are expected to be absent in Josephson tunneling circuit networks.

The basic effects underlying this technology are sketched in the next section before specific and preferred structures of switching gates, and their characteristics are discussed in the third section, and configurations and operations of memory and logic circuits in the fourth section. A review of presently known technological aspects is given in the fifth section followed by a brief summary in the final section.

SUPERCONDUCTIVITY, TUNNELING AND JOSEPHSON EFFECT

Superconductors are well-known to exhibit specific properties when they are cooled below a critical temperature T_c. Their electrical resistance drops to zero, and they behave like diamagnetic bodies, expelling magnetic fields. If they are arranged in closed loops, they can trap magnetic flux and sustain circulating persistent electrical current indefinitely.

These properties can be understood by postulating that superconductors comprise two interpenetrating electron fluids, a normal fluid of density n_n and a superfluid of density n_s. The normal fluid consists of single conduction electrons and the superfluid is made up of bound electron (Cooper) pairs which are the product of a condensation process taking place below the critical temperature and involving single conduction electrons with equal and opposite momentum and spin. The participating electrons occupy energy levels just below and above the Fermi level of the metals. The depletion

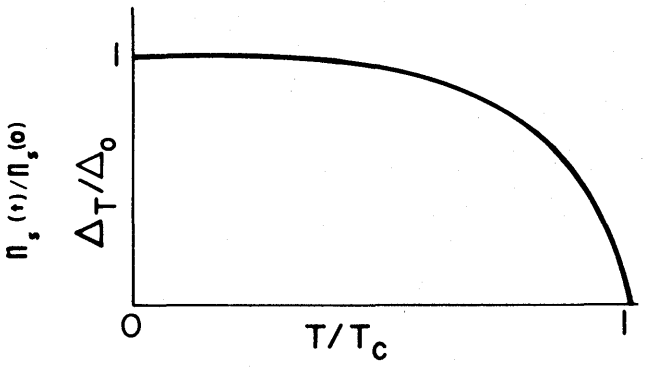

Figure 1—Normalized diagram of a superconducting energy gap Δ_T and superfluid $n_s(t)$ dependence on temperature T. Δ_o and $n_s(o)$ denote values at $T = 0$.[13]

of these levels leads to the development of a forbidden energy band, the so-called superconducting energy gap 2Δ (on the order of meV) around the Fermi level.

The Cooper pair system occupies a single energy state which lies below the Fermi energy by an amount of energy Δ (per electron) corresponding to the binding energy of the Cooper pairs in accordance with the classic (BCS) theory of superconductivity[4] by Bardeen, Schriefer and Cooper. The Cooper pair system is highly correlated throughout the superconducting region which is commonly expressed as the long range order of the superconducting state. The system can be described in quantum mechanical terms by a wavefunction $\psi(r)$, the phases $\phi(r)$ of which are related throughout the entire superconductor.

The Cooper pair system density n_s and the energy gap Δ are related to each other and depend on temperature as is shown in Figure 1. n_s and Δ are zero for $T > T_c$, rise first rapidly, then much more slowly with decreasing temperature until Δ is full developed and only the superfluid n_s exists at $T = 0°K$.

The second effect to be reviewed is electron tunneling. It is well-known that electric currents can be transported through a metal-insulator-metal sandwich with an attendant voltage drop across the thin insulator by means of the tunneling process. This process is readily understood as a consequence of the quantum mechanical concept of assigning to electrons in metals wavefunctions of the form $e^{i\mathbf{k}\cdot\mathbf{r}}$ with $\mathbf{r}$ being a space variable and $\mathbf{k}$ being the wave vector. For $\mathbf{k}$ imaginary—which is the case outside of the metal surface—the wavefunction decays exponentially. Since the square of the amplitude of the wavefunction at any point in space is interpreted as the probability of finding an electron at that point, it becomes apparent that electrons can be found with finite probability outside of a metal surface. These electrons can be captured by a second metal with available allowed energy states if the second metal is placed close enough to the first metal surface. The distance between the metals is not to exceed about 50 Å since the probability of finding electrons decreases rapidly with distance from the metal surface and the tunnel currents become extremely small.

Holm[5] has calculated the electron flux based on a simple one-dimensional model, from which the tunnel resistance R_{NN} of a tunnel junction can be deduced for $V \ll \phi_w$ as:

$$\frac{1}{AR_{NN}} = \frac{e^2}{h^2 d}(2m\phi_w)^{1/2} \exp - \frac{4\pi t}{h}(2m\phi_w)^{1/2} \quad (1)$$

with t and ϕ_w denoting the potential barrier thickness and height, respectively, A the junction area, e and m the electronic charge and mass, respectively and h Plank's constant.

Expression (1) indicates the exponential dependence of the tunnel resistance on the potential barrier height $\phi_w^{1/2}$ and thickness t and also that the voltage-current relation is linear.

The latter characteristic was shown by I. Giaever[6] to change when the electrodes become superconducting. He found that for voltages $V < 2\Delta/e$ the tunnel current is suppressed, rises rapidly at $V = 2\Delta/e$, and approaches the linear R_{NN} asymptotically for $V \gg 2\Delta/e$.

The discovery of this effect represents a direct confirmation of the existence of the superconductive energy gap as postulated in the BCS theory and it has served as a valuable tool to probe into the electronic structure of superconductors. As an example, Figure 2 shows

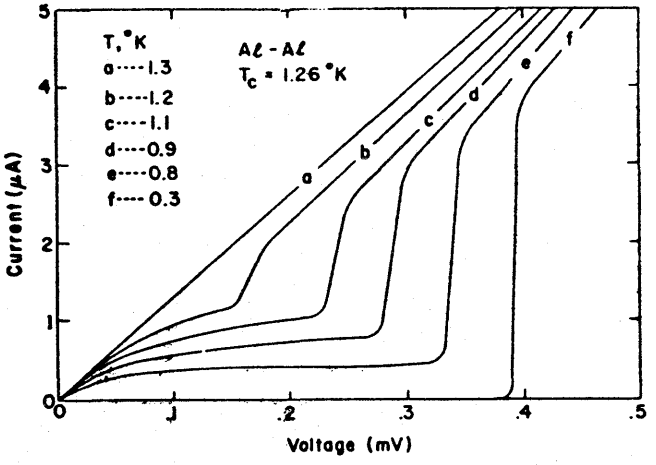

Figure 2—Current-voltage diagram of superconducting tunneling (with parameter a to f referring to decreasing temperature T).[22]

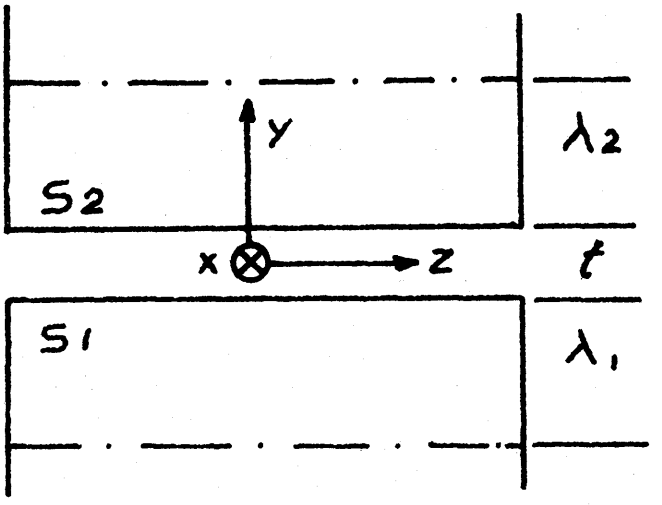

Figure 3—Geometry of superconductor-insulator-superconductor structure

by way of tunnel characteristics how the energy gap develops with decreasing temperature.

The third effect to be reviewed is the Josephson effect[7] itself. It is a property of the Cooper pair system and manifests itself in regions where superconductivity is weak, i.e., where the Cooper pair density is (locally) low. Figure 3 shows two superconductors S_1 and S_2 separated by a distance t and denotes a coordinate system in compliance with Equations 2, 3 and 4.

The Josephson effect[7] is contained in Equations 2, 3 and 4.

$$j(z, t) = j_1 \sin \phi \tag{2}$$

$$\frac{d\phi}{dt} = \frac{2e}{\hbar} V \tag{3}$$

$$\frac{d\phi}{dz} = \frac{2ed}{\hbar c^2} H_x \tag{4}$$

with $\phi = \phi_1 - \phi_2$; $V = V_1 - V_2$; and $d = \lambda_1 + \lambda_2 + t$ and $\hbar = h/2\pi$. ϕ_1 and ϕ_2 denote the phases of the wave-function $\psi(r)$ in S_1 and S_2 respectively; V_1 and V_2 the electrical potential of S_1 and S_2 respectively and λ_1 and λ_2 the London penetration depths of S_1 and S_2, respectively. e, h and c denote the electronic charge, Plank's constant and the speed of light, respectively.

Equation (2) states that a *dc* Josephson current $j(z, t) \leq j_1$ can flow between S_1 and S_2 for $\phi = \text{const}$ which according to Equation (3) indicates that the voltage between S_1 and S_2 is zero. Equation (3) indicates, on the other hand, that ϕ changes in time if a constant voltage V is impressed between S_1 and S_2 which, in conjunction with Equation (2) states that application of a voltage between S_1 and S_2 generates an ac Josephson current with a frequency which is proportional to the applied dc voltage. Equations (4) and (2) indicate that $j(z)$ is modulated in amplitude and even in direction along the z-coordinate in the presence of static magnetic fields penetrating the weak superconducting region. This leads to nonuniform internal current distributions which reduce the external current carrying capability of the weak superconducting region thus permitting one to control the (external) dc Josephson current threshold by applying magnetic fields. The experimental demonstration of the magnetic field dependence of the dc Josephson current threshold confirmed conclusively the existence of the Josephson effect.[23]

The Josephson effect has been observed in a variety of configurations such as superconductor-normal metal-superconductor sandwiches, point contacts, micron size constrictions in thin films, whiskers, even wires pressed together to form point contacts. The most suitable configuration for computer switching circuits appears, however, to be the Josephson tunneling gate which is described in the next section. An excellent and exhaustive discussion of Josephson devices is given by Matisoo.[8]

JOSEPHSON TUNNELING GATES

Figure 4 depicts schematically a Josephson tunneling switching gate. Two superconducting thin films S_1 and S_2 are shown partially overlapping and separated from each other by an insulating layer of 10 Å to 30 Å thickness, preferably an oxide grown on the bottom film S_1. They are overlaid by a third superconducting film insulated from S_1 and S_2 and patterned as a control line C. The entire structure is deposited on top of a superconducting and insulated ground plane in order to minimize circuit inductances.

The tunnel junction length and width are denoted by L and W, respectively, the oxide thickness by t, the London penetration depths in S_1 and S_2 by λ_1 and λ_2, respectively. The tunnel resistance R_{NN} of this configuration could be calculated from Equation (1) if t and ϕ_w were known, it can also be measured quite accurately at $T < T_c$ at a voltage V (with $2\Delta/e < V \ll \phi_w/e$). (Measurements at $T < T_c$ are necessary to eliminate dominating effects of the electrode resistances.)

Once R_{NN} is known, the Josephson current density j_1 can be calculated from:

$$j_1 = K(\pi\Delta/2eR_{NN}.L.W) \tanh (\Delta/2kT) \tag{5}$$

with the Boltzman constant k, a correction factor K to include strong coupling effects[9] (e.g., $K = 0.91$ for tin

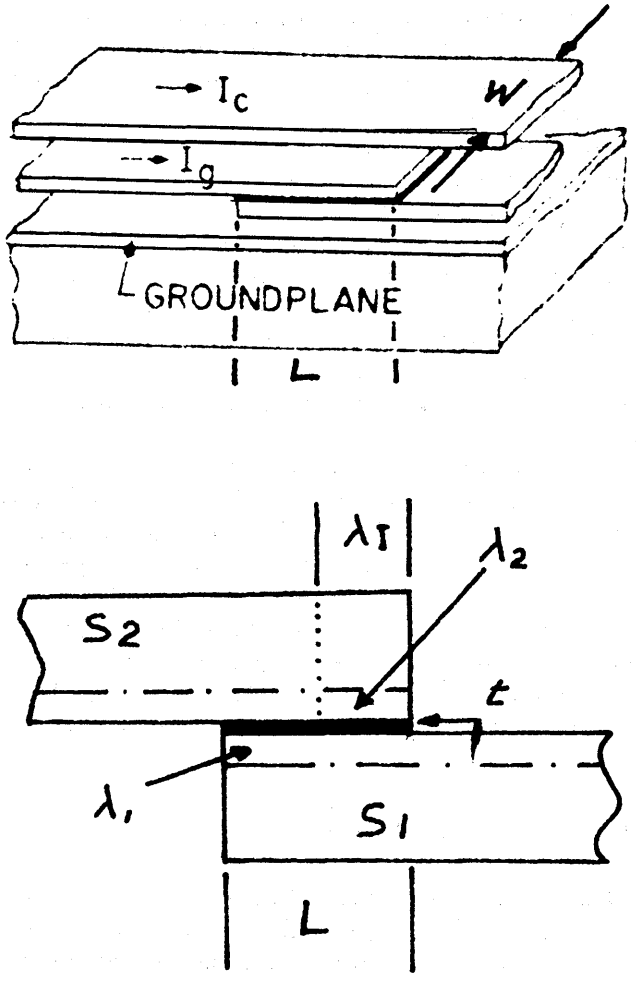

Figure 4—Josephson tunneling in-line gate configuration.[13]

and $K=0.788$ for lead) and the other quantities as defined before. The temperature dependence of j_1 is mainly determined by $\Delta(T)$; thus the functional relationship of $\Delta(T)$ shown in Figure 2 holds to a very good approximation also for the Josephson current density j_1.

An important parameter for the control of Josephson current thresholds which is well defined in Josephson tunneling junctions is the Josephson penetration depth:

$$\lambda_J = (hc^2/8\pi e d j_1)^{1/2} \tag{6}$$

with $d=t+\lambda_1+\lambda_2$, the junction "thickness" into which magnetic fields can penetrate, and all other quantities as defined before. The Josephson penetration depth λ_J denotes the distance, from the junction edges in which Josephson currents actually flow (as a consequence of Meissner effect) as shown in Figure 4.

Since $\lambda_J \propto j_1^{-1/2}$ and $j_1 \propto e^{-t}$, it is obvious that desirable current distributions can be readily obtained for a wide range of junction lengths L by simply changing the oxide thickness t.

The magnetic field dependence of the dc Josephson threshold current is strongly influenced by the current distribution in the junction.

Let us first consider the case of $\lambda_J \gg L$. Integration of Equation (4) with appropriate boundary conditions results in the expression:

$$I_{\max} = j_1 W \cdot L \frac{\sin \pi\Phi/\Phi_0}{\pi\Phi/\Phi_0} \cdot \sin\phi \tag{7}$$

with $\Phi_0 = hc/2e$, the superconducting flux quantum ($2.07 \cdot 10^{-15}$ V sec) and $\Phi = \mu s H \cdot L \cdot d$ the total magnetic flux penetrating the entire junction cross section for applied magnetic fields H. The dependence of $I_{\max}$ on Φ/Φ_0 is shown in Figure 5. The agreement between theory and experiment is excellent.

For junctions with nonuniform current distribution ($\lambda_j \simeq L$) the magnetic field dependence of the threshold current does not obey Equation (7); a full discussion of this fact is beyond the scope of this paper. The resultant dependence of the gate current threshold on the control current for a junction with $\lambda_j \sim (1/10)L$ is shown in Figure 6, displaying again the excellent agreement of the theoretical values (solid lines) and experimental data (dots). It should be noted that the slope of the line $c-a$ approaches unity for $\lambda_J/L \to 0$ while the slope of the line $c-d$ approaches infinity. The asymmetry with respect to the $I_{\max}$ axis is introduced in the so-called in-line configuration by the ground plane, which causes the magnetic fields of gate current and control current

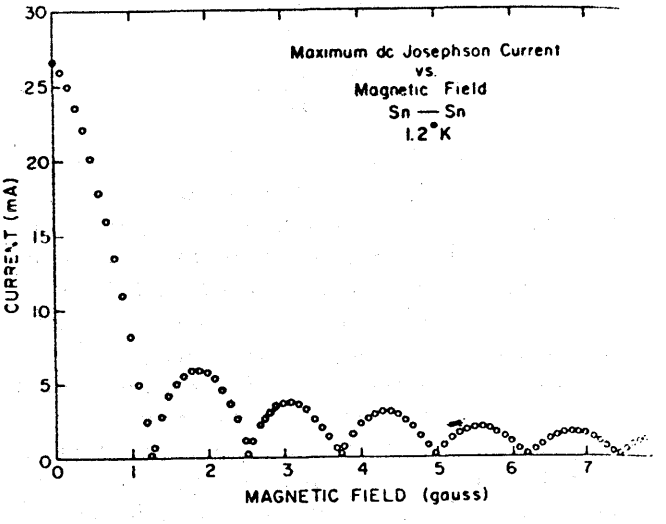

Figure 5—Normalized diagram of Josephson threshold current versus magnetic flux for junction with $\lambda_J \gg L$.[22]

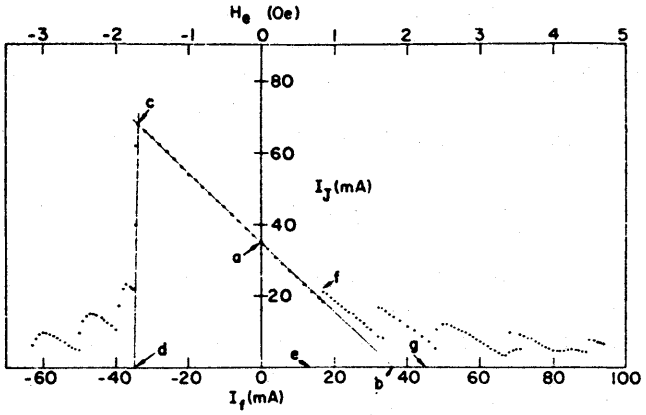

Figure 6—Diagram of Josephson gate current I_j versus control current I_F with $\lambda_J \ll L$.[8]

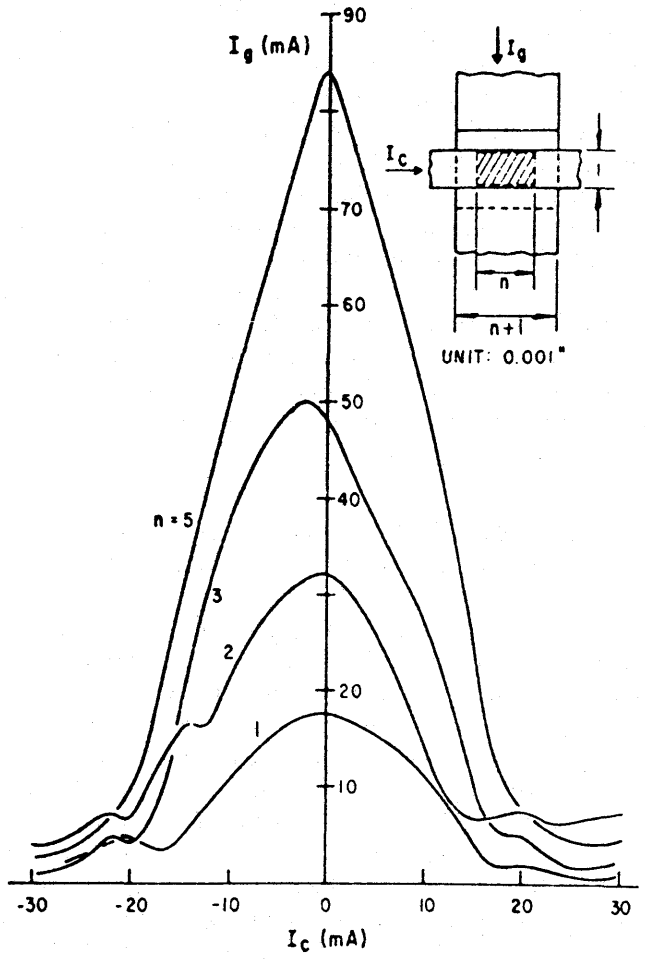

Figure 7—Diagram of Josephson gate current I_g versus control current I_c for window type crosscontrol gate configuration as shown on upper right (n denotes the ratio of gate line width to control line width). [10]

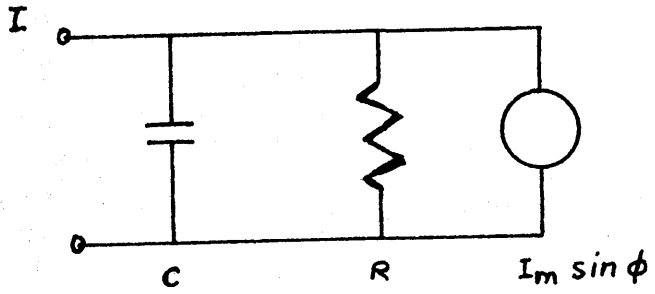

Figure 8—Equivalent circuit of Josephson tunneling junction, driven by current I

to add if currents flow in parallel and to subtract if currents flow antiparallel.

Symmetry with respect to the I_{max} axis can be restored by arranging the control line perpendicular to the gate lines in the so-called cross-controlled gate configuration. The I_{max} vs I_c characteristic of a window type version of this gate configuration as reported in Reference 10 is shown in Figure 7. The straight lines in Figure 7 indicate again a fairly nonuniform current distribution. It should be noted that this configuration permits one to raise the slope of the I_g vs I_c lines above unity by increasing the ratio $n = W_1/W_2$ which is frequently useful for gain considerations.

The dynamic behavior of Josephson tunneling gates

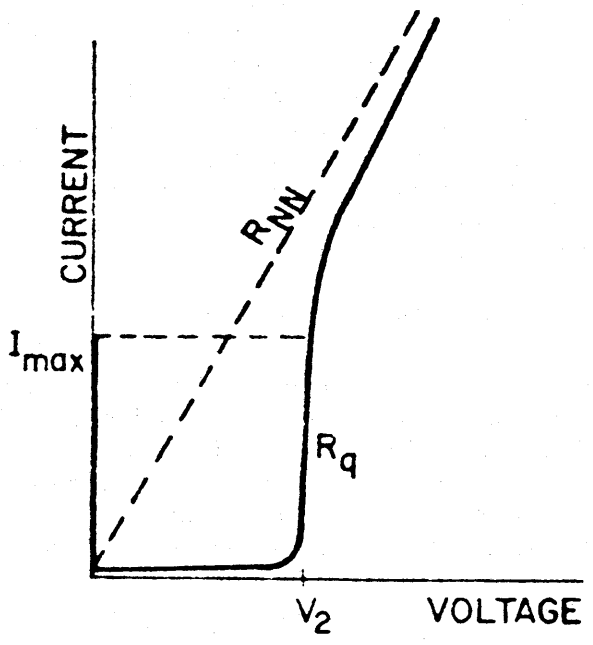

Figure 9—Current-voltage diagram of tunnel junction exhibiting Josephson and Giaever tunneling effects.[13]

is comprised of two aspects. One is the occurrence of hysteresis in the voltage-current curve, the other the dynamics during switching from $V=0$ to $V=2\Delta/e$ and back to $V=0$. Both effects are explained by resorting to the equivalent circuit of a Josephson tunneling junction[11] as shown in Figure 8. Two overlying metal films separated by a very thin dielectric layer evidently form a capacitance C, the tunnel resistance is expressed as a nonlinear resistance R (Giaever tunneling) and the Josephson effect is represented by a nonlinear Josephson current source ($I_{\min}\sin\phi$) with I_m being the maximum Josephson current through the junction. The differential equation of the equivalent circuit of Figure 8 in conjunction with Equation (3) produces the nonlinear equation:

$$C\frac{dv}{dt}+\frac{1}{R}V+I_{\min}\sin\phi=I \qquad (8)$$

Equation (8) has been solved numerically for linear resistance R[11] and a current source driving the junction with a dc current. The solutions show that hysteresis grows for increasing capacitance. Numerical solutions with nonlinear resistances R, more closely resembling Giaever type tunneling should reflect the experimental I-V curve of a Josephson tunneling junction as shown in Figure 9 rather closely. The hysteresis is of interest for circuit design since it permits the switching of gate currents in excess of control currents without requiring that the $I_{\max}$ vs I_c characteristic exceeds a slope of unity, thus providing for logic gain.

Equation (8) describes the time dependence of the gate voltage $V(t)$ when either the gate current I_g exceeds the Josephson current threshold $I_{\max}$ or the Josephson current threshold $I_{\max}$ is reduced below the gate current I_g (for example by application of a control current I_c). For the voltage rise, the Josephson current term ($I_{\max}\sin\phi$) can be neglected in Equation (8). The solution is then given by

$$V(t)=I_g\cdot R(1-e^{-t/RC}) \qquad (9)$$

with R being approximated by the average resistance of the Giaever tunnel curve for $0<V<2\Delta/e$. The voltage tends to rise to $V_1=I_g\cdot R$. It is, however, clipped at $V=2\Delta/e$ because of the small differential resistance of the Giaever tunnel curve at $V_g=2\Delta/e$. For $I_g\cdot R\gg V_g$ one may, therefore, express the rise time approximately by $\Delta t=I_g\cdot C/V_g$.

The ($I_{\max}\sin\phi$) term cannot be neglected in the switching operation from $V=V_g$ back to $V=0$. Equation (8) must be solved numerically in this case. Simulations indicate that the ac Josephson currents play a role in this case leading to oscillations and requiring careful device and current design.

The equivalent circuit of a Josephson tunneling gate driving a superconducting loop is derived by adding a parallel inductance to the equivalent circuit of Figure 8. The corresponding differential equation is given by:

$$C\frac{dv}{dt}+\frac{1}{R}V+\frac{1}{L}\int V\,dt+I_{\max}(\sin\phi)=I \qquad (10)$$

Equation (10) indicates oscillatory behavior even when the Josephson current term is neglected if care is not taken to provide sufficient circuit damping. The complete Equation (10) must be evaluated numerically for each case under consideration.

It is, of course, of interest to test the validity of the equivalent circuit models for Josephson tunneling circuits. Switching times for voltage rise and current steering were measured and compared with calculated switching times on the basis of the equivalent circuits of Figure 8 without and with inductances.[12] Agreement is very good for voltage risetimes as short as 65 psec and current steering time of 550 psec. The current and voltage levels in this experiment were 17 mA and 2.5 mV, respectively, leading to a switching energy of $1.4\cdot10^{-15}$ Joule per switching operation or about 10 μW in continuous operation with 50 percent duty cycle. The circuit dimensions in the experimental work were rather large; a junction with an area of about 20 mil^2 and a loop with a length of 410 mil were used. It is expected that miniaturization with attendant reduction in capacitances and inductances will result in even shorter voltage rise and current steering times and in lower power dissipation.

JOSEPHSON TUNNELING CIRCUITS FOR MEMORY AND LOGIC FUNCTIONS

Some features of cryotron technology such as infinite resistance ratios of the ON and OFF states, trapping of magnetic flux, persistent current, etc., will also be exploited in Josephson tunneling circuits. Specific features of Josephson tunneling gates, such as the I-V hysteresis, the well defined and relatively large gap voltage V_g and the ease with which I_g vs I_c characteristics can be designed will undoubtedly be used to advantage, too.

The basic circuit configuration for register and memory elements is a superconducting loop comprising Josephson tunneling gates for steering currents from one branch into another and changing the direction (or amount) of magnetic flux trapped in the loop. The storage of binary data can, for example, be accomplished by setting up persistent supercurrents which

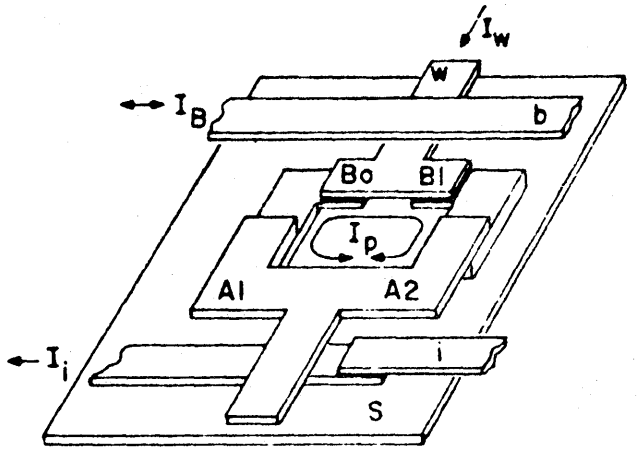

Figure 10—Memory cell comprising Josephson tunneling gates for coincidence selection and nondestructive readout.[13]

flow clockwise ("1") or counterclockwise ("0") as long as the loop remains superconducting.

As an example of a practical memory circuit[13] Figure 10 shows a superconducting loop comprising two Josephson tunneling gates for writing and controlling a third Josephson tunneling gate for nondestructive reading. The memory loop is in the selection line w; the control line b overlaying both write gates serves as a second selection line during writing; the interrogate line i, which comprises the sense gate S acts as a selection line during read out. The operation of the loop as a bit organized memory cell is described next under the assumption that there exists already a counterclockwise circulating current $I_w/2$ in the loop which represents a stored "0". First, a current pulse I_w is applied to line w, causing currents of amount $I_w/2$ to flow downwards through each branch of the loop. (Both branches are assumed to be equal inductance.) The applied and circulating currents superimpose, leaving the right branch without current and causing a total of I_w to flow in the left branch. The write gates are of the in-line configuration and their I_{max} vs I_c characteristic is assumed to be asymmetric ($\lambda_j < L$). A coincident current pulse I_B is then applied to the control line b. If I_B is directed from left to right (representing a write "0" signal) it increases I_{max} of the left write gate and decreases I_{max} of the right write gate. None of the gates will switch, however, since the actual gate currents—I_w in the left gate and 0 in the right gate—are smaller than the actual I_{max} values. If I_B is, however, directed from right to left (representing a write "1" signal), I_{max} of the left gate is decreased and I_{max} of the right gate is increased. With appropriate design $I_w > (I_{max})_{left}$, the left gate switches and develops a finite voltage, initiating transfer of the current I_w to the right branch until the current through the left gate falls below $I_{min} \sim 0$. This causes the left gate to return to $V=0$. The current I_w is now flowing through the right branch, and the loop has again become superconducting. Conservation of magnetic flux causes now a clockwise circulating current $I_w/2$ to flow in the loop representing a stored binary "1" upon termination of I_w in line w.

For reading of stored information, I_w is applied to w in coincidence with an interrogate current I_i flowing from right to left through line i. Superposition of I_w with a clockwise or counterclockwise circulating current subjects the sense gate underneath the right branch to a control current of $I_c = I_w$ and $I_c = 0$, respectively, thus rendering $I_{max} < I_i$ in the sense gate in case of a stored "1", and $I_{max} > I_i$ in case of a stored "0". In consequence, a finite voltage will be developed across the sense gate only for a stored "1" but not for a stored "0".

The current steering mode can be applied as well to larger loops comprising, for example, as branches selection lines w, b and i of memory arrays. It can be argued that array lines w, b and i in small memory arrays may be of about the same length as the loop (410 mil) of the high speed experiment mentioned in the third section. Hence, one may project memory cycle times in such arrays on the order of a nanosecond since usually the selection of array lines represents the major portion of the cycle time.

A drawback of the current steering mode in superconducting loops of extended length in high speed operation is the fact that the loops act as pairs of transmission lines above ground plane with a virtual short opposite the switching gate, thus causing multiple voltage and current reflections to travel along the lines and slowing the current steering operation. This behavior, especially undesirable in high speed logic circuits may be remedied. In Figure 11, the Josephson tunneling gate on the left drives a pair of striplines on top of a ground plane with a characteristic impedance Z_0. The strip lines which serve as control lines for other Josephson tunneling gates are terminated at the right

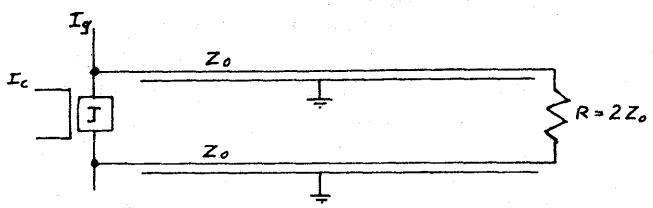

Figure 11—Schematic of high speed logic curcuit with terminated striplines

end by a resistor of resistance $R=2Z_0$. If the Josephson tunneling gate on the left switches from $V=0$ to $V=V_g$, two waveforms, one of amplitude $+V_g/2$ and the other of amplitude $-V_g/2$, will travel along the striplines; they will find a matched termination condition at the right end and be thus absorbed. Then the current $I_0=V_g/R$ will be established in the striplines right after the wavefront has propagated along the line. This current is a function of the (well defined) gap voltage V_g and the resistor R only.

Logic functions can be performed in different ways, for example, by overlaying several control lines on top of a Josephson tunneling junction or by interconnection of Josephson tunneling gates. If the 410 mil long loop in the high speed experiment had been properly terminated, the loop current would have been fully established in about 170 psec. (This assumes a 65 psec risetime and a phase velocity of 10^{10} cm/sec in the stripline.) In this case also, miniaturization is likely to reduce risetime and propagation delay.

TECHNOLOGICAL ASPECTS

An important question is, of course, whether useful devices and circuits can be made reproducibly, reliably and economically. A full assessment can only be made on the basis of a fairly extensive technological study; short of that, one must be content with collecting whatever data is available to date.

Following a recent review[14] it can be stated that Josephson tunneling junctions have been prepared using a variety of superconducting metals, tunnel barriers and preparation methods. A selection of superconductors, along with their critical temperatures T_c and energy gap 2Δ, which have reportedly been used for Josephson tunneling junctions are listed in Table I. Since operation at $T \leq \frac{1}{2}T_c$ is preferred because of the weak temperature dependence of Δ and j_1 in this range, niobium and lead electrodes are desirable candidates for this technology since they permit operation at

TABLE I—Superconducting Electrodes for Josephson Tunneling Junctions

Electrodes	T_c (°K)	$2\Delta_0$ (meV)
Nb	9.2	2.9
Pb	7.2	2.5
Sn	3.7	1
In	3.4	1
Al	1.26	0.38

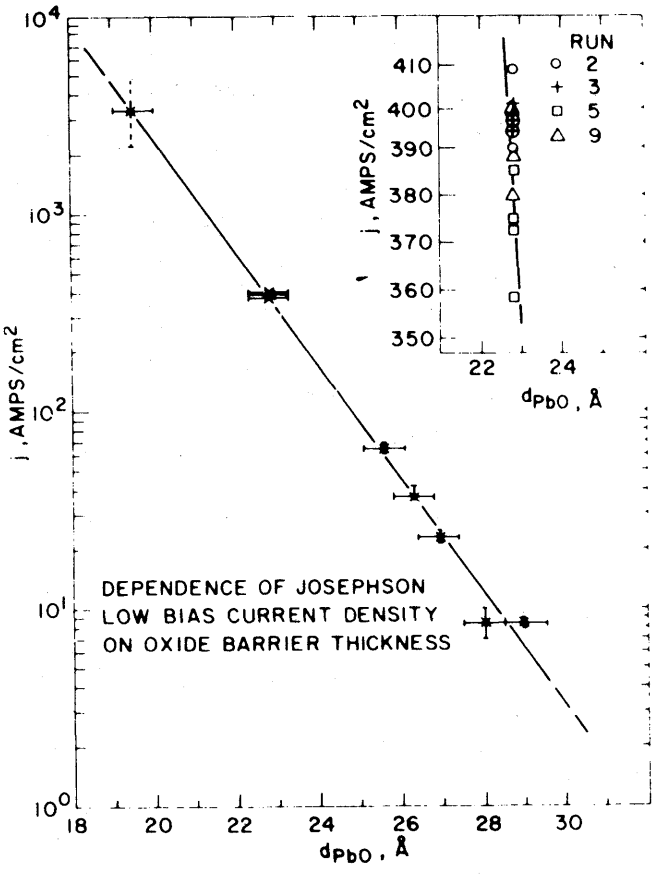

Figure 12—Diagram of Josephson current density versus oxide thickness in Pb-PbO_x-Pb junctions with indication (insert on upper right) of run to run reproducibility of barrier thickness and current density.[15]

about 4.2°K, the boiling point of liquid helium at atmospheric pressure.

Native oxides grown on the base electrode are preferable as suitable tunnel barriers for Josephson tunneling junctions. Successful attempts of barrier preparation by deposition of semiconductor films such as CdS,[15] tellurium[16] have also been reported. However, pinholes in the thin semiconductor films appear to pose a problem which is usually overcome by a subsequent oxidation step which fills the pinholes in the semiconductor films again by a native oxide. Hence, it appears to date, that native oxides grown on the bottom film electrode S_1 provide the best chance of getting shortfree tunnel barriers which are sufficiently thin to provide usable Josephson current densities for computer circuits.

Of major importance is the question of whether it is possible to control the growth of a thin oxide film with a thickness on the order of 20 Å to 30 Å sufficiently

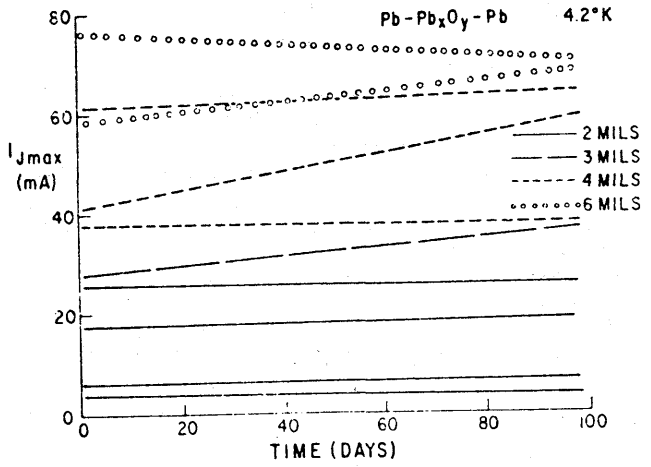

Figure 13—Diagram of Pb-PbO$_x$-Pb junction stability over extended period of time.[19]

uniformly and reproducibly to obtain reasonably reproducible Josephson current densities j_1. Figure 12 depicts the results of a thermal oxidation experiment[17] to produce Pb-PbO$_x$-Pb junctions in a well controlled oxygen atmosphere. The spread of current density j_1 is about ± 6 percent between independent oxidation runs and even less on the same samples.

Dc-glow discharge experiments have been reported[18] to result in a logarithmic time dependence of the oxide thickness from which one can conclude that the reproducibility is reasonable here, too.

Another interesting variation of the dc glow discharge oxidation has been reported[19] in which an *rf* source is used rather than a dc supply and the sample is affixed to the cathode. Two competing processes, oxide growth and removal of oxide by *rf*-sputtering are apparently at work leading to a simultaneous process of surface cleaning and oxide formation. The inherent surface cleaning aspect makes this method attractive for large scale circuit integration where the electrodes are being subjected to photoresist process steps prior to the formation of the oxide tunnel barriers.

Another technological aspect concerns the stability of the junction characteristics when they are thermally cycled between cryogenic and room temperatures and during shelf life. It was found that niobium junctions[20] are excellent in this aspect. Figure 13 shows that lead-lead oxide-lead junctions[21] can also be kept for an extended time at room temperature and can be thermally cycled a number of times without undue change of characteristics.

To date, the technological issues related to Josephson tunneling circuits may be described as having yielded some encouraging results; they can, however, not yet be considered as being solved. More effort will have to be invested to assess the feasibility and bring the technology to fruition.

SUMMARY

Relevant basic physical and computer circuit aspects of Josephson devices have been reviewed. It has been shown that Josephson tunneling devices are well characterized and perform in very good agreement with numerical calculations on the basis of simple models. They are potentially useful for high performance computer applications since they possess the necessary attributes of extremely high switching properties, and of extremely little power dissipation; they adapt readily to miniaturized LSI fabrication processes.

They do not suffer from basic switching speed limitations of cryotron circuits caused by superconducting—normal conduction phase changes and low voltages. On the contrary, they promise to surpass semiconductor circuit networks in operational speed, and provide memory functions with zero standby power.

Some technological aspects appear favorable, however, much more work is required in order to demonstrate feasibility. The potential, however, appears to warrant effort to address and solve technological problems.

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