Simulation of Intrinsic Parameter Fluctuations in Decananometer and Nanometer-Scale MOSFETs

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Invited Paper

Abstract—Intrinsic parameter fluctuations introduced by discreteness of charge and matter will play an increasingly important role when semiconductor devices are scaled to decananometer and nanometer dimensions in next-generation integrated circuits and systems. In this paper, we review the analytical and the numerical simulation techniques used to study and predict such intrinsic parameters fluctuations. We consider random discrete dopants, trapped charges, atomic-scale interface roughness, and line edge roughness as sources of intrinsic parameter fluctuations. The presented theoretical approach based on Green's functions is restricted to the case of random discrete charges. The numerical simulation approaches based on the drift diffusion approximation with density gradient quantum corrections covers all of the listed sources of fluctuations. The results show that the intrinsic fluctuations in conventional MOSFETs, and later in double gate architectures, will reach levels that will affect the yield and the functionality of the next generation analog and digital circuits unless appropriate changes to the design are made. The future challenges that have to be addressed in order to improve the accuracy and the predictive power of the intrinsic fluctuation simulations are also discussed.

Index Terms—Interface roughness, intrinsic parameter fluctuation, line edge roughness, MOSFETs, numerical simulation, random discrete dopants, scaling.

I. INTRODUCTION

IN the past couple of years, MOSFETs have reached decananometer (between 10 and 100 nm) dimensions with 40–50 nm physical gate length devices that are available now in the 90-nm technology node [1], [2], 35–nm transistors ready for mass production in 2 to 3 years time [3] and 15 nm [4], and even 10 nm [5] MOSFETs with conventional architecture demonstrated in a research environment. The 2001 edition of the International Technology Roadmap for Semiconductors forecasts that the MOSFET will become a nanometer scale (i.e.

sub-10 nm) device after 2016 when its physical dimensions in a mass production environment will reach 9 nm [6].

Fig. 1 shows that MOSFETs are becoming truly atomistic devices. The conventional way of describing, designing, modeling and simulating such semiconductor devices, illustrated in Fig. 1(a), assuming continuous ionised dopant charge and smooth boundaries and interfaces, is no longer valid. The granularity of the electric charge and the atomicity of matter, as illustrated in Fig. 1(b), begin to introduce substantial variation in individual device characteristics. The variation in number and position of dopant atoms in the active region of decananometer MOSFETs makes each transistor microscopically different and already introduces significant variations from device to device [7]. In addition, the gate oxide thickness becomes equivalent to several atomic layers with a typical interface roughness of the order of 1 to 2 atomic layers [8]. This will introduce a variation in the oxide thickness within an individual transistor of more than 50%, resulting in each transistor having a microscopically different oxide thickness pattern. The unique oxide roughness pattern in each decananometer MOSFET will affect the device electrostatics, the surface roughness limited mobility and the gate tunnelling from device to device. The granularity of the gate material and the photoresist, together with other factors, will introduce unavoidable line edge roughness (LER) in the gate pattern definition and statistical variations in geometry between devices [9].

When combined, the variations in dopant statistics, oxide thickness pattern, gate material, and geometry will have a crucial impact on the functionality, yield, and reliability of the corresponding circuits and systems at a time when the fluctuation margins shrink due to continuous reduction in supply voltage and increased transistor count per chip. As it has been shown in the past [10]–[13], such fluctuations might affect not only analogue circuits but also the yield and functionality of the corresponding digital circuits. For example, in a 10 billion-transistor chip, at least 20 transistors are expected to have a 6σ deviation in their parameters, assuming Gaussian statistics. With 0.85-V supply voltage and expected threshold voltage standard deviation σV_T in the range of 20–30 mV, there will be at least 20 transistors with threshold voltage of zero or half the supply voltage.

The sub 10-nm MOSFET illustrated in Fig. 1(c) is essentially a molecular scale device. It is anticipated, however, that the scaling of the field effect transistor below the 10-nm barrier

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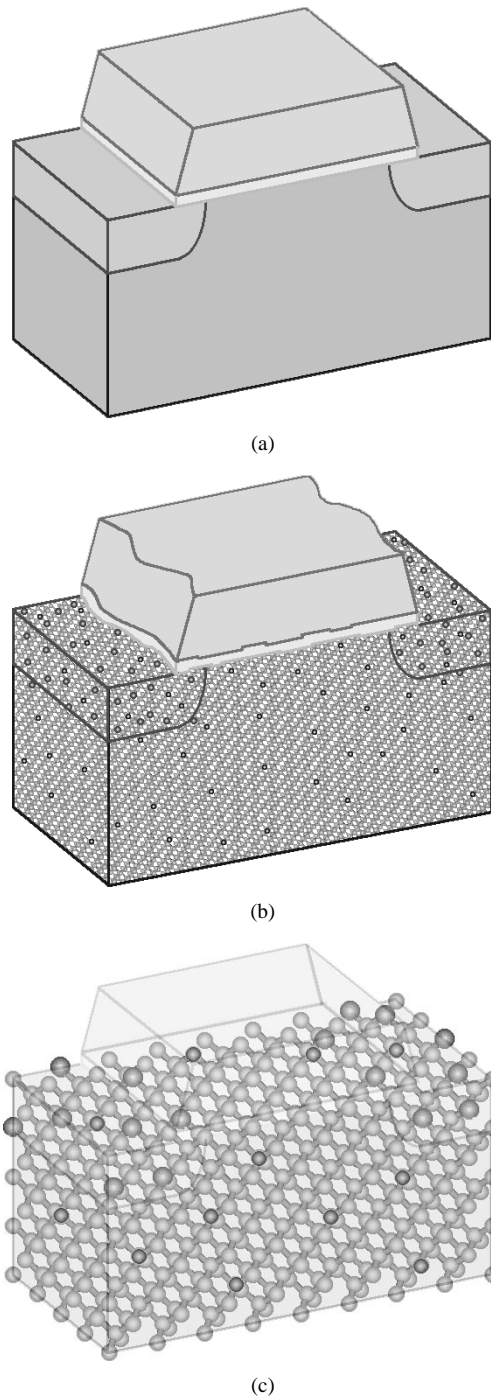
(a)

(b)

(c)

Fig. 1. Transition from continuous toward "atomistic" device concepts. (a) Current approach to semiconductor device simulation assumes continuous ionised dopant charge and smooth boundaries and interfaces. (b) Sketch of a 20-nm MOSFET expected in mass production before 2010. There are less than 50 Si atoms along the channel. Random discrete dopants, atomic scale interface roughness, and line edge roughness introduce significant intrinsic parameter fluctuations. (c) Sketch of a 4-nm MOSFET expected in mass production in 2020. There are less than 10 Si atoms along the channel. The device becomes smaller than biologically important molecules such as ionic channels.

requires an intolerably thin gate oxide and unacceptably high channel doping and therefore demands a departure from the conventional MOSFET concepts [14]. One of the most promising new device structures that is scalable to dimensions below 10 nm is the double gate MOSFET studied extensively in the last couple of years [15]. To allow a full appreciation for the
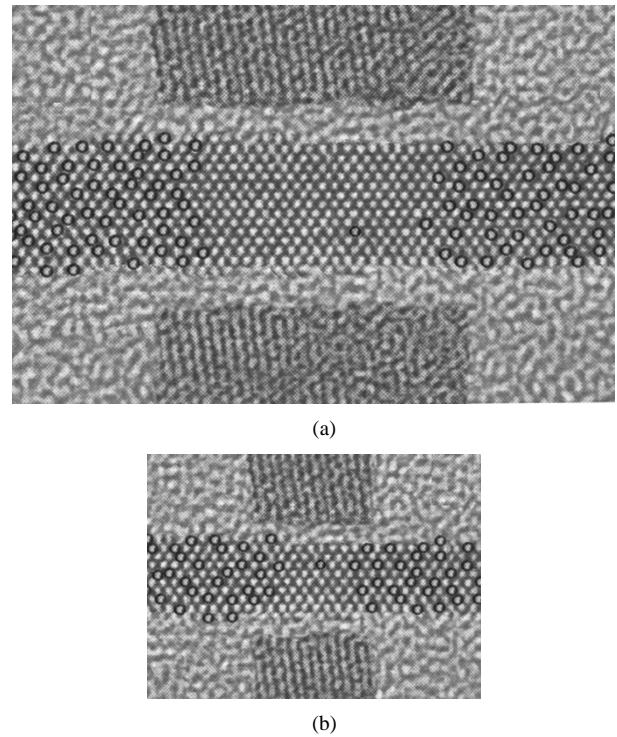

(a)

(b)

Fig. 2. Impression of (a) 10-nm and (b) 4-nm gate length double gate MOSFETs based on a TEM image of the Si-SiO$_2$ interface to illustrate the various sources of intrinsic parameter fluctuations.

importance of the atomic scale effects in such devices, we present, in Fig. 2(a), and (b), respectively, the atomic scale structure of a 10-nm and a 4-nm double gate MOSFET "fabricated" using Photoshop and a real TEM image of the Si/SiO$_2$ interface.

In this paper, we review the analytical and the numerical simulation techniques used until now to study and predict the intrinsic parameter fluctuations in decananometer and nanometer scale MOSFETs. The paper is illustrated with simulation results highlighting the importance of the various sources of intrinsic parameter fluctuations in the next-generation semiconductor devices. We also identify the current limitations and the future challenges facing the "atomistic" device simulation.

II. THEORETICAL CALCULATIONS OF FLUCTUATIONS

Of the numerous sources of fluctuations described in the preceding section, the electrostatic potential due to random charges is the most amenable to theoretical analysis. There are two principal sources of such charges: fixed charges in the oxide and ionised impurities in the depletion layer. Fluctuations in early devices were dominated by oxide charges, whose effect was first studied theoretically by Brews [16]. The mobility of MOSFETs at low density and temperature is also limited by these oxide charges [17]. The effect of oxide charges on the interface potential [18], [19], [107], carrier density [20], energy levels [21], and mobility [22] have been calculated. Nicollian and Brews [23] provide a comprehensive review of the early work.

Since the 1980s, improved technology has reduced the density of charges in the oxide, while scaling laws require greatly increased doping in the channel of deep submicron devices.
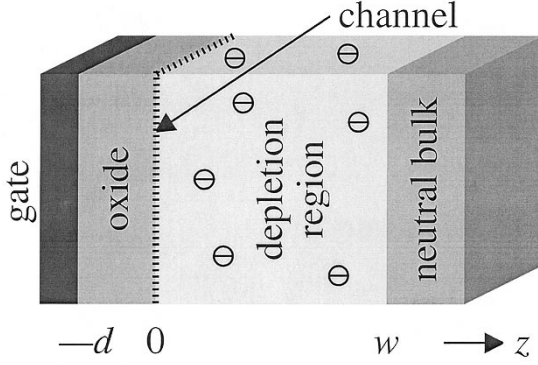
Fig. 3. Interior of a MOSFET showing gate, oxide, and random charges in the depletion layer.

Thus the dominant source of random charges is now the depletion layer near the channel rather than the oxide, a situation that also holds in III–V devices [24], [25]. We shall now show how Brews' approach [16] can be extended to treat these charges. The calculations are based on the same simple model of the layers in a MOSFET, shown in Fig. 3. We take z as the normal to the layers and assume them to be of infinite extent in x and y; no account is taken of the source, drain and lateral boundaries. The features of the model are as follows.

1) The gate is a perfect conductor and occupies the region $z < -d$.
2) The oxide has thickness t_{ox} and dielectric constant κ_{ox}. Fluctuations in its thickness and random charges are neglected.
3) The channel has infinitesimal thickness and lies at the silicon-oxide interface in the plane $z = 0$.
4) The depletion layer of thickness w and dielectric constant κ_{sc} contains no carriers. The acceptors are fully ionised and random in x and y with average concentration $N_A(z)$, which may vary as a function of depth.
5) The bulk of semiconductor ($z > w$) is neutral; its interface with the depletion layer is abrupt and flat, and is therefore treated like a metal plate at $z = w$.

The "bare" potential from the impurities may be reduced by screening due to free electrons or holes in the channel. Far below threshold the channel is nearly empty and there is no such screening. The definition of threshold used in the simulations [26] is close to this limit. In the opposite limit, well above threshold, the density of electrons is so high that linear screening holds, and we will also provide results for this case. Between these two limits, just above threshold, the density of electrons is grossly inhomogeneous and screening is strongly nonlinear [27].

The strategy of the calculations is as follows. They are centred on the Green's function $G(|\mathbf{r} - \mathbf{r}'|; z, z')$, which gives the electrostatic potential at the point $(\mathbf{r}, z)$ due to a unit charge at $(\mathbf{r}', z')$. We assume that the sample has translational and rotational invariance in the plane $\mathbf{r} = (x, y)$ after averaging. The Green's function includes the electrostatic effect of all the layers in Fig. 3 and any screening due to carriers in the channel. This is used to construct the power spectrum and autocorrelation function of the fluctuations. The two most important quantities that can be deduced from the autocorrelation function are the vari-

ance, which gives the magnitude of the fluctuations in potential, and the correlation length, which is the scale over which they vary in space. As an example we take a device with oxide $t_{ox} = 3$ nm thick, depletion layer $w = 18$ nm thick, nominally uniform doping of channel $N_A = 5 \times 10^{18}$ cm^{-3}, and density of electrons above threshold $N_i = 10^{12}$ cm^{-2}. The dielectric constants are $\kappa_{sc} = 11.8$ for the semiconductor and $\kappa_{ox} = 3.9$ for the oxide. Further details are given in [28].

A. Green's Function for the Potential

We shall calculate only the potential at the silicon-oxide interface ($z = 0$). This requires the Green's function $G(r; 0, z)$, where r and z give the location of the random charge in the depletion layer. For most calculations it is more convenient to use the two-dimensional (2-D) Fourier transform $\tilde{G}(q; 0, z)$, which is defined by

$$\tilde{G}(q; 0, z) = \int G(r; 0, z) e^{-i\mathbf{q}\cdot\mathbf{r}} d^2\mathbf{r}. \tag{1}$$

This can be written in terms of the Green's function $\tilde{G}(q)$ for both points at the interface

$$\tilde{G}(q; 0, z) = \frac{\sinh q(w - z)}{\sinh qw} \tilde{G}(q). \tag{2}$$

Brews [16] showed that the Green's function in the absence of screening due to electrons in the channel is given by

$$\tilde{G}_0(q) = \frac{1}{\varepsilon_0 q(\kappa_{ox} \coth qt_{ox} + \kappa_{sc} \coth qw)}$$
$$= \frac{1}{2\varepsilon_0 \bar{\kappa} (Q_s^2 + q^2)^{\frac{1}{2}}} \tag{3}$$

where $\bar{\kappa} = (1/2)(\kappa_{ox} + \kappa_{sc})$ is the average dielectric constant at the interface. The usual Fourier transform of the Coulomb potential is $1/(2\varepsilon_0 \bar{\kappa} q)$, and the remaining factors show how the potential is screened by image charges in the gate and by the carriers below the depletion layer. These are expressed as a geometrical screening wavevector

$$Q_s \approx \frac{\frac{\kappa_{ox}}{t_{ox}} + \frac{\kappa_{sc}}{w}}{\kappa_{ox} + \kappa_{sc}}. \tag{4}$$

The gate makes the greater contribution but only by a factor of around 2 in a well-scaled device. The approximate Green's function can be inverted to real space, giving

$$G_0(r) = \frac{\exp(-Q_s r)}{4\pi\varepsilon_0 \bar{\kappa} r}. \tag{5}$$

This is a screened Coulomb potential decaying exponentially with the characteristic length $1/Q_s \approx 8$ nm. It shows that long-ranged potential fluctuations are damped by the image charges induced in the gate and the edge of the depletion layer.

Well above threshold, linear screening [29] contributes an additional term to the inverse of the Green's function, giving

$$\tilde{G}_0(q) = \frac{1}{\varepsilon_0 q(\kappa_{ox} \coth qt_{ox} + \kappa_{sc} \coth qw) + 2\varepsilon_0 \bar{\kappa} q_s}$$
$$\approx \frac{1}{+2\varepsilon_0 \bar{\kappa} \left[(Q_s^2 + q^2)^{\frac{1}{2}} + q_s\right]} \tag{6}$$
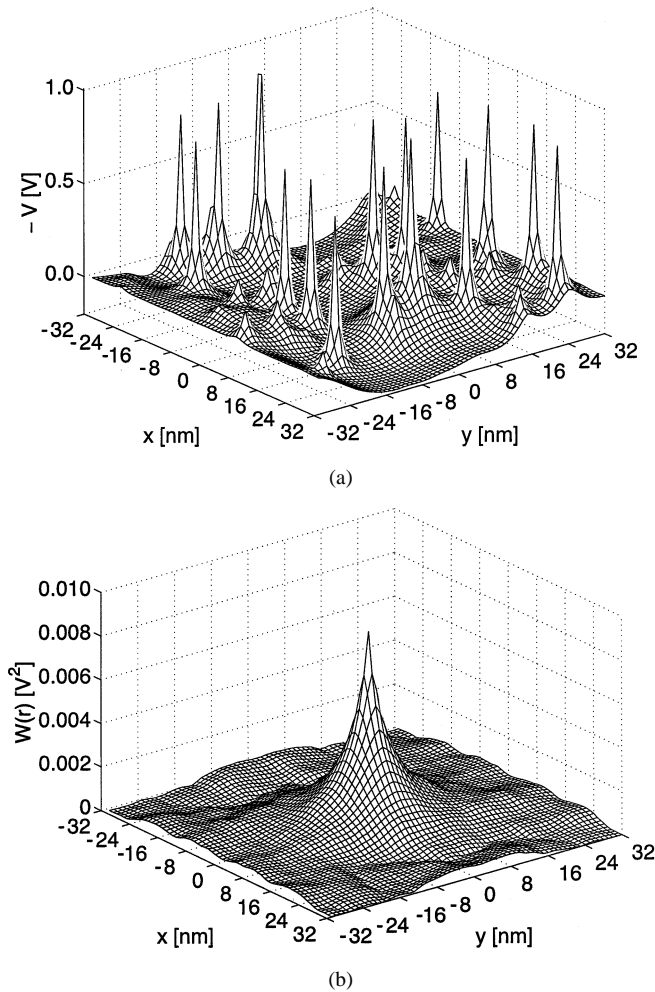
(a)

(b)

Fig. 4. (a) Typical example of the random potential near threshold at the Si-SiO$_2$ interface. (b) Corresponding autocorrelation function.

At room temperature, the screening wavevector [16] is given by $q_s = (e^2 N_i / 4 \varepsilon_0 \bar{\kappa} k_B T)$. The corresponding length is $1/q_s \approx 5$ nm for our example, showing that screening by carriers in the channel above threshold is somewhat stronger than the effect of the boundaries alone below threshold. Unfortunately there appears to be no simple, accurate expression for the Fourier transform back to real space of the screened potential.

B. Variance and Correlation Function of the Random Potential

Fig. 4(a) shows a typical example of the random potential $\phi(\mathbf{r})$ at the silicon-oxide interface in an area of 64×64 nm. The form of this potential depends on the positions of the random dopants in the depletion layer and can be repeated for many configurations. Its two most important features are the magnitude of the fluctuations, given by the variance or standard deviation, and the length scale on which the potential varies, given by the correlation length. These can be deduced from the (auto)correlation function of the potential, which is defined by

$$W(r) = \langle \phi(r')\phi(r' + r) \rangle_{r'} . \qquad (7)$$

This shows how the potential at any point $\mathbf{r}'$ is related to that at a point displaced by $\mathbf{r}$ and is averaged over $\mathbf{r}'$. The autocorrelation function for the potential in Fig. 4(a) is plotted in Fig. 4(b).

It rises to a central peak at the origin and the variance of the potential is given by $W(0)$. The correlation length is defined by the distance over which $W(r)$ decays by a factor of $1/e$.

The Fourier transform of $W(r)$ can be found by integrating the Green's function over the random charges in the depletion layer, which gives

$$\tilde{W}(q) = e^2 \int_0^w \left| \check{G}(q; 0, z) \right|^2 N(z) dz. \qquad (8)$$

The integral over z can often be performed analytically but the inverse Fourier transform must usually be evaluated numerically. In the case of an empty channel, however, there is a good approximation for a well-scaled device [28]

$$\tilde{W}(q) \approx \frac{N_A}{2} \left(\frac{e}{2\varepsilon_0 \bar{\kappa}} \right)^2 \frac{1}{(\alpha^2 + q^2)^{\frac{3}{2}}} \qquad (9)$$

where $\alpha^3 = 3Q_s^2/2w$. This can be inverted to real space, giving

$$W(r) \approx \frac{N_A}{4\pi Q_s} \left(\frac{e}{2\varepsilon_0 \bar{\kappa}} \right)^2 \left(\frac{2}{3} Q_s w \right)^{\frac{1}{3}} \exp(-\alpha r). \qquad (10)$$

The factor in front of the exponential function gives the variance, which shows that $\sigma = 70$ mV for the example. This is in excellent agreement with 69 mV from a numerical evaluation of (8) using the exact Green's function. This expression also shows that the autocorrelation function decays exponentially with a length scale $L = 1/\alpha = 9$ nm. The size of features is typically around twice the correlation length and is therefore the same as the thickness of the depletion region. This convenient relation relies on good scaling with the thicknesses of the depletion region and oxide related by $w \approx 6d$.

The integrals must be evaluated numerically when screening by carriers in the channel is included in the Green's function. The standard deviation is reduced from 69 to 40 mV and the correlation length is reduced to 5 nm so that the effect of this additional screening is not dramatic.

C. Effect of Fluctuations on Threshold Voltage

It has been recognized since the early 1970s that the random positions of charges leads to fluctuations in the characteristics of individual devices [30], [36]. The randomness also reduces the average threshold voltage because current can percolate through the favorable regions of the fluctuations in the potential in the channel.

It is not straightforward to go from the statistics of the potential in the channel to the threshold voltage because this requires a model of conduction through the random potential. This in turn depends on the relation between the length scales of the fluctuations and the device. For example, if the device is large compared with the correlation length, which is in turn much longer than the mean free path, a breakdown of the real device into a mosaic of statistically different transistors [31] may be an appropriate model. This is close to the checkerboard originally considered by Keyes [30].

In the opposite limit, where the transistor is small compared with the correlation length, the standard deviation of the threshold voltage is the same as that of the random potential.
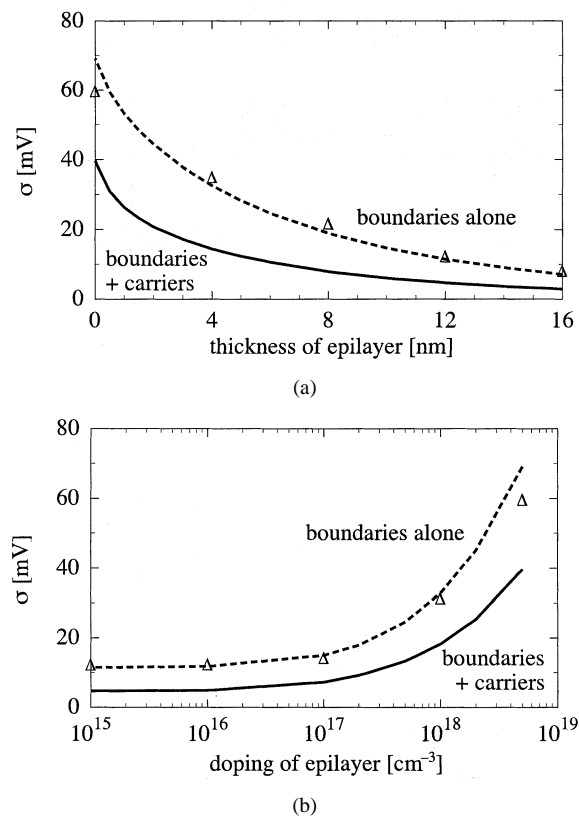
Fig. 5. Standard deviation of fluctuations in a MOSFET as a function of (a) thickness and (b) doping of a lightly doped epitaxial channel. Lines show the random potential calculated analytically and points are the results of atomistic simulations.

We have seen that the length scale L of the fluctuations is roughly the same as the thickness of the depletion region w, and the length of a well-scaled device is typically $3w$; therefore, this is not obviously applicable. However, conduction at threshold with a small source-drain voltage is limited by the potential barrier in the middle of the channel, whose length is comparable to L. Fluctuations turn the barrier into an irregular mountain range and current starts to flow when the first pass through the mountains becomes accessible. The width of the simulated devices is larger than L and the variance of the potential should therefore be reduced by a factor of $(2L)/(\text{width of device})$ to allow for several passes through the mountain. A further correction is also needed because there is a "lever" factor of about 2 between the change in gate voltage and the corresponding change in potential in the channel. This roughly cancels the factor due to the width of our particular device and we simply compared the threshold voltage in simulations directly with the analytic random potential. An example is shown in Fig. 5, where we studied the effect of a lightly doped epilayer on the fluctuations in the threshold voltage [28], [32]. There is good agreement between the numerical and analytic work and both show that the standard deviation can be reduced from 60 mV to about 10 mV by a lightly doped 12-nm layer.

D. Extensions of the Theory

It is relatively straightforward to extend the theory described here to more complicated layers. For example, a lightly doped layer next to the silicon-oxide interface can be shown to reduce

the fluctuations dramatically [28]. The effect of a polysilicon gate could be treated in the same way and the thickness of the channel could be included. This would account for quantization [21] and the spread of the inversion layer as the temperature rises. It is a great deal more difficult to perform the calculation for a device of finite area to account for the source, drain, and lateral boundaries. This is important because the effect of ionised impurities is reduced by screening near the source or drain because of their heavy doping. (Against this, it is the impurities in the middle of the device that have the largest effect on the threshold characteristics.) The general approach described in this section would work but translational invariance in **r** would no longer hold and the variance of the random potential would be a function of position in the device. The Green's function would almost certainly have to be calculated numerically.

Given that numerical methods are probably essential, can the full power of a device simulator be harnessed within an analytic framework? A study has already been made of the effect of a single, random charge on the characteristics of a MOSFET [33]. This showed that a single charge in a device with no other randomness had the greatest effect when it was at the middle of the channel. When all ionised impurities were treated as discrete, random charges the effect was more complicated, and the effect of the single charge was amplified when it lay near a critical path for the source-drain current.

Mayergoyz and Andrei [34] have recently proposed that the results of a similar numerical calculation can be analyzed to yield the variance of the threshold voltage, averaged over all possible configurations of the impurities. Computationally, this is less expensive than the "brute force" method of averaging the results over many devices, described in the next section of this paper. This type of approach—harnessing the strong points of numerical and analytical techniques—will surely grow as more subtle effects of fluctuations are investigated.

III. NUMERICAL SIMULATION

The statistical variations in decananometer devices shift the paradigm of numerical device simulations [35]. It is no longer sufficient to simulate a single device with continuous doping distribution, uniform oxide thickness, and unified dimensions to represent one macroscopic design. Each device is microscopically different at the level of dopant distribution, oxide thickness and gate pattern; therefore, an ensemble of macroscopically identical but microscopically different devices must be characterized. The aim of the numerical simulation shifts from predicting the characteristics of a single device toward estimating the mean values and the variance of basic design parameters, such as threshold voltage, subthreshold slope, transconductance, drive current, etc., for a whole ensemble of microscopically different devices in the system. It must be emphasised that even the mean values obtained from, for example, statistical atomistic simulations are not identical to the values corresponding to continuous charge simulation. The simulation of a single device with random dopants, oxide thickness and gate pattern variation requires a three–dimensional (3-D) solution with fine grain discretization. The requirement for statistical simulations transforms the problem

into a four-dimensional one where the fourth dimension is the size of the statistical sample. The result from the physical simulation of intrinsic fluctuations in ensembles of devices has to be transferred into statistical circuit level models. Statistical circuit simulations have to be carried out in order to estimate at what scaling stage the intrinsic fluctuations in a particular device architectures will become unacceptable from circuit and systems point of view.

A. Random Discrete Dopants

The intrinsic parameter fluctuations associated with discrete random dopants in MOSFETs were predicted in the early seventies [36], [37] and first treated analytically and numerically in [38]. The predicted threshold voltage fluctuations were experimentally confirmed for a wide range of fabricated and measured MOSFETs [7], [39]–[41] down to sub 0.1 μm dimensions [42]–[45]. Several analytical models with different degrees of complexity describing the random dopant induced threshold voltage fluctuations in MOSFETs have been developed over the years [38], [39], [41], [46], [47]. Two-dimensional numerical simulations have also been used to study, to some extent artificially, the effects of random dopant fluctuations in devices with channel lengths down to 0.1 μm [38], [48], [49].

Due to sheer computational intensity most of the 3D statistical atomistic simulation studies published up to now, which take into account the discrete random distribution of dopants, are based on the drift-diffusion (DD) approach [26], [32], [35], [48], [50]–[54]. In [55], the principles of 3-D atomistic hydrodynamic simulations were illustrated but no analysis of fluctuation phenomena on a statistical scale were carried out. Only recently have quantum mechanical corrections based on the density gradient (DG) algorithm [56]–[58] been introduced into 3-D atomistic DD simulations and used to study the impact of the quantum mechanical confinement effects on the random dopant-induced intrinsic parameter fluctuations [59], [60].

It is clear that the drift-diffusion approach does not properly represent the nonequilibrium carrier dynamics and ballistic transport effects in decananometer MOSFETs and, hence, underestimates the drain current. However, in atomistic simulations, it can be used with confidence to estimate the threshold voltage based on a current criterion in the subthreshold region, where the current is exponentially controlled by the gate and its underestimation produces a minute error in the calculated value for the threshold voltage. Above threshold the quantum corrected DD simulations provide a sufficiently accurate estimate for the variation in the device parameters resulting from the electrostatics of random discrete dopants, local oxide thickness variations, and LER. Effects associated with mobility and carrier velocity variation due to variation in the Coulomb scattering from different ionised impurity configurations in each microscopically different MOSFET from the sample are also excluded from the above simulation studies.

A typical atomistic solution domain used in the simulation of well scaled 50 × 50 nm MOSFET is shown in Fig. 6(a). The discrete dopants are placed in the active region of the device including the source and drain. In the rest of the simulation domain the doping charge has a continuous distribution to simplify the
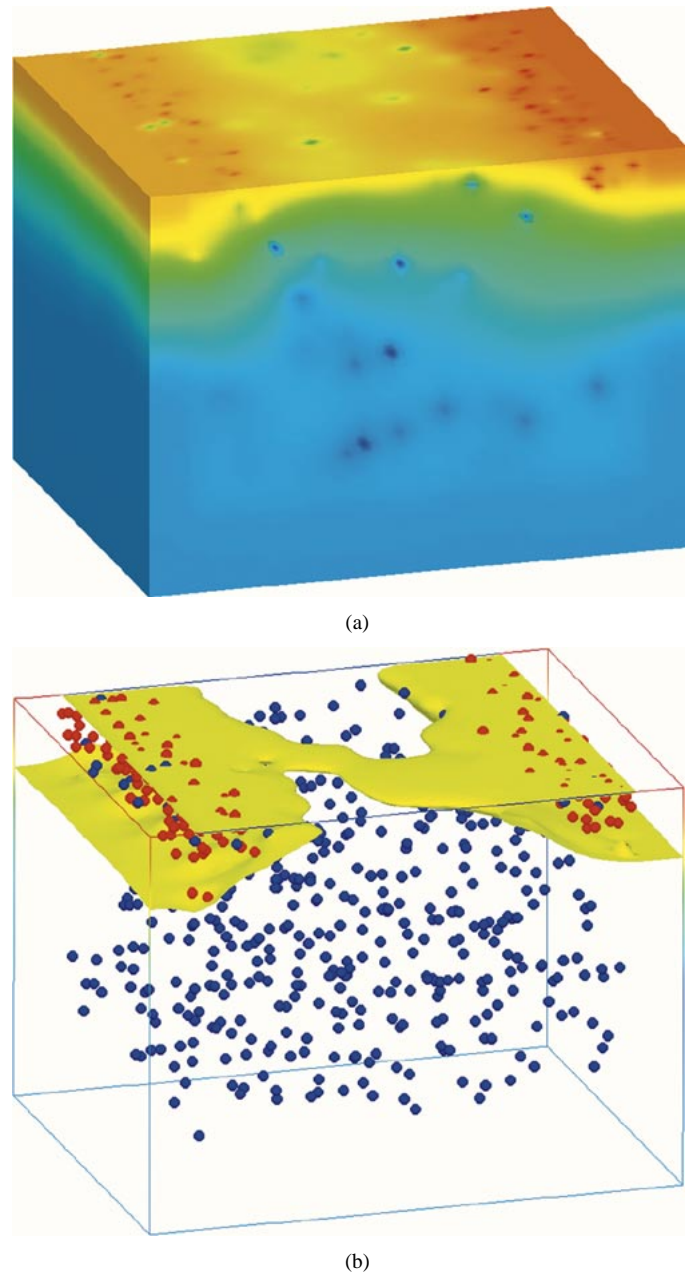

(a)

(b)

Fig. 6. Simulation domain in typical atomistic DG simulations of a 50 × 50 nm MOSFET. (a) Potential distribution indicating also the positions of the individual dopants. (b) One equi-concentration contour.

handling of the boundary conditions. In ohmic boundary conditions used at the contact region, the doping concentration is used to define electro neutrality. This is how boundary conditions are imposed in traditional simulations. Numerical experiments show that only dopants that are adjacent to the active region of the device influence the fluctuations [61]. Although the best way to introduce the doping distributions in the atomistic simulations would be to use the output from an atomic scale process simulator [62], [63], all of the previously published simulation studies generate random dopant distributions from continuous doping distributions [26], [48], [50], [51], [53], [55]. Typically, the expected number of each sort of dopant in the atomistic simulation region is estimated by integrating the continuous doping distribution, which is obtained, for example,

from a standard process simulator. The actual number of dopants in each MOSFET from the simulated ensemble is chosen randomly from a Poisson distribution with the above mean. Then, using a rejection technique [64], the dopants are placed randomly according to the initial continuous doping distribution. A more precise approach for generating random dopant distribution is used in [52]. Each and every silicon atom position in the simulated device is identified, and a random number is rolled to determine whether or not it is a dopant depending on the local continuous doping concentration.

The potential distribution at a gate voltage equal to the threshold voltage is depicted in Fig. 6(a) and exhibits strong potential fluctuations at the Si-SiO$_2$ interface associated with the discrete dopants. One electron equi-concentration contour, which corresponds to this solution, is presented in Fig. 6(b). The equi-concentration contour highlights the basic features of the quantum charge distribution. The quantum confinement in the channel results in a smoothing of the carrier density profile with a maximum in the electron concentration, which is located approximately 1.5 nm below the interface.

In general, for devices with channel length below 100 nm and channel doping concentrations $N_A > 10^{18}$ cm^{-3}, the classical atomistic simulations show that the doping concentration dependence of the random dopant induced threshold voltage fluctuations σV_T is stronger than the $N_A^{0.25}$ dependence suggested by many analytical models [38], [39], [41], [46]. This discrepancy is associated with the fact that the these analytical models only take into account the fluctuation of the total number of dopants in the channel depletion region but do not include the effects associated with the random position of the individual dopants. The atomistic simulations have, however, confirmed that the theoretically predicted $(L_{eff}W_{eff})^{-1/2}$ channel length and width dependence of σV_T, and its proportionality to the oxide thickness t_{ox} remains valid in properly scaled decananometer MOSFETs with uniform channel doping. By fitting our atomistic results in the range of L_{eff} from 30 to 100 nm, W_{eff} from 50 to 500 nm, t_{ox} from 1 to 6 nm and N_A from 1×10^{18} cm^{-3} to 5×10^{18} cm^{-3}, we have extracted a useful empirical expression relating σV_T to the basic structural MOSFET parameters:

$$\sigma V_T = 3.19 \times 10^{-8} \frac{t_{ox} N_A^{0.4}}{\sqrt{L_{eff} W_{eff}}} [V]. \tag{11}$$

This shows a weaker dependence on doping than the random potential within an infinite device, which would give $\sigma V_T \propto N_A^{1/2}$.

Further, we concentrate on effects related to quantum mechanics [59] and the polysilicon gate [54]. The dependence of the threshold voltage on oxide thickness, which is obtained from classical and quantum DG simulations, is presented in Fig. 7 for a 50 $\times$ 50 nm MOSFET. With channel doping concentration 5×10^{18} cm^{-3} such devices have, on average, 170 atoms in the channel depletion region. Samples of 200 microscopically different devices are simulated to extract the average threshold voltage and its standard deviation for each macroscopic combination of device design parameters. Results for the average threshold voltage, obtained from atomistic simulations, and for the threshold voltage, obtained from continuous charge simulations, are compared for metal and poly-silicon gate devices.
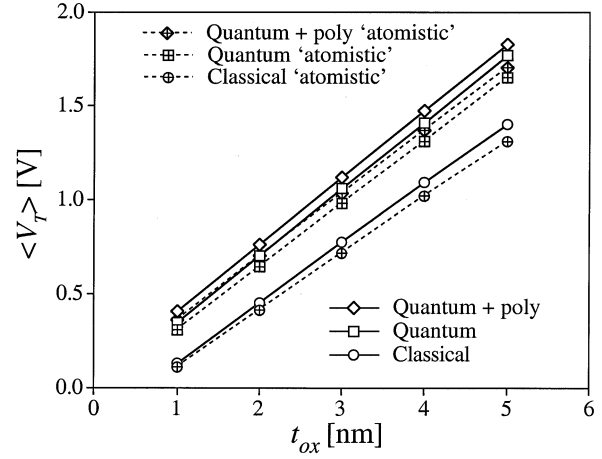

Fig. 7. Dependence of threshold voltage on the gate oxide thickness in a 50 $\times$ 50 nm MOSFET.

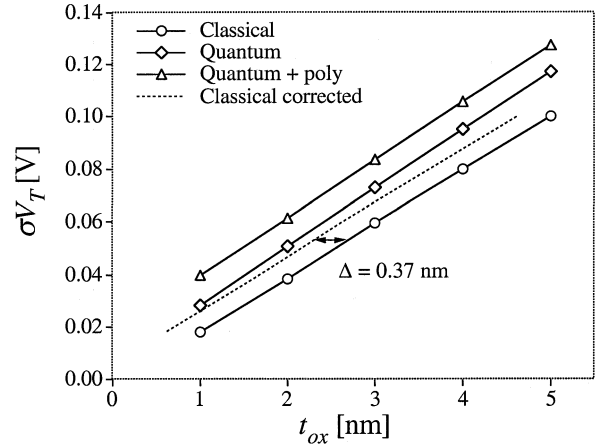Fig. 8. Threshold voltage standard deviation as a function of the oxide thickness in a 50 $\times$ 50 nm MOSFET. "Classical corrected" means that the oxide thickness is increased by the distance between the interface and the centroid of the quantum mechanical charge distribution.

The quantum mechanical threshold voltage shift decreases with the reduction in the oxide thickness t_{ox}. The inclusion of the poly-Si gate in the simulations results in additional increase in the threshold voltage due to the well know poly-depletion effect [65]. Most importantly, the random dopant induced threshold voltage lowering, inherent to the atomistic simulations, and associated with percolation of the channel current through "valleys" in the potential fluctuations is enhanced in the quantum case.

The dependence of the threshold voltage standard deviation, σV_T, on oxide thickness, extracted from classical and quantum atomistic simulations, is plotted in Fig. 8. In the classical simulations of metal gate devices, σV_T scales linearly to zero with the corresponding scaling of t_{ox} as a result of the screening from the gate. The values of σV_T corresponding to the quantum simulations are shifted up with respect to the classical simulations, and the shift increases slightly with the increase in the oxide thickness. The inclusion of the poly-silicon gate in the simulations results in an additional increase of σV_T, due both to an increase in the effective oxide thickness and remote enhancement of the surface potential fluctuations associated with the random
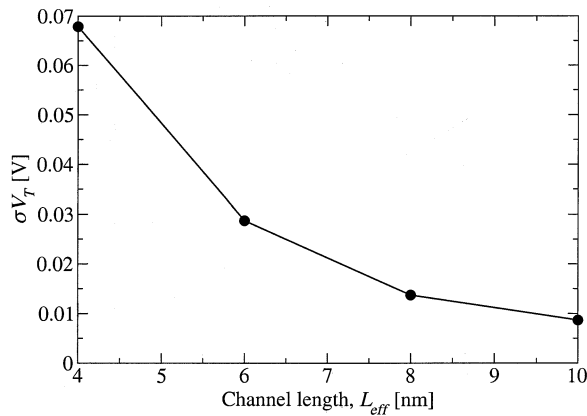
Fig. 9. Standard deviation in threshold voltage, σV_T, due to random discrete dopants in the source and drain of double gate MOSFETs with different channel lengths.

dopant distribution in the polysilicon gate itself [54]. This, in combination with the increase associated with the quantum mechanical effects, almost doubles the fluctuations for oxide thickness below 2 nm compared with pure classical simulations.

Numerical simulations have shown that the dopants closest to the interface are responsible for a large fraction of the intrinsic parameter fluctuations and this is confirmed by analytic work [28]. Therefore, devices with steep halo channel doping of low doped epitaxial channels [32] show significant dopant fluctuation resistance, which is seen in Fig. 5. Double-gate devices do not require channel doping to operate and therefore are considered to be inherently resistant to random dopant induced parameter fluctuations [66]. However, when the double gate devices are scaled to dimensions below 10 nm (see Fig. 2), the placement of random discrete dopants in the source/drain regions results in fluctuations in the effective channel length along the width of the device on a scale comparable to the average distance between the dopants. At typical source/drain doping concentrations in the range of 10^{20} cm^{-3} the average distance between the dopants is about 2 nm, constituting a large proportion of the channel length and becoming accountable for significant variations in the device parameters. The dependence of the standard deviation in threshold voltage σV_T as a function of channel length are shown in Fig. 9 for well-scaled double-gate MOSFETs [67]. The magnitude of the fluctuations increases dramatically as the channel length reduces from 10 to 4 nm. For the 4-nm device the standard deviation in threshold voltage is approximately 70 mV. Assuming a $\pm 3\sigma$ spread around the mean in a normal distribution of V_T, this gives a range of approximately ± 0.2 V around the nominal threshold voltage of $V_T \approx 0.2$ V. This means that a significant number of the devices on a chip with a billion transistors will not turn off.

B. Single Charge Trapping

Trapping of a single carrier charge in defect states near the Si/SiO$_2$ interface, and the related local modulation in carrier density and/or mobility [68]–[70] in an area comparable with the characteristic device dimensions, will have a profound effect on the drain and gate current [71] in decananometer MOSFETs. Corresponding random telegraph signals (RTS)

with amplitudes larger than 60% have already been reported at room temperature in decananometer channel width devices [72]. Current fluctuations on such a scale will become a serious issue, not only as a source of excessive low-frequency (LF) noise in analog and mixed-mode circuits [73], [74], but also in dynamic memories [75] and possibly in digital applications. Depending on the device geometry a single [76] or few discrete charges [77] trapped in hot carrier or radiation created defect states will be sufficient to cause a pronounced degradation in decananometer MOSFETs. However, the modeling and simulation efforts are mainly restricted to simple analytical models [68], [78] and 2-D numerical simulation studies [79] and, for example, fall short of explaining the wide range of RTS amplitudes observed in otherwise identical devices [80]. There are suggestions that strategically located traps influence the magnitude and the spreading of RTS amplitudes due to surface potential fluctuations and channel nonuniformity [73], [74], [80]. However, such potential fluctuations have been mainly associated with oxide nonuniformity [78] and fixed and trapped interface charges [81]. Only recently has the impact of the random discrete dopants been considered [26].

The atomistic simulation approach described in the previous section has been applied to study the impact of a single trapped charge on the current in decananometer MOSFET when the random discrete dopant distribution in the channel is properly taken into account [26], [61]. The random dopant induced surface potential fluctuations result in current percolation through the "valleys" in the potential landscape. These dominate the current flow, particularly in weak inversion where the ionised acceptor charges are not screened by the electrons in the inversion layer. Trapping of electrons in defect states positioned along the dominant current percolation paths will produce RTS with large amplitudes.

The potential distribution in three 50×50 nm MOSFETs with discrete random dopants in the channel region is presented in Fig. 10. The devices are selected from a sample of 200 transistors with randomly generated dopant distributions to have the smallest, the largest and a typical threshold voltage in the distribution. The plane above the channel of each transistor maps the RTS amplitudes associated with the trapping of a single electron at the interface. Unlike the continuous doping simulations, the largest RTS amplitudes in this case are not in the middle of the channel but in the regions with the deepest valley in the potential landscape corresponding to the highest density of percolating current.

The drain current dependence of the maximum RTS amplitudes in the three transistors from Fig. 10 is compared in Fig. 11 with the corresponding dependence when continuous doping is used in the channel region and only trapped charge is simulated "atomistically." In weak inversion, the maximum RTS amplitudes in the discrete dopant simulations are always higher compared to the continuous doping simulations. The difference is more than three times for the discrete dopant MOSFET with the largest threshold voltage. Inspection shows that in the device with the lowest threshold voltage ($V_T = 0.49$ V), a lucky arrangement of dopants leaves almost half of the channel relatively low doped and highly conductive. The trapping of a single electron there has a less dramatic effect compared to the other
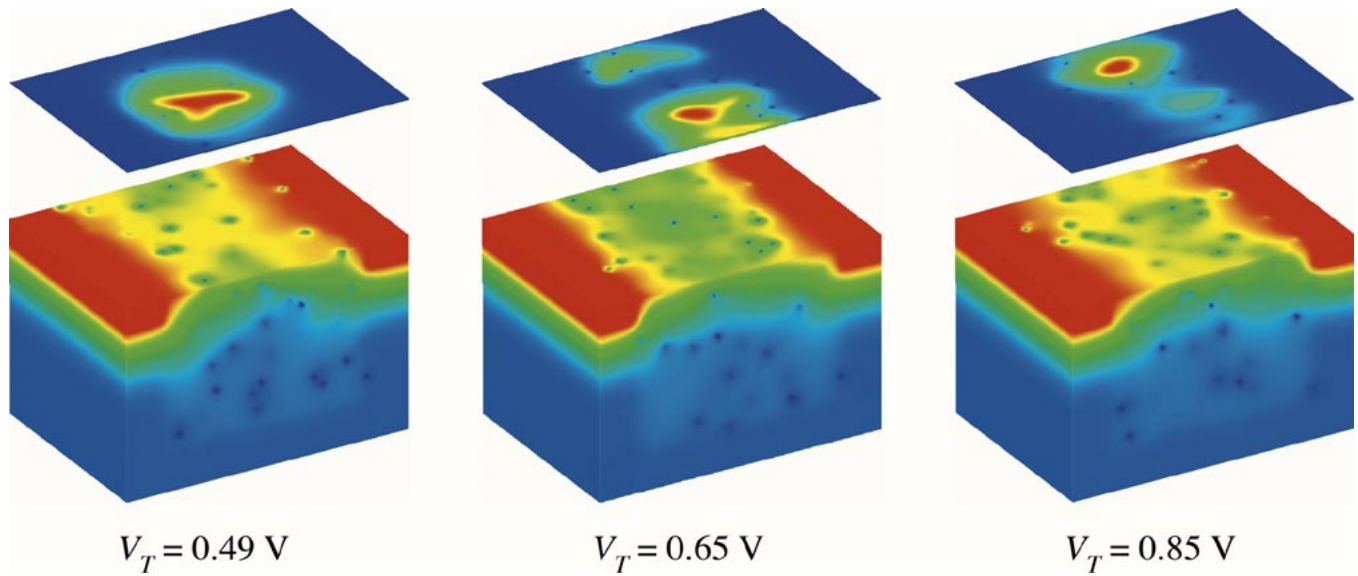
Fig. 10. Potential distribution in three 50×50 nm MOSFETs with discrete random dopants in the channel region. The positional dependence of the magnitude of the RTS amplitudes associated with the trapping of a single electron is mapped in the plane above each transistor.
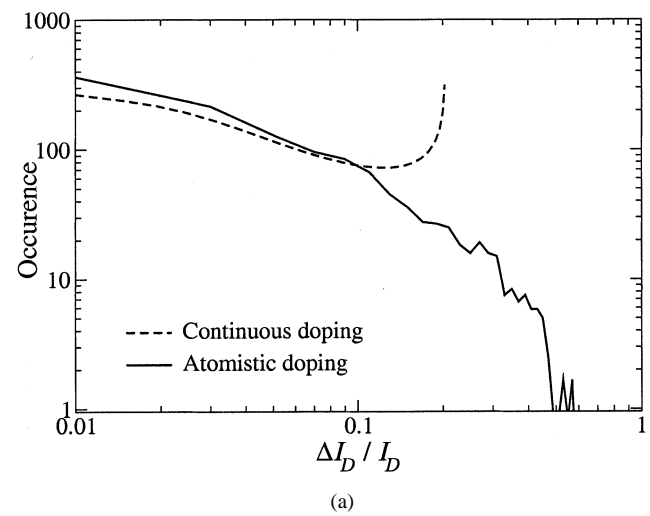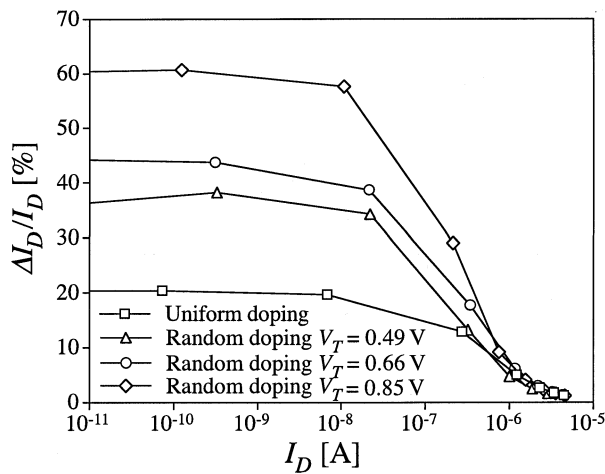

Fig. 11. Dependence of the maximum RTS amplitudes on the drain current for three 50×50 nm devices with different atomistic doping. The corresponding dependence obtained from continuous doping simulations is also presented.

simulated devices with discrete random dopants. The MOSFET with the largest threshold voltage ($V_T = 0.85$ V) has a large concentration of dopants in the middle of the channel, leaving very narrow paths for the percolating current. The trapping of a single electron in the vicinity of a dominant but narrow current channel has a strong effect on the overall current in this device.

The simulations using continuous and the discrete doping produce distinctly different distributions of the relative RTS amplitudes illustrated in Fig. 12(a). The continuous doping simulations result in a bimodal distribution with high density at both the smallest and the highest amplitudes. Such a distribution follows from the fact that in this case the trapping in the middle of the channel has strongest impact on the drain current, and the trapping in the regions adjacent to the source and drain has a minute effect. In the discrete dopant simulation the distribution has high density at the small amplitude end and a low-density tail at the high amplitude end, which is in good qualitative
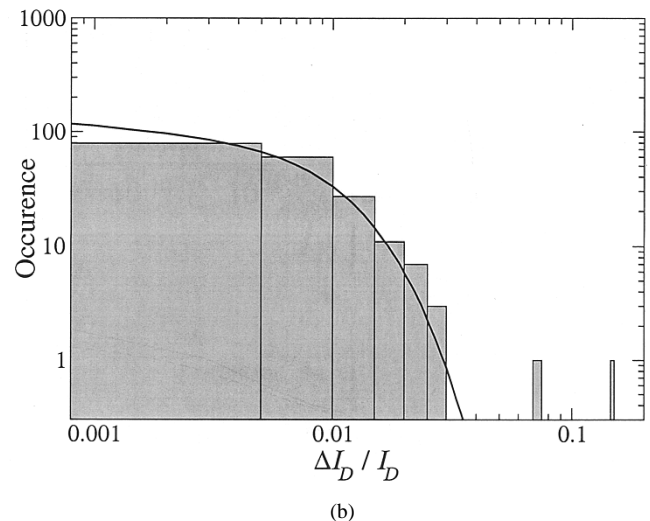

Fig. 12. Distribution of RTS amplitudes. (a) Obtained from the simulation of 50×50 nm MOSFETs with continuous doping and random discrete dopants. (b) Experimentally observed in 187 500×500 nm MOSFETs.
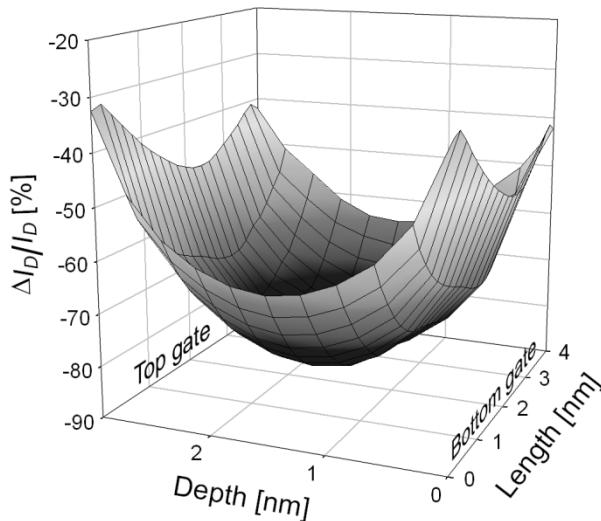
Fig. 13. Percentage change in current when a negative discrete charge is present at a particular location within the channel in a $4 \times 4 \times 3$ nm device. The maximum reduction in current is 84%.

agreement with the experimentally observed distribution obtained from 187 different 500×500 nm MOSFETs illustrated in Fig. 12(b) [81].

Even in an undoped channel, double-gate MOSFET, the unavoidable background doping introduces a finite probability of at least one ionised dopant (acceptor or donor) being present at a random location within the channel. In addition, if an electron or hole becomes trapped in a defect state at the interface or in the silicon body, it will introduce a fixed charge in the channel region [73]. These potential sources of localized single charge will have an electrostatic effect on the channel potential introducing, for example, in the case of acceptor or trapped electron in an n-channel double-gate MOSFET, a localized barrier to current flow, and a corresponding shift in the threshold voltage [76].

The change in the drain current at threshold as a function of the position of a single negative charge in the device (either acceptor or trapped electron) is mapped for the 4-nm double-gate MOSFET in Fig. 13. The mapping is done for a vertical cross section running through the middle of the channel from source to drain. Due to the quantum distribution, resulting in the majority of current flowing in the plane through the middle of the device, a charge trapped in the centre of the channel produces the largest effect. For the range of MOSFETs investigated here the maximum reduction in the current increases from 69% in the 10 nm device to 84% in the 4–nm one.

C. Oxide Thickness Fluctuations

The gate dielectric thickness in mass production MOSFETs has already reached the 1.5–nm barrier [1], [82] with sub 1–nm physical thickness utilized in the advanced research devices [5]. Atomic scale roughness of the Si/SiO$_2$ and gate/SiO$_2$ interfaces introduces significant intrinsic parameter fluctuations. Indeed when the oxide thickness is only a few silicon atomic layers the atomic scale interface roughness steps [83] will result in significant oxide thickness variations (OTVs) within the gate region of an individual MOSFET (see Fig. 2). The unique random pattern of the gate oxide thickness and interface landscape makes

each decananometer MOSFET different from its counterparts and leads to variations in the surface roughness limited mobility, gate tunnelling current [84], [85] and real [86] or apparent threshold voltage [87] from device to device.

In the same way as in the simulation of random dopant fluctuation effects [35], the numerical study of local oxide thickness fluctuation effects requires 3-D statistical simulations of ensembles of MOSFETs with macroscopically identical design parameters but with microscopically different oxide thickness and interface patterns. It is also important to include quantum mechanical confinement effects [88], which push the inversion layer away from the rough interface and smooth the spatial inversion charge variations [57] compared with classical simulations.

The random 2-D surfaces used to represent the boundary between the oxide and the silicon and/or between the oxide and the gate material in, to the best of our knowledge, the only 3-D simulation study of this kind [89] are constructed using standard assumptions for the autocorrelation function of the interface roughness. Generally, the interface is described by a Gaussian or exponential autocorrelation function with a given correlation length Λ and rms height Δ [90]. There is reasonably close agreement in the rms values Δ of the interface roughness reported by different sources but the reported values for the correlation length Λ vary by more than an order of magnitude. Correlation lengths in the range of 1–3 nm are reported from TEM measurements [90] and are typically used in Monte Carlo simulations and to fit surface roughness limited mobility to experimental data [91]. At the same time, the values of Λ reported from AFM measurements vary from 10–30 nm [92]. Random 2D surfaces are generated from the corresponding power spectra using a standard 2D Fourier synthesis approach [93]. The "analog" random surface is then quantised in steps to take into account the discrete nature of the interface roughness steps associated with the atomic layers in the crystalline silicon substrate [83]. The step height is approximately 0.3 nm for the (001) interface.

A typical random Si-SiO$_2$ interface, generated according to the above described procedure and used in the simulation of a 30×30 nm MOSFET with average oxide thickness $\langle t_{ox} \rangle = 1.05$ nm and continuous channel doping concentration $N_A = 5 \times 10^{18}$ cm^{-3} is shown at the top of Fig. 14. The interface has been reconstructed using the power spectrum for a Gaussian autocorrelation function. Only the roughness of the Si/SiO$_2$ interface was introduced in the simulations and the gate-SiO$_2$ interface was flat. The potential distribution at threshold voltage is shown at the bottom of the same figure. The oxide thickness fluctuations introduce surface potential fluctuations similar to the fluctuations introduced by random impurities. DG quantum corrections are included in the simulation. One equiconcentration surface corresponding to electron charge density 1×10^{17} cm^{-3} is plotted in the middle, illustrating the quantum confinement effects in both vertical and lateral directions.

The dependence of the threshold voltage standard deviation σV_T on the correlation length Λ obtained from classical and DG simulations of the device in Fig. 14 is compared in Fig. 15. The introduction of quantum corrections results in an increase in the threshold voltage variation. We believe that this is related
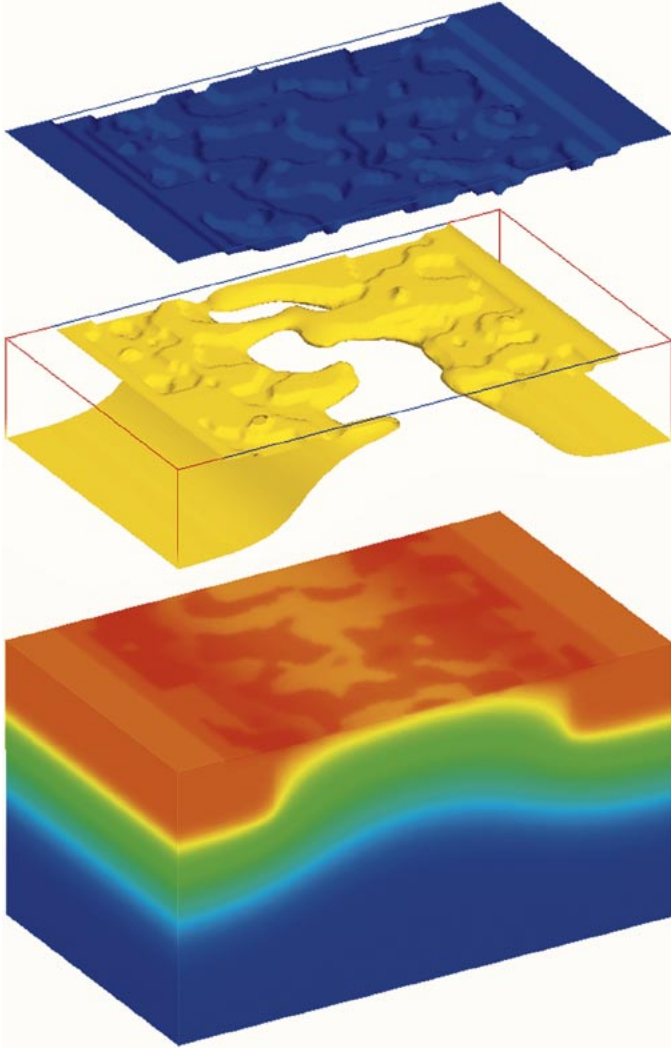
Fig. 15. Dependence of the threshold voltage standard deviation σV_T on the correlation length Λ for the 30×30 nm MOSFETs as in Fig. 14. Classical and DG simulation results are compared.

Fig. 16. Comparison of the doping concentration dependence of standard deviation of the threshold voltage introduced by oxide thickness variation (OTV) and by doping fluctuations (DF) for a 30×30 nm MOSFET.

Fig. 14. (Top) Typical profile of the random Si-SiO$_2$ interface in a 30×30 nm MOSFET. (Middle) Equiconcentration contour obtained from DG simulations. (Bottom) Potential distribution.

to the lateral confinement effects, which narrow the current percolation paths. In both cases the dependence of σV_T on Λ is linear for correlation lengths much smaller than the characteristic MOSFET dimensions and saturates for large Λ. The dependence of the kurtosis (in [94, Eq. 26.1.16]) of the threshold voltage distribution as a function of Λ in the DG case is presented as an inset in the same figure. The increasingly negative values of the kurtosis are an indication of the flattening of the σV_T distribution with the increase in correlation length. For devices with characteristic dimension below 30 nm, the oxide thickness induced threshold voltage fluctuations become comparable with the fluctuations induced by random discrete dopants, particularly when the contribution of the both interfaces is taken into account, and the larger correlation length suggested by AFM measurements are adopted.

A comparison is made in Fig. 16 between the doping concentration dependences of standard deviation in the threshold voltage induced by oxide thickness variation $\sigma V_T^{\mathrm{OTV}}$ and the standard deviation in the threshold voltage induced by dopant fluctuations σV_T^{DF}. In order to isolate the doping fluctuation effects, simulations were carried out first using random dis-
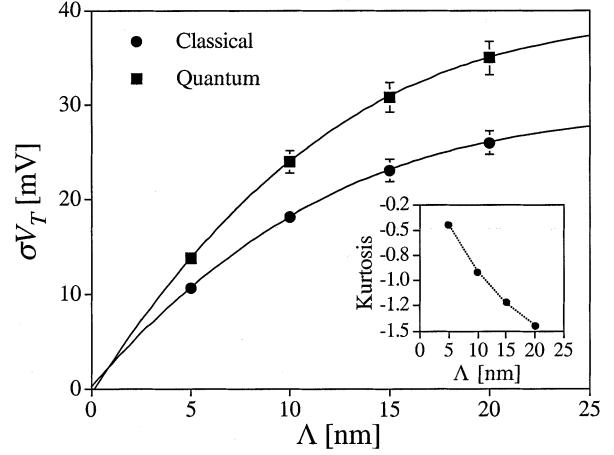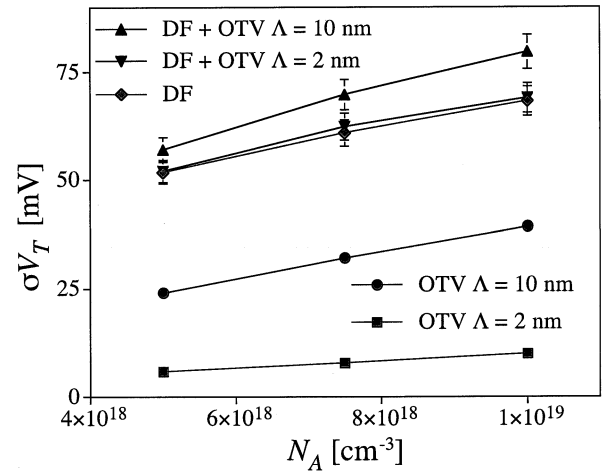
crete dopants and uniform gate oxide. The corresponding σV_T^{DF} is approximately two times larger than $\sigma V_T^{\mathrm{OTV}}$ for correlation length $\Lambda = 10$ nm and more than five times larger for $\Lambda = 2$ nm. However, with the increase in the doping concentration, the gap between σV_T^{DF} and $\sigma V_T^{\mathrm{OTV}}$ reduces. Finally, simulations were carried out in which the oxide thickness variation and the dopant fluctuations are taken into account simultaneously. The close inspection of the results reveals that the two sources of intrinsic parameter fluctuations act in a statistically independent manner resulting in a total standard deviation σV_T^{tot} that closely follows the relationship $\sigma V_T^{tot} = \sqrt{(\sigma V_T^{\mathrm{OTV}})^2 + (\sigma V_T^{\mathrm{DF}})^2}$.

D. Line Edge Roughness

The line edge roughness (LER) caused by tolerances inherent to materials and tools used in the lithography processes is yet another source of intrinsic parameter fluctuations [95], [96], which needs close attention. LER has caused little worry in the past since the critical dimensions of MOSFETs were orders of magnitude larger than the roughness. However, as the aggressive scaling continues into the decananometer regime, LER does not
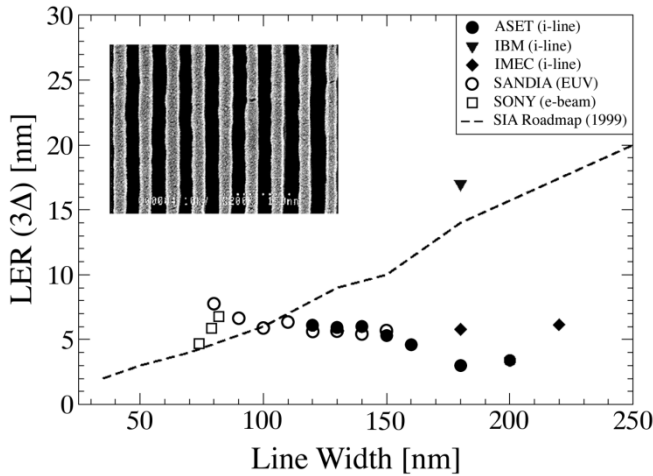
Fig. 17. LER found in advanced lithography processes by various labs and required by the SIA roadmap The inset shows LER found in sub-100 nm e-beam generated lines.

Fig. 18. Potential distribution at threshold in a well scaled 30×30 nm MOSFET with line edge roughness of the gate of $3\Delta = 6$ nm.

scale accordingly, becoming an increasingly larger fraction of the gate length. As shown in Fig. 17, the edge roughness remains typically on the order of 5 nm almost independently of the type of lithography used in production or research [6], [9], [95], [97]–[100]. Although attempts have been made to simulate analytically the impact of the gate edge roughness on leakage [101], they rely on fitting parameters and lack predictive power due to the complex 3-D nature of the problem. Previous efforts to numerically model edge roughness effects were limited in terms of realism and sophistication due to the massive computational resources needed to perform statistical simulations on realistic 3-D geometries. Pioneering 3D simulation studies treated the problem deterministically using a "square wave" approximation for the gate edge [102], [103]. The simplified statistical approach adopted in [95], [104], [105] is based on 2-D simulations of samples of MOSFETs with statistical variations in the channel length but fixed channel width. The attempt to validate this approach using 3-D simulations reveals more than 30% discrepancy in the 3σ estimates of the off-current [95], which is most sensitive to multidimensional short channel effects.

As a natural extension to the statistical 3-D simulations methodology, the simulation of LER in decananometer MOSFETs was approached in a coherent statistical fashion in [96], [106]. The LER in the simulations is specified by rms amplitude Δ and correlation length Λ. This allows both 3-D and statistical aspects of LER to be naturally incorporated in a single simulation framework. The reconstruction of realistic gate edges is based on a 1-D Fourier synthesis approach, similar to that used in the generation of the Si-SiO$_2$ interface. A typical 30×30 nm MOSFET with continuous doping and LER is shown in Fig. 18 for $\Lambda = 10$ nm and LER with $3\Delta = 6$ nm.

Similarly to random discrete dopants [26], [51], random LER introduces threshold voltage fluctuations in devices with otherwise identical design parameters even when continuous doping is used in the simulations. For given device dimensions the standard deviation in threshold voltage due to LER increases when Δ or Λ are increased. The former dependence is illustrated in Fig. 19 for 30×50 and 50×50 nm MOSFETs with oxide
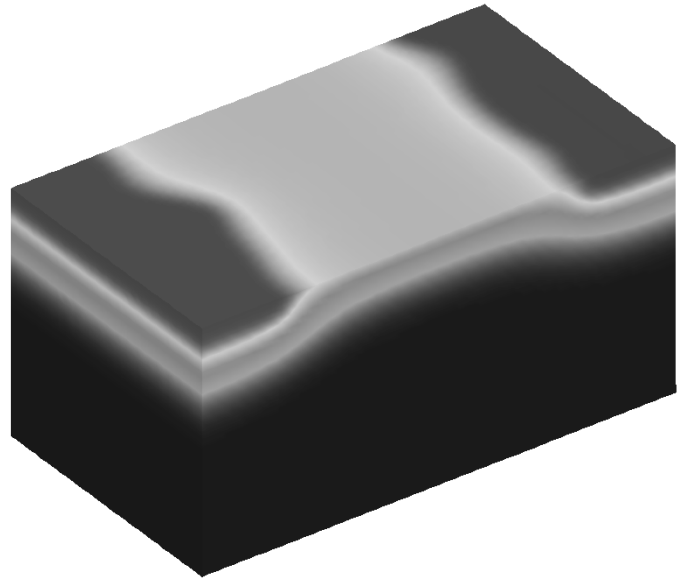

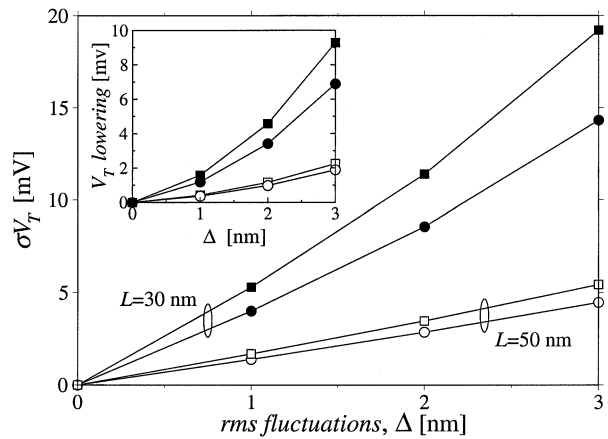
Fig. 19. Threshold voltage fluctuations associated with LER as a function of the rms amplitude Δ.

thickness $t_{ox} = 1.3$ nm and continuous channel doping concentration $N_A = 5 \times 10^{18}$ cm^{-3}, assuming LER correlation length $\Lambda = 20$ nm. In addition, similarly to the atomistic simulations [26], [51], the introduction of LER results in threshold voltage lowering compared with the threshold voltage V_{T0} of the corresponding generic device with straight gate edges. The inset in Fig. 19 shows the average threshold voltage lowering $\langle V_T \rangle - V_{T0}$. The threshold voltage fluctuations increase with the increase in the drain voltage. For given LER parameters both the threshold voltage fluctuations and lowering increase as gate dimensions are reduced. Moreover, the fluctuations are comparable in magnitude to those resulting from random dopants in similar 30–nm devices [26].

Simulations with both random discrete dopants and LER were carried out in [106] in order to understand the simultaneous effect of these two sources of intrinsic parameter fluctuations. Fig. 20 displays the standard deviation in the logarithm of the off current $\sigma \log(I_{off})$ for a set of MOSFETs with channel width 50 nm and channel lengths varying from
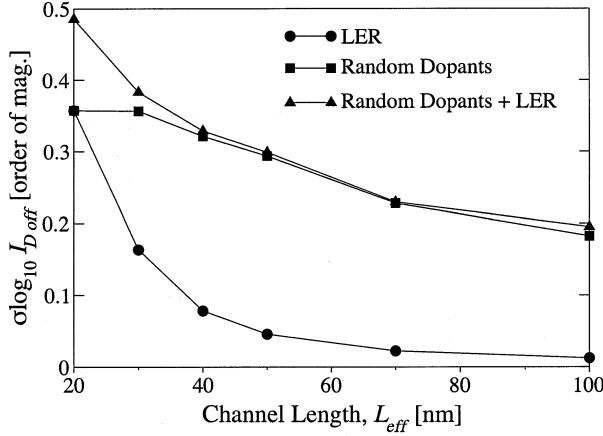
Fig. 20. Dependence of $\sigma \log(I_{off})$ on the channel length for a set of MOSFETs with channel width 50 nm. The LER parameters used to define the gate edges are $\Lambda = 20$ nm and $\Delta = 2$ nm.
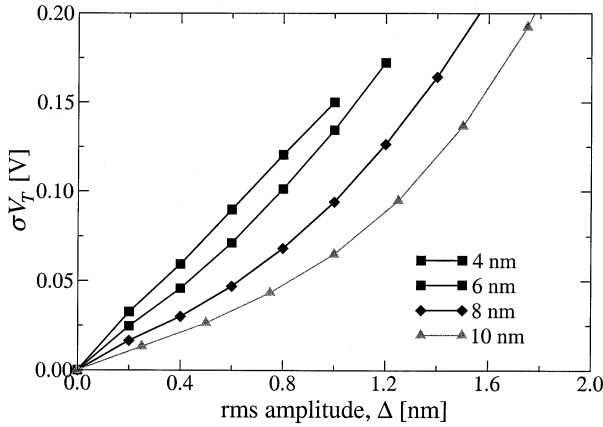

Fig. 21. Standard deviation in threshold voltage, σV_T, due to LER with rms amplitude Δ for double gate MOSFETs with different channel lengths.

TABLE I
DIMENSIONS OF THE DOUBLE GATE MOSFETs USED IN THE SIMULATIONS
PRESENTED IN FIG. 21, SCALING FROM A 10 nm CHANNEL LENGTH
DOWN TO 4 nm

Channel length [nm]	Channel width [nm]	Silicon body thickness, t_{Si} [nm]	Oxide thickness, t_{ox} [nm]
10	10	4.0	1.0
8	8	3.7	0.8
6	6	3.3	0.6
4	4	3.0	0.4

tuations are still of a significant magnitude, with V_T covering a range of approximately ± 0.15 V for the 4-nm device.

IV. CHALLENGES AHEAD

In any simulation, the accuracy is only as good as the description of the simulation domain and the complexity of various physical models in use. Hence, predictive atomistic process simulators should be natural companions to further attempts in atomistic device modeling, providing atomic scale information for the device structures. One of the main challenges in studying decananometer devices therefore lies in interfacing the atomistic device modeling tools with predictive atomistic process simulations, resulting in a more reliable description of the problem at hand.

Based on the same philosophy, improvements to the physical models employed in the transport problem are also required. For instance, higher moments of the Boltzmann transport equation such as hydrodynamic models may be incorporated in the atomistic simulations to account correctly for nonequilibrium conditions in decananometer devices. Particle simulations may be especially useful to uncover effects related to the discrete nature of carriers and noise, which would affect the device performance at an atomistic level, and to resolve *ab initio* long-range electrostatic effects, carrier-carrier, and carrier-impurity interactions. A more elaborate or exact treatment of quantum effects has not yet been included in our simulations. For example, tunnelling through the gate oxide can result in additional gate leakage and threshold voltage fluctuations. At present, the trade off is between the efficiency of numerical simulations and the range of applicability in quantum mechanical simulation strategies.

The increased understanding of different components of fluctuations in device characteristics points to a growing need to develop new device architectures that can suppress them. Several novel device concepts such as double gate MOSFETs or SiGe heterojunction MOSFETs must be simulated to assess their susceptibility to atomistic processes. Ultimately, the device performance is affected by the interplay of many different sources of fluctuations discussed within this paper. Thus, the correlation between the contributions of different components of fluctuations should be investigated in atomistic simulations by concurrently incorporating different processes in a single device. In doing so, any other processes which are relevant to the decananometer regime but have not been treated fully here must also be included. There is indeed a challenging future for device simulation.

20 to 100 nm. Three sets of results representing i) rough gate edges with continuous doping, ii) straight gate edges with random discrete dopants, and iii) rough gate edges with random discrete dopants are depicted. The LER parameters used to define the gate edges $\Lambda = 20$ nm and $\Lambda = 2$ nm are typical for the advanced lithography techniques today. It is clear that within the margins of the statistical error the two sources of intrinsic parameter fluctuations, LER, and random dopants might be considered statistically independent, particularly for channel lengths larger than 30 nm. The standard deviation in the simulations combining the two sources σ_{TOT}, closely follows the relation $\sigma_{TOT} = \sqrt{\sigma_{LER}^2 + \sigma_{RD}^2}$, where σ_{LER} and σ_{RD} are the standard deviations when LER and random dopants are considered independently in the simulations.

Nanometer scale, double gate MOSFETs will be extremely sensitive to LER. The dependence of the standard deviation in the threshold voltage on the rms amplitude Δ is illustrated in Fig. 21 for a set of double gate MOSFETs with dimensions given in Table I, using $\Lambda = 5$ nm [67]. As one would expect, the fluctuations increase as Δ increases. It is clear that LER must be drastically reduced from its current level if devices below 10 nm are to be of practical use near the end of the Roadmap. Even if Roadmap requirements are met (i.e. $\Delta \approx 0.3$ nm), the fluc-

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