A CMOS LNA Using a Harmonic Rejection Technique to Enhance Its Linearity

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***Abstract*—In this study, we design a differential low-noise amplifier (LNA) using a 0.18-μm RF CMOS process. To improve its linearity, we propose a harmonic rejection technique using RC feedback at the gain stage. The third harmonic component of the drain node of the common-gate transistor is fed back to the source node of the common-gate transistor to restrict the generation of the third harmonic component at the output of the LNA. To verify the feasibility of the proposed technique for a linear amplifier, we designed a typical LNA and the proposed LNA in an identical process and with the same design parameters apart from the feedback loop of the proposed LNA. The measured improvement of the input-referred P1 dB of the proposed LNA is approximately 3 dB compared to that of the typical LNA. From these measured results, we successfully prove the feasibility of the proposed linearization technique.**

***Index Terms*—Differential, feedback, harmonic rejection, linearity, third harmonic.**

I. Introduction

THE low-noise amplifier (LNA) finds many uses owing to its essential functions for wireless communication systems. In particular, LNAs designed to use CMOS technology have become more popular due to their low unit cost and easy integration with other circuit blocks [1]–[4]. However, CMOS technology presents various obstacles in the design of RF amplifiers, thwarting efforts to achieve good performance compared to RF amplifiers designed using III-V compound semiconductors. For example, given that there is no through-via hole in the CMOS process, a gain-reduction problem arises due to the parasitic inductance of the bond wires. Additionally, the linearity of the CMOS process itself is worse than that with a compound semiconductor, which makes it challenging to design a CMOS amplifier with high linearity [5], [6]. Fortunately, the gain-reduction problems induced by the parasitic inductance can be resolved by adapting a differential structure and hence generating virtual ground (GND) nodes in the CMOS circuits. However, a technique to improve the linearity of CMOS needs to be sought consistently for the satisfactory performance of a CMOS amplifier compared to that of a compound semiconductor. In this study, we propose a harmonic rejection technique using a feedback loop at the gain stage to enhance the linearity of CMOS amplifiers.

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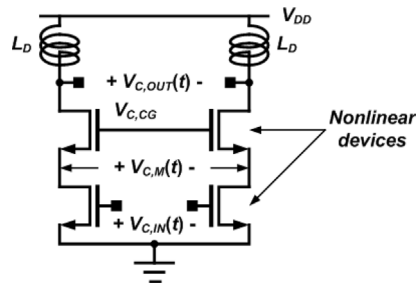

Fig. 1. Typical differential amplifier in the differential mode of operation.

II. Proposed Harmonic Rejection Technique Using a Feedback Loop

To enhance the linearity of the amplifier, the harmonic components at the nodes of the amplifier need to be suppressed. If we first consider the second harmonic component in the differential amplifiers, by virtue of the benefit of the differential structure, the second harmonic component may be suppressed at the input and output baluns and at the virtual ground nodes. Thus, we focus here on the rejection of the third harmonic component for a CMOS amplifier designed using a differential structure. The second harmonic component is ignored to simplify the analysis. The node voltages of the typical CMOS amplifier shown in Fig. 1 can therefore be calculated as follows:

$$\begin{aligned} V_{C,IN}(t) &= A\cos(\omega t) \\ V_{C,M}(t) &= \alpha_1 V_{C,IN}(t) + \alpha_2 V_{C,IN}^2(t) + \alpha_3 V_{C,IN}^3(t) + \cdots \\ &\approx \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)\cos(\omega t) + \frac{\alpha_3 A^3}{4}\cos(3\omega t) \\ V_{C,OUT}(t) &= \beta_1 V_{C,M}(t) + \beta_2 V_{C,M}^2(t) + \beta_3 V_{C,M}^3(t) + \cdots \end{aligned} \quad (1)$$

Here, we assume that the amplifier is fully differential and that the even-order harmonics generated from α_i and β_i with an even i do not exist. From (1), the third harmonic term of $V_{C,OUT}(t)$ can be calculated as follows:

$$V_{C,OUT}(t)\Big|_{3^{rd}} = \frac{\beta_3}{4}\left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)^3 + \beta_1\left(\frac{\alpha_3 A^3}{4}\right) + \frac{3}{4}\beta_3\left(\frac{\alpha_3 A^3}{4}\right)^3. \quad (2)$$

In general, given that $\alpha_1 A + (3\alpha_3 A^3)/4$ and β_1 are higher than $(3\alpha_3 A^3)/4$ and β_3, respectively, to guarantee the linear

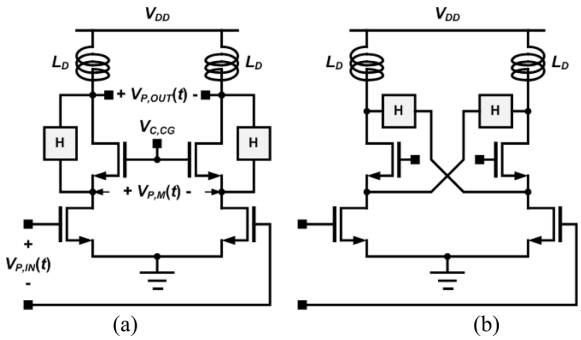

Fig. 2. Proposed harmonic rejection techniques (a) with a simple feedback loop and (b) with a cross-coupled feedback loop.

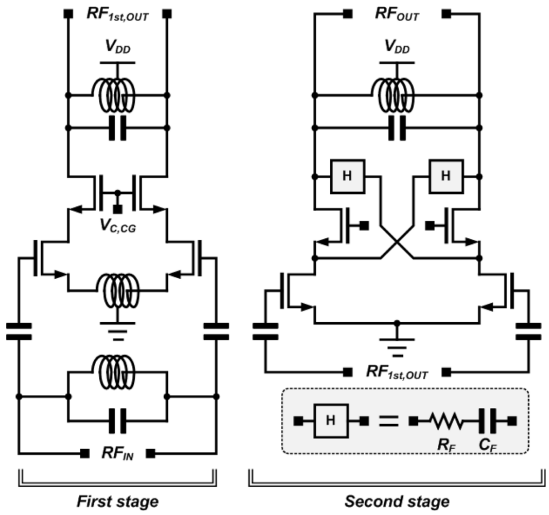

Fig. 3. Simple schematic of the proposed LNA.

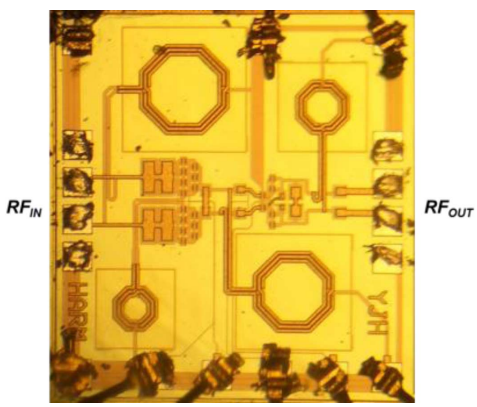

Fig. 4. Photograph of the designed LNA.

operation of the amplifier, (2) can be simplified as follows:

$$V_{C,OUT}(t)\Big|_{3^{rd}Harmonic} \approx \frac{\beta_3}{4}\left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)^3 + \beta_1\left(\frac{\alpha_3 A^3}{4}\right). \quad (3)$$

In this work, we proposed a harmonic rejection technique using a feedback loop to suppress the third harmonic of (3). A conceptual diagram of the proposed harmonic rejection technique is provided in Fig. 2. As shown in Fig. 2(a), we use feedback of which the transfer function is $H(\omega)$ between the drain

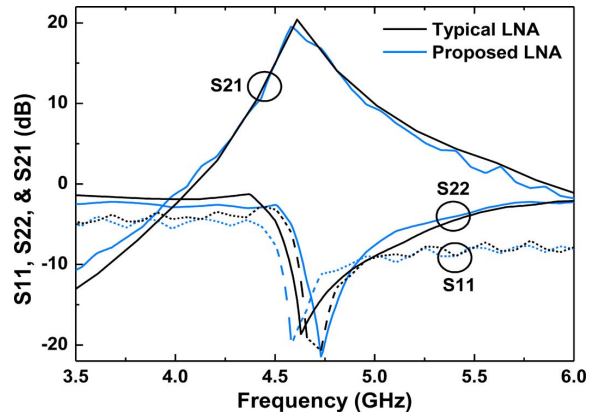

Fig. 5. Measured s-parameters of the proposed LNA.

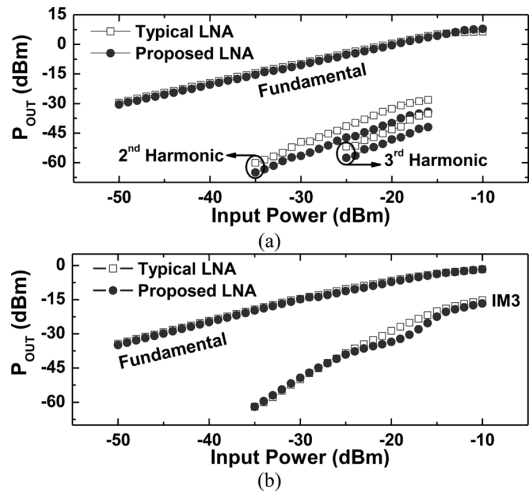

Fig. 6. Measured output power according to the input power: (a) single-tone test and (b) two-tone test.

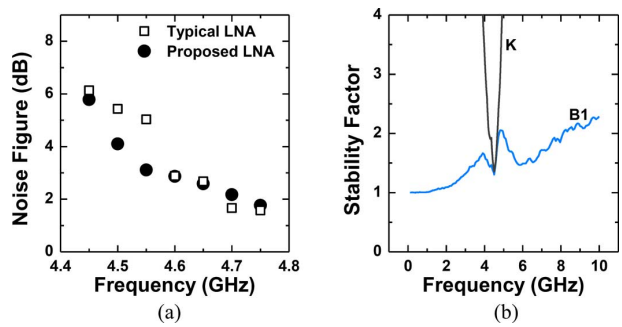

Fig. 7. Measured results: (a) noise figure and (b) stability factor.

and source node of the common-gate transistor. The third harmonic component of $V_{P,OUT}$ can then be calculated as follows:

$$V_{P,OUT}(t)\Big|_{3^{rd}} \approx \frac{V_{C,OUT}(t)\Big|_{3^{rd}}}{1-\beta_1 H} \approx \frac{1}{1-\beta_1 H}\left[\frac{\beta_3}{4}\left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)^3 + \beta_1\left(\frac{\alpha_3 A^3}{4}\right)\right]. \quad (4)$$

Here, we assume that the magnitude of $H(\omega)$ is zero for the fundamental frequency and that β_1 is much larger than β_3. From (4), to ensure that the third harmonic of $V_{P,OUT}(t)$ is lower than that of $V_{C,OUT}(t)$, the $(1-\beta_1 H)$ term of (4) must be higher than β_1. Accordingly, the polarity of the magnitude of $H(\omega)$

TABLE I
COMPARISON OF DIFFERENTIAL CMOS LNAS

.	[7]	[8]	[9]	This work (Typical)	This work (Proposed)
Stage	1	1	1	2	2
Freq.(f_c) [GHz]	5.7	5.25	5.0	4.6	4.6
Tech. [nm]	180	250	180**	180	180
Supply [V]	1.8	3	1.5	1.2	1.2
NF [dB]	3.7	2.5	0.95	2.87	2.87
Gain [dB]	12.5	16	11	20	19
P1dB* [dBm]	-11	-11	-7	-14	-11
IIP3 [dBm]	-0.45	-1.5	5	1	4
P_{DC} [mW]	14.4	24	12	22.8	22.9
BW [GHz]	-	-	-	0.15	0.22
FoM	1.12	1.21	19.11	2.71	4.82

* Input-referred P1dB, ** SOI CMOS technology

for the third harmonic component must be negative. For negative polarity of $H(\omega)$ without additional circuit components, we reconstruct the circuit shown in Fig. 2(a) into the circuit shown in Fig. 2(b). By cross-coupling through $H(\omega)$, as shown in Fig. 2(b), we easily ensure that $H(\omega)$ has negative polarity, thus suppressing the third harmonic component at the output node of the differential amplifier.

III. DESIGN OF A LNA USING THE PROPOSED HARMONIC REJECTION TECHNIQUE

To verify the feasibility of the proposed harmonic rejection technique, we designed a 5 GHz LNA in the 0.18 μm RF CMOS process. Fig. 3 shows a simplified schematic of the designed LNA, where some of the bias circuits are omitted. The first stages of the designed LNA are designed using a noise-matching technique with inductive source-degeneration, as shown in Fig. 3. The harmonic rejection technique is adapted to the second stage of the LNA. The R_F and C_F components shown in Fig. 3 constitute the feedback loop. The value of R_F determines the strength of the feedback signal. C_F acts as a dc blocking device and restricts the fundamental components from entering into a feedback loop.

We also designed a typical LNA. All of the design parameters of the LNAs are identical to each other except for C_M and the feedback loop, $H(\omega)$. To ensure an identical operating frequency of the typical and the proposed LNA, the designed values of C_M are 620 fF and 450 fF for the typical and the proposed LNA, respectively. The R_F and the C_F values in Fig. 3 are 200 Ω and 70 fF, respectively. Although we assume that the magnitude of $H(\omega)$ is zero for the fundamental frequency in (4), the magnitude is in fact approximately 1/35.

IV. MEASUREMENT RESULTS

Fig. 4 shows a photograph of the LNA using the proposed harmonic rejection technique. The chip size of the LNA is 980 $\times$ 910 μm^2. The measured results are obtained using an on-wafer test with a GSSG probe tip. Fig. 5 shows the measured s-parameters of the proposed LNA. We obtained a maximum gain of 19 dBm at an operating frequency of 4.6 GHz. Fig. 6 shows the measured fundamental and third harmonics of the proposed and typical LNAs according to the input power. As shown in Fig. 6, the third harmonic of the proposed LNA is lower than that of the typical LNA by approximately 3 dB. The gain of the fundamental frequency is degraded by 1 dB compared to that of the typical LNA. We determined that the undesired feedback of the fundamental component degrades the gain of the proposed LNA. We find that the proposed feedback loop to reduce third harmonic does not cause instability. The measured noise figures of the typical and proposed LNAs are shown in Fig. 7(a). Fig. 7(b) shows the measured stability factor of the proposed LNA. The measured performances of the typical and proposed LNAs are summarized in Table I [7], [8]. Here, the figure of merit (FoM) is calculated as follows [9]:

$$FoM = \frac{Gain[abs.] \cdot IIP3[mW] \cdot fc[GHz]}{(NF-1)[abs.] \cdot P_{DC}[mW]}. \quad (5)$$

V. CONCLUSION

In this study, we proposed a harmonic rejection technique using RC feedback for a differential CMOS amplifier. The third harmonic component of the drain node of the common-gate transistor is fed back to the drain of the common-source transistor to restrict the generation of the third harmonic component at the output of the LNA. The feedback of the fundamental component is minimized using the values of a resistor and a capacitor, which constitute the feedback loop. To verify the feasibility of the proposed technique for a linear amplifier, we designed a typical LNA and the proposed LNA in an identical process and with the same design parameters except for the feedback loop of the proposed LNA. The experimental results successfully demonstrate the feasibility of the proposed technique. Although the proposed technique is demonstrated by designing what can be considered a pseudo-differential LNA, it will work for a differential LNA as well.

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