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CNTFET Technology for RF Applications: Review and Future Perspective

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ABSTRACT RF CNTFETs are one of the most promising devices for surpassing incumbent RF-CMOS technology in the near future. Experimental proof of concept that outperformed Si CMOS at the 130 nm technology has already been achieved with a vast potential for improvements. This review compiles and compares the different CNT integration technologies, the achieved RF results as well as demonstrated RF circuits. Moreover, it suggests approaches to enhance the RF performance of CNTFETs further to allow more profound CNTFET based systems e.g., on flexible substrates, highly dense 3D stacks, heterogeneously combined with incumbent technologies or an all-CNT system on a chip.

INDEX TERMS Carbon nanotubes, CNTFET, radio frequency, cut-off frequency, maximum oscillation frequencies, linearity, RF circuits, compact modelling.

I. INTRODUCTION

Among the many emerging technologies being investigated for extending the life of CMOS technology, single-walled carbon nanotube (CNT) field-effect transistors (FETs) have become one of the frontrunners. This is attributed to the superior material properties of CNTs. E.g., compared to graphene, the reasonable bandgap of CNTs enables the realization of transistors having much lower leakage current and much higher radio-frequency (RF) power gain. CNTs exhibit a much higher carrier mobility than 2D transition metal dichalcogenide materials (such as MoS_2), thus allowing to build transistors with much higher operating frequencies and current drive capability. Compared to incumbent bulk material (such as silicon and In(Ga)As), the saturation velocity is at least a factor two higher and scattering is exclusively limited to $\pm 180°$, resulting in a higher current carrying capability (e.g., [1], [2]), temperature stability and electrothermal ruggedness [3] as well as in lower power dissipation and thermal noise [4]. Furthermore, CNTs enable to easily build chemical, biological and irradiation (e.g., THz) sensors with superior detectivity (e.g., [5], [6]). Metallic CNTs allow realizing interconnects [7], [8], and the low-mass and high mechanical stability of CNTs enables micro-electromechanical devices with much higher frequency than with incumbent materials [9].

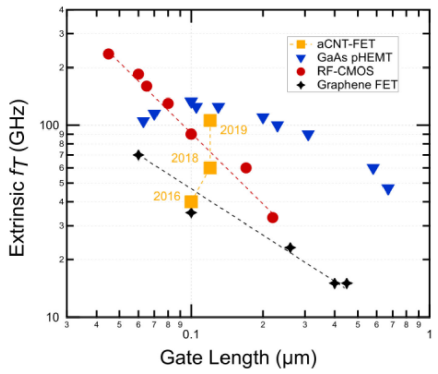

FIGURE 1. Progression of CNTFET technology achieved by Carbonics Inc. in terms of extrinsic transit frequency is closing the gap with the incumbent FET technologies [12].

The combination of all these features offered by the same material induces the vision of an all-CNT system-on-a-chip (SOC), powered possibly by on-chip CNT or graphene based supercapacitors.

Many of the functionalities listed above have already been demonstrated stand-alone, but not necessarily with the required performance, making the all-CNT SOC rather a long-term vision. So far, the major focus of CNTFET related research has been on applications for chemical sensors and digital electronics (e.g., [10], [11]). Since channel formation can be a cold process and due to the thermal ruggedness of CNTs, stacking CNTFET layers is considered as a major advantage over conventional materials. Thus, increasing the packing density has driven the effort of building CNTFET based microprocessors [11]. Other features of the all-CNT SOC, such as integrated circuits (ICs) with CNTFETs for RF applications have not been realized so far due to the lack of a suitable back-end-of-line (BEOL) for RF passives. However, experimental results of the latest 110 nm CNTFETs from Carbonics Inc. achieve, averaged over 107 devices, extrinsic unity current gain cut-off frequencies of about 80 GHz (cf. Fig. 1) and slightly over 100 GHz for "hero" devices [12]. These results are now in the same range as the 90 GHz for 130 nm CMOS, despite the just 50 CNTs per μm channel width and an average current of about 5 μA per tube. Both values are still far below the theoretically achievable density of about 600 CNTs per μm (at 1.5 nm diameter) and the already measured drain current of more than 20 μA per tube [1], [13], [14]. Considering this recent progress, one can now safely expect the HF (high-frequency) performance of CNTFETs to significantly exceed that of RF-CMOS (for a given lithography node) in near future, making a near-term entry in the low-GHz RF market more probable than the realization of competitive large-scale digital circuits.

This paper provides an overview on the present status of CNTFETs for RF applications. Starting in Section II, the process technology for building multi-tube RF CNTFETs is described, followed by selected electrical results. Existing modeling approaches and tools are discussed in Section IV. Section V gives an overview on RF circuits built so far, ending with a simulation based performance comparison to 130 nm RF-CMOS using the same RF passives. Finally, future development and obstacles to be overcome are discussed.

II. DEVICE TECHNOLOGY

Over a decade ago, the theoretical and experimental single nanotube device work had laid the foundation that CNTFET technology would possess remarkable electrical transport properties. However, realizing this in practical multitube devices for RF applications would require material advances largely related to overcoming the engineering challenges of *i*) obtaining high purity semiconducting CNTs and eliminating their metallic counterparts and other impurities (high output conductance), *ii*) assembling those CNTs into dense aligned arrays (high currents), and *iii*) achieving low contact resistance [15]. An important figure of merit for evaluating the RF device performance is the extrinsic unity current gain cut-off frequency f_T, which is approximately given by [15]

$$f_{\mathrm{T}} = f_{\mathrm{T,intrinsic}} \left(\frac{1}{1 + \frac{C_{\mathrm{w}}}{C_{\mathrm{gg1}}} d} \right) \tag{1}$$

where $f_{T,\mathrm{intrinsic}}$ is the transit frequency without any parasitic capacitances, $C_{gg,1}$ is the gate capacitance of an individual CNT, d is the average pitch between nanotubes, and C_w is the parasitic capacitance per gate width. Recently, huge progress has been made overcoming the above mentioned challenges allowing the underlying intrinsic CNT properties to materially manifest more. This has pushed f_{T} results for CNTFETs to within par with incumbent RF-CMOS technologies as shown in Fig. 1.

Presently, there are two main approaches towards developing wafer-scale CNTFET technology. The first approach is to use post-processed CNTs. In this method, CNTs obtained from bulk growth are then separated in solutions according to their electronic type. The separating techniques employed are density gradient ultracentrifugation, dielectrophoresis separation, polymer wrapping, gel-chromatography, and others [16]. While all approaches enrich the semiconducting content only polymer wrapping and gel chromatography possess the potential to separate CNT material on a large scale. This solution based CNT processing generated enthusiasm about high purity semiconducting CNTs above 99.9%. However, the post-processed CNTs normally possess an enhanced level of structural defects induced from the purification and dispersion processes [17]. Moreover, their surface and potentially interior as well is wrapped with surfactant or polymer which can be challenging to remove. These issues have inspired an alternative CNT synthesis and integration approach, which is to directly grow CNTs on a Silicon (Si) substrate by a catalytic Chemical Vapor Deposition (CVD) method. CVD grown CNTs have been shown to exhibit superior material quality for single tube devices. They can carry higher current and deliver higher gain (g_m) [18], [19]. Also, CVD growth allows control to synthesize CNT *in-situ* by controlling

the catalyst deposition sites [13], [20]. In addition, the as demonstrated CVD approach is fundamentally and practically suitable for commercial-grade manufacturing of 4″ and even larger wafers. Aligned nanotubes are realized via directed gas flow [21]–[25], applied electric fields [26], [27] and interactions with the substrate. In particular, CVD fabricated CNT arrays on single-crystal substrates like quartz or sapphire [28]–[38] were considered as ideal type of CNT materials for RF FETs because of high-quality (high density, alignment and clean surface). Typically, carbon nanotubes with length of over 100 μm, linear density of 10–100 tubes/μm and alignment angle less than 0.01° could be achieved.

The main challenge of the CVD growth method to date is the yield of semiconducting CNTs and the high thermal load on the substrate during synthesis. The high amount of metallic CNTs mainly reduces the on/off ratio and the output resistance and thus the power gain for a given frequency of operation. Many attempts to selectively remove the metallic nanotubes from the semiconducting ones have been developed. Various gas-phase or plasma-etching approaches [39], [40], selective electrical breakdown of metallic CNTs [41], microwave/laser radiation based approaches [42]–[44] or nanoscale thermo-capillary flows [45]–[49] have been exploited to enhance the semiconducting CNT content.

Although the on/off ratio could be improved to 10^4, these selective etching approaches induce other effects, such as mobility degradation, breakdown residuals in the channel resulting in enhanced parasitic capacitances, device to device variation and additional processing effort.

Regarding semiconducting type-enhanced CVD growth, progress has been made through cloning of semiconducting CNTs [50], [51], integration of molecular seeds [52]–[54], specific catalyst configurations [55] and engineered catalyst particles. For the latter approach the catalyst particles have been externally synthesized and subsequently deposited on the substrate. Thereby, the size of the particles and the spacing between them are very well controlled. So far, from those methods only catalytic CVD reached a sufficient practical level in terms of type purity as well technological applicability for RF applications. Nevertheless, there are still huge challenges accompanied by high processing temperatures, which restrict integration scenarios to simple substrates without already integrated structures and electronics. To circumvent this drawback transfer processes, even combined with intermediate metallic removal steps [56], are preferable. Also the carrier mobility of CNTs on quartz is several times lower than on silicon dioxide. This necessitates the substrate transfer process of the aligned arrays any way.

The other widely-used method for producing RF CNTFETs is the 'preparation from solution' [57]. To achieve semiconducting purities of above 99.9%, a simple and highly scalable polymer-based solution sorting method is often used. When CNTs are dispersed with a conjugated polymer, the semiconducting CNTs will be solubilized and the semiconducting CNTs selectively stabilized within the CNT dispersion while the metallic tubes bundle and precipitate from the solution

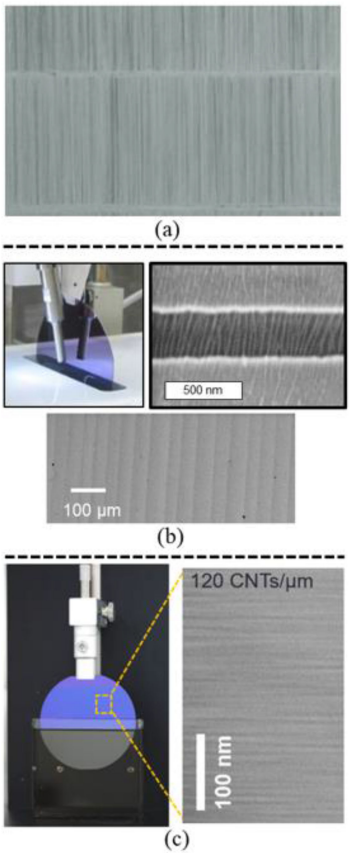

FIGURE 2. Aligned CNT arrays prepared by (a) directed CVD growth [25] (b) FESA using Carbonics Zebra technology [12] (c) DLSA method [77], [80]. Reproduced with permission from [12], [25], [71], [77], [80].

[58]. These solubilized CNTs can then be deposited into dense aligned arrays using various deposition techniques.

Dip-coating, incubation [59], spin-coating [60] or printing like techniques [61] are simple approaches to form randomly oriented CNT layers, inducing performance degradation though due to CNT-CNT junctions and crossings caused by random CNT orientation in the channel. Aligned CNT arrays from 'solution' on a substrate have been realized by Langmuir-Blodgett/Langmuir-Schaefer [62], [63], dielectrophoresis [61], [64]–[69] or evaporating-droplet [62], [70]–[73], approaches. Y. Joo *et al.* have demonstrated a self-assembly process called FESA (floating evaporative self-assembly) [74] resulting in the ZEBRA process developed at Carbonics. There, the high-purity CNTs are dispersed in a chloroform solvent and dropwise applied on a water surface as shown in Fig. 2(b). [12], [75]. As a vertically oriented wafer is slowly extracted from a water bath, a series of stick-slip events at the water/chloroform-wafer interface cause CNTs to deposit on wafer in a monolayer of dense (40–60 CNT/μm) and horizontally aligned (with the water surface) CNTs.

An innovation of the ZEBRA process was it produced a nearly continuous region of aligned CNTs within the deposition area without the limitation of periodic low-density, non-aligned CNT bands [12]. The Langmuir-Blodgett

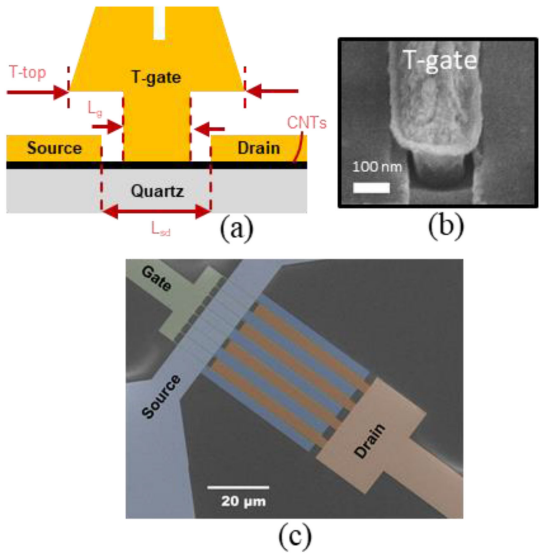

FIGURE 3. (a) sketch of a T-shape top gate on 4″ wafer and (b) corresponding SEM image, (c) SEM image [12] in false colors depicting a multifinger buried gate CNTFET on an 8" wafer. Reproduced with permission from [61].

technique yields linearly aligned tubes with 30–50 tubes/μm, whereas a very high density of about 500 tubes/μm is achieved by dielectrophoresis, which suffers though from weak gate modulation and reduced current density owing to thick multi-layer CNT films and serious tube-tube screening effects. Although this 'solution' approach is still not perfect, it has become the mainstream method [76] for aligned CNT arrays featuring high purity and density. In 2020, a group from Bejing University developed a multiple-dispersion & sorting process and a dimension limited self-alignment (DLSA) procedure [77] to prepare 4-inch wafer-scale well-aligned CNT arrays with a density of approximately 120–140 CNT/μm at a very high semiconducting purity of over 99.99%.

After CNT deposition, the surfactants or polymers have to be removed from the CNTs in order to achieve low-ohmic CNT-to-metal contacts, avoid hysteresis and maintain a high conductivity under bias conditions. While ionic surfactants are usually cleaned by a combination of a water, acid and thermal treatment [68], the polymer removal is more complex. To disperse the CNT typically PFO-based copolymers are used with the PFO monomer unit dispersing the CNTs and a second monomer unit to facilitate the polymer removal [78]. Thus, the cleaning procedure is adapted to the copolymer. The copolymer PFO-BPy features the best selective dispersing properties and is widely used but is rather difficult to remove. Joo *et al.* [79] have described a method to initially collapse the polymer and subsequently remove it from the CNTs.

Two RF CNTFET architectures have been reported in the literature, namely a top gate and a buried gate approach. While the best RF results until now were demonstrated with self-aligned T-shaped top gate devices, a buried gate device geometry has several advantages. According to Mothes *et al.* the parasitic capacitances are reduced and a higher control of the CNT-metal heterojunction is obtained [81], [82]. Moreover, it allows an unrestricted alignment of the gate electrode within the channel, enabling symmetrical and asymmetrical source-/drain- to gate spacers down to 0 nm, with the option to optimize the device for high linearity and breakdown voltage. Furthermore, access to the CNT top region is enabled, allowing for subsequent electrostatic doping approaches or sensor functionality. However, the alignment with respect to the source and drain electrodes is technologically challenging. Following this approach RF CNTFETs have been fabricated on 8″ wafer [61].

In contrast, following the self-aligned T-gate approach guarantees an excellent alignment because the top of the T-gate is used as a shadow mask for the source-drain contact metal. However, this approach too has its drawbacks since it constrains the T-gate top dimension to be the same as the channel spacing. Using the precision alignment of the ebeam lithography tool, these dimensions can be decoupled by applying the source-drain pattern first, to minimize the channel length, and the T-gate last to maximize its T-shape gate-head dimension. This approach is depicted in Fig. 3(a–b). Moreover, the bulky gate design results in a reduced gate resistance at the expense of somewhat higher parasitic capacitance. The gate resistance can be further reduced by a multi gate-finger design [61].

III. ELECTRICAL RESULTS

Over the past decade, performance of multitube CNTFETs built with both CVD grown and solution-processed CNTs have improved significantly. Before 2009, several preliminary works [19], [83]–[89] on RF performance of FETs based on film-like CNTs were published, representing the beginning of CNT based RF electronics. However, all of the intrinsic results were below 30 GHz mainly due to low purity. The extrinsic f_T of these CNTFETs have been increased from a few hundred MHz up to recently 100 GHz [83]–[87], [90]. In 2011, RF Nano Co. demonstrated a 4″ wafer CNTFET process with extrinsic values of f_T and maximum oscillation frequencies $f_{\max}$ around 10 GHz [13], [20], [89]. The CNT material used for that 4″ process was grown in-place directly on the substrate using CVD. The device had a source-drain distance of 800 nm, with a CNT density about 6∼7 CNTs/μm and no particular enhancement of semiconducting to metallic CNT ratio (i.e., only about 2/3 semiconducting CNTs). Even without the benefit of selectivity, the results demonstrate the quality of the tubes achievable from CVD growth and the reliability and repeatability of the CVD process itself. Following this approach Y. Che *et al.* demonstrated in 2013 a CNTFETs with an extrinsic f_T of 25 GHz and a 100 nm channel length [91]. For solution integrated CNTs with 300 nm gate length, $f_T = 9$ GHz along with $f_{\max}$ of 3 GHz was achieved in 2009 by enhancing semiconducting purity [88]. In 2012, IBM fabricated RF CNTFETs by dielectrophoresis-assembled CNTs with 100 nm L_g and pushed extrinsic f_T to 7 GHz and the extrinsic $f_{\max}$ up to 15 GHz [92]. After 2012, the USC group published a series of works [91], [93]–[97] on RF CNTFETs fabricated

by solution-based networks and solution-based aligned CNT arrays, all with a T-shaped gate structure for gate resistance reduction. Especially in 2016, Cao *et al.* from USC fabricated RF CNTFETs based on polyfluorene sorted aligned CNT arrays prepared by a dose-controlled, floating evaporative self-assembly approach. Process optimization yielded a current density of 350 μA/μm and a transconductance of 310 μS/μm along with extrinsic f_T and $f_{\max}$ of 70 GHz [95]. In 2019, the PKU group published results [90] based on a solution-derived randomly oriented CNT films with a transconductance up to 380 μS/μm. Due to the high density combined with successful channel length reduction, the extrinsic $f_{\max}$ exceeded 100 GHz for 30 nm gate length devices, representing the best extrinsic (only pad de-embedded) performance to date.

Recently, Carbonics demonstrated device performance in key metrics that are beginning to challenge incumbent technologies such as GaAs pHEMTs and RF-CMOS [12]. Their breakthrough performance was attributable to using densely aligned (40–60 CNT/μm), high purity (>99.9% semiconducting) CNT arrays and various process related improvements. When averaged over the top fifteen 100 nm gate-length T-gate devices from one 4-inch single-crystal quartz wafer, the as-measured performance was RF $g_{m,avg} = 330$ μS/μm, extrinsic $f_{T,avg} = 77$ GHz and $f_{max,avg} = 99$ GHz with the champion device having an extrinsic $f_T = 106$ GHz. This compares favorably to 130 nm RF-CMOS ($L_g \approx 100$ nm) with an f_T of 90 GHz [82] and is closing in on 100 nm gate-length GaAs pHEMT technology with an f_T of 130 GHz [83]. Fig. 4(a, b) shows select device data while Fig. 4(c–f) depicts histograms of aggregate data from 227 devices. It was also observed that these CNT-FETs produced a higher f_T/g_m value which suggests that as g_m is further increased towards its potential upper-bound (≈20 μS per CNT), or 3x in our case, one can project a much higher f_T upwards of 300 GHz for devices with an $L_g \approx 100$ nm.

Despite the potential intrinsic linearity, several early theoretical works [81], [99]–[101] analyzed realistic CNTFETs and pointed out three strict conditions should be met for high linearity: 1) ballistic single-subband transport, 2) ohmic contacts and 3) quantum capacitance limited operation [102]. Since especially the latter regime is practically impossible to achieve, investigations of realistic structures in [82], [103] have shown CNTFETs to be significantly more linear than modern microwave FETs depending on optimized design rules [82], [103].

So far, two experimental works showed real linearity performance for CNTFETs [12], [93]. Marsh *et al.* reported linearity measurements using the standard two-tone technique in combination with a triangle 1 kHz gate-voltage sweep for hysteresis mitigation. The respective champion devices showed peak OIP3/P_{dc} of 15.7 dB and an OIP3/P_{1dB} of 26.5 dB [12], [104]. (OIP3 is the output 3rd intercept point and P1dB is the one dB output gain compression point.) Generally, values exceeding the 10 dB rule-of-thumb for these figures of merit are considered very good and superior [12] to those of RF

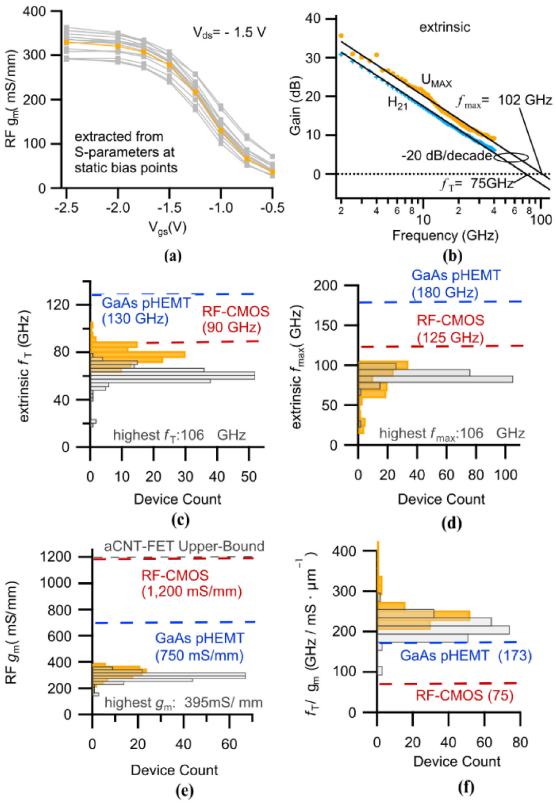

FIGURE 4. (a) Average RF transconductance (orange line) and (b) as-measured H_{21} and U_{max} data for a representative device. (c–f) Aggregated device data in histogram form of 107 T-gate aligned CNTFETs with L_g~110 nm (orange bars) and 220 devices with L_g~140 nm (grey bars) [12].

CMOS and on par with a commercial GaAs pHEMTs (Qorvo QPL6202Q).

A. IMPACT OF DEVICE DESIGN ON RF-PERFORMANCE

Utilizing a 200 mm wafer compatible CNT integration approach via printing, Hartmann *et al.* at TU Chemnitz have investigated the impact of symmetrical and asymmetrical source/drain-to-gate spacer length on the HF properties of CNTFETs [61]. For sake of reduced complexity, this study was performed with relaxed device dimensions of 280 nm channel length and unaligned CNTs. The polymer sorted CNT raw material was purchased from Nano Integris with a claimed purity of 99.9% semiconducting CNTs. In order to reduce parasitic S/D to gate electrode capacitances [82] (long spacer lengths) while maintaining an effective control over the metal-CNT contact (short spacer lengths), two sets of CNTFETs with varying spacer length were fabricated and studied, both with a constant channel length of 280 nm. An exemplary device is shown in Fig. 5. In the first step the spacer was varied symmetrically resulting in different gate lengths. To further reduce parasitic drain-gate capacitances the source-gate spacer were shrunk while increasing the drain spacer and maintaining a constant gate length.

Confirming theory [81], [82], the corresponding experimental results indicate, that the best device RF performance

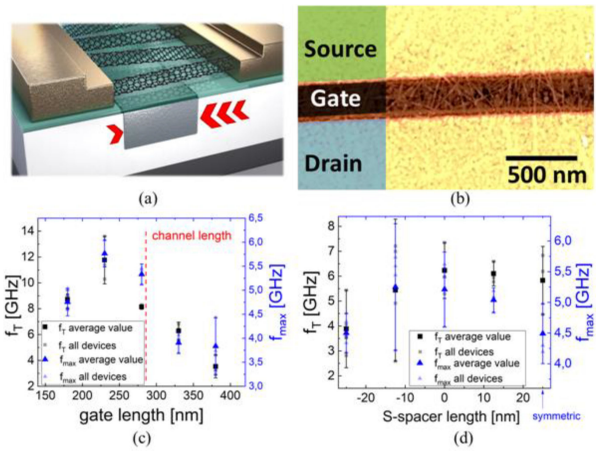

FIGURE 5. **gate spacer variation in CNTFETs with randomly oriented CNTs (a) sketch of a asymmetric buried gate design, (b) AFM image of the channel region featuring the unaligned CNTs, (c–d) gate length and gate-source spacer dependence of f_T and f_{max}. Reproduced with permission from [61].**

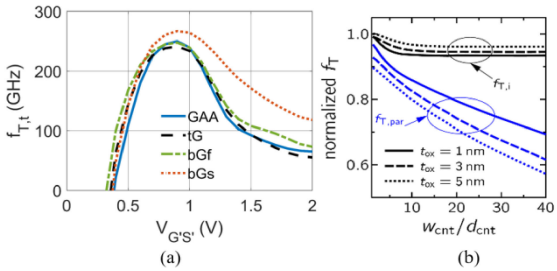

FIGURE 6. **(a) Transit frequency f_T (at $V_{DS} = 1$ V) of a single tube transistor (100 nm gate length) for different gate arrangements (GAA: gate all-around; tG: top gate; bG: buried gate). (b) f_T versus tube distance w_{cnt} (normalized to tube diameter d_{cnt}) from 3D calculations [106].**

can be achieved by properly balancing the device electrostatics. In particular, a spacer reduction between the gate and source electrode results in an increased control over the Schottky-like barrier between the metal and the CNT, with an increased conductance and transconductance at the cost of increased parasitic capacitances. Thus, according to equation (1) there is an optimum for the device speed for a certain spacer length. Highest values of f_{max} as well as f_T of symmetrical device designs were reported at a 25 nm spacer length. This is equivalent to an 82% coverage of the gate electrode within the channel. Thereby, f_{max} and f_T increased by 20% and 35%, respectively, compared to a 50 nm long spacer. Interestingly, they reported g_m decreased for an underlap between the gate electrode and the source electrode. This was attributed to the modulation of the heterojunction between the CNTs and the source metal on the bottom side of the contact where the CNTs are not covered by metal [105]. Increasing the drain-gate spacer length results in lower drain-gate electrode parasitic capacitances and thus increased device speed in addition to an increased breakdown voltage. They could show with respect to symmetrical structures an increase of 8% in f_T and 18% in f_{max} by shifting the gate- towards the source electrode at a 0 nm source-gate spacer. Moreover, it is highly promising to further investigate the linearity performance of CNTFETs with different gate spacer configurations [61], [82].

IV. DEVICE SIMULATION AND COMPACT MODELS

A. DEVICE SIMULATION (TCAD)

For incumbent technologies, device simulation has become an essential part of process development as it allows saving time and cost by minimizing experiments and enabling device design. The latter is also very important for emerging technologies in addition to obtaining a physics-based understanding of the fundamental device operation. For example, the bias dependent charge and capacitance on a single tube cannot be easily measured under transistor operating conditions, but can be obtained from device simulation, and the adjustment of device linearity in buried gate FETs by layout has been discovered through device simulation [81], [82].

While commercial simulation tools rarely support non-silicon-based emerging technologies, there is a plethora of CNT(FET) simulators from academia. All of them combine the solution of the Poisson equation with some carrier transport formulation approach. Most of the early approaches were based on either solving the ballistic Schrödinger equation or on solving the Boltzmann transport equation (BTE) along a 1D line representing the CNT (the so called line charge model). With an optical phonon scattering mean free path of ≈20 nm, ballistic transport is not a realistic assumption for typical transistor operating voltages in circuits, unless the channel length is very short, which is not the case for HF CNTFETs due to the required output power and resulting breakdown voltage requirements.

Optimizing a realistic 3D device structure requires many simulation runs and therefore short simulation times. The computational burden required to include scattering in the Schrödinger equation or to solve the BTE is too high despite all efforts to reduce the complexity. Hence, Mothes *et al.* developed an augmented drift-diffusion (aDD) transport approach in which CNTs are represented as cylinders and a complete 3D structure including the electrostatic interactions between adjacent CNTs can be investigated [106], [107]. The aDD transport models have been calibrated on results from the BTE with carrier scattering included as well as from measurements. Recent 3D device design investigations [82], [106] have shown that the best overall performance (e.g., speed, linearity, gain) is obtained by FET structures with a local buried gate (s. Fig. 6(a). Moreover, increasing the tube density in a multi-tube FET with aligned CNTs will always improve f_T (s. Fig. 6(b) since the increase in transconductance is always beneficial for charging the parasitic capacitances of an actual 3D structure.

B. COMPACT MODELING

Circuit design requires a representation of the fabricated devices in a computer-based design tool. The corresponding

models are known as compact models. The vast majority of publications in this area have focused on modeling the static drain current, I_D, for digital applications, assuming ohmic source/drain contacts. The latter does not represent reality since all fabricated CNTFETs have a heterojunction (often called Schottky) barrier [105], [108] between source/drain and the tube channel region. The often used capacitance-based charge model [109] is only valid around equilibrium, but not under non-linear circuit operating conditions. Evaluation of digital I_D models has uncovered discontinuities and severe limitations of the usable operating region [110]. This, combined with missing accurate charge descriptions, makes those models unsuitable for HF circuit design [111]. For the latter, a semi-physical and a modified virtual source MOSFET compact model have recently been implemented in commercial circuit simulators and demonstrated to be suitable [14], [112] for describing experimental data and for circuit simulation.

Typically, physics-based models are preferred in the semiconductor industry as they enable device scaling (for circuit optimization) as well as predictive and statistical modeling. However, CNTFET device physics understanding has not yet reached the state that fully allows physics-based models to be formulated. For instance, the calculation of I_D and the tube charge require a closed-form solution of integrals (e.g., the Landauer equation for I_D) which so far has turned out to be impossible without making too simplistic assumptions. The availability of a device simulation tool including all known relevant physical effects (especially the impact of the S/D heterojunction barrier) and being applicable to realistic structures and transistor operating conditions has accelerated the development of physics-based compact models. As long as HF measurements on single-tube FETs are elusive, device simulation will remain the main reference for model verification.

For matching the 50 Ω impedance and delivering sufficient amplifier output power in HF systems, FETs with up to thousands of parallel tubes are required. As detailed investigations have shown, the diameter variation of these tube due to process tolerances within a range of 1.1 nm to 2.3 nm does not change the shape of the bias dependent characteristics so that one can assume the formulations derived for a single tube but with properly adjusted model parameters. The electrostatic screening effect due to the proximity of adjacent tubes can be taken into account according to [106].

V. RF CIRCUITS

The demonstration of an emerging technology's application potential requires the design of integrated circuits (ICs) and the comparison of their performance with that of incumbent technologies. Especially for HF applications, building ICs is difficult as this requires competitive passive devices (i.e., the BEOL), the development of which is time consuming and costly. Thus, so far only ring oscillators [113], [114] or simple amplifiers have been built on-chip [12], [87], [89], [104], [115]–[121] while HF specific circuits such as amplifiers, a mixer and a VCO have been realized in discrete form [122]–[124]. For CVD processed FETs, metallic tubes have so far limited the circuit performance.

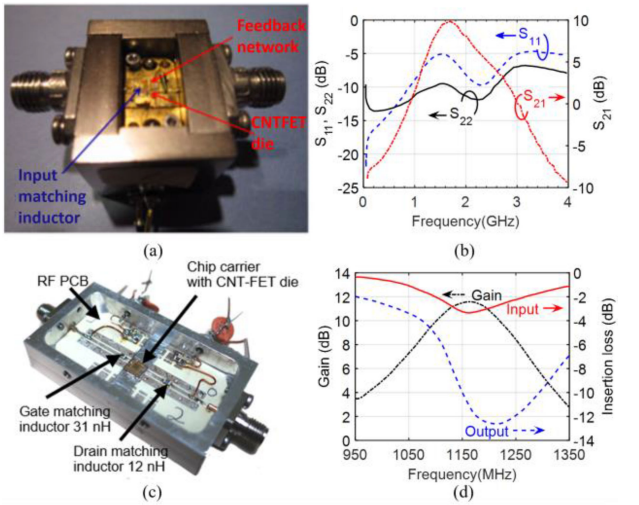

FIGURE 7. (a) Fastest discrete PCB based CNTFET amplifier module and (b) S-parameters vs. frequency of the corresponding two-stage CNTFET amplifier [89]. (c) CNTFET die mounted on alumina chip carrier and (d) gain and return loss of the completed amplifier module from [104]. Reproduced with permission from [104].

After about a decade of CNTFET development, first RF circuits based on CNTFETs were realized. In 2006, a group from Stanford University fabricated the first CNT-based amplifier [121] with 11.5 dB gain but at a frequency of 175 kHz and a unity voltage gain frequency of only 560 kHz due to the relatively high impedance of the single CNT employed. Two years later, Kocabas *et al.* demonstrated discrete RF amplifiers [87] based on aligned CNT arrays working at 125 MHz with 1-14 dB gain. The radio system built with these amplifiers could pick up a traffic report from a local radio station (1090 kHz) and has so far been the most complicated CNT-based RF system. In 2011, Eron *et al.* built the first ever CNTFET amplifier that operated at GHz (L-band) frequencies, employing multi-finger RF CNTFETs with 800 μm gate width in order to improve power drive ability and achieved 11 dB at 1.3 GHz [89]. A two-stage version using CNTFETs from the same wafer achieved 10 dB gain at 1.8 GHz (Fig. 7(a–b)), which has been the best performance so far.

In 2019, based on CNTFETs with 140 nm gate length, 50 μm gate width and over 100 GHz extrinsic operating frequency , Rutherglen *et al.* from Carbonics demonstrated an L-band (1.2 GHz) amplifier [12], [104]. Their CNTFETs were demonstrated within two simple amplifier circuits, each having the quartz CNTFET die mounted into a hard alumina chip carrier [104]. The CNTFET with chip carriers were then mounted in the RF PCB circuit as shown in Fig. 7(c–d). The use of a chip carrier enabled safe electrical bonding of the CNTFETs prior to mounting into the amplifier circuits. RF probe-compatible pads on the chip carriers allowed direct measurement of the combined CNTFET with chip carriers'

TABLE 1. Overview of Extrinsic f_T and f_{max} Values of RF CNTFETs Fabricated by Different CNT Integration Approaches and Source-Drain Contact Lengths (CL)

	$f_{T\,\mathrm{extr}}$ / GHz	$f_{max\,\mathrm{extr}}$ / GHz	CL / nm	CNT integr. technol.	Ref
Rutherglen et al.	~100	~100	110	FESA	[12]
Cao et al.	40	40	100	FESA	[95]
Wang et al.	15	5	500	CVD	[98]
Zhong et al.	86	85	50	Dip coating	[90]
Hartmann et al.	14	6	280	printing	[61]
Cao et al.	22	19	120	Dip coating	[96]
Louarn et al.	11		300	DEP	[85]
Che et al.	25		100	CVD	[72]

TABLE 2. Carbonics CNT FET Amplifier Overview

#	Gain	MSG	OIP3	P1dB	OIP3-P1dB
1	11.6 dB	16 dB	-1 to -1.8 dBm	-10.3 dBm	~10 dB
2	10 dB	17 dB	-1.8 to +0.4 dBm	-11.9 dBm	~12 dB

S-parameters. This approach enabled accurate design of the RF PCB circuit elements without having to separately model or measure the chip carrier. Laser milling at UCLA was used to form each chip carriers' metal patterns as well as to excavate backside pockets under their gate pads. These backside pockets significantly reduced the parasitic gate capacitance to improve gate matching and gain.

Table 2 and Fig. 7d show maximum gains ranging between 10–11.6 dB in a 50 Ω system. The amplifiers' OIP3 and P1dB ranged from −1.8 dBm to +0.4 dBm and 10–11 dB, respectively, as shown below.

Moreover, frequency synthesizers were also realized utilizing the nonlinear bias dependence of the tube capacitance and ambipolarity in narrow band gap CNTs. In 2009, a group from Stanford University designed and simulated frequency doublers and mixers [125]. Thanks to ballistic carrier transport, a signal up to a terahertz (THz) could be doubled in frequency, indicating the potential for THz circuit application. One year later, a group from PKU fabricated a frequency doubler [35] based on a single CNT that exhibited an operating frequency of just 1 kHz. In 2014, the same group using aligned CNT arrays by scalable fabrication [98] realized frequency doublers and mixers with output signals up to 40 GHz, a conversion gain of −66 dB limited by CNT purity in 2014, a LO power of 18 dBm and $P_{\mathrm{out}} = -44$ dBm at frequency of $f_{\mathrm{RF}} + f_{\mathrm{LO}}$ (40.4 GHz).

Due to the difficulties of fabricating integrated RF circuits, a simulation based study was recently performed based on the compact model CCAM [14] that was calibrated on the measurements of [12]. Integrated HF CNTFET amplifiers with feedback and matching assuming realistic quality factors were designed in [126] for comparison with 130 nm RF-CMOS, assuming the same passives (i.e., BEOL), gate

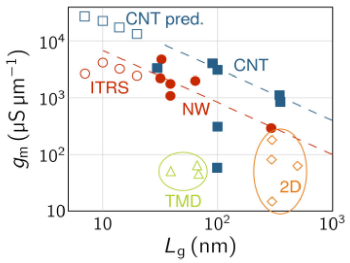

FIGURE 8. Transconductance per gate width vs. gate length: comparison of different FET technologies. Filled symbols represent measured data and open symbols TCAD predictions. The lower dashed line corresponds to RF-CMOS, the upper one to CNTFETs.

width and channel length. With the presently achievable low tube density of 10/μm and drain saturation current of about 15 μA, a double-stage 2.4 GHz LNA achieves ≈10 dB gain, 2.2 dB minimum noise figure and ≈15 dBm OIP_3 at a power consumption of 30 mW. This performance already matches that of RF-CMOS for the same process node.

VI. FUTURE DEVELOPMENT

Future CNTFET technology development will focus on three general aspects which are supported by simulations and modeling: (i) CNT layer morphology, (ii) device concept and structure, and (iii) system integration.

A. CNT LAYER MORPHOLOGY

Given the fact that most recent CNTFET performance has matched that of RF-CMOS at a similar channel length but with still relatively low tube density (≈50 /μm) and drain saturation current (≈5 μA/CNT), it becomes clear that with increasing CNT density and current per CNT the technology has the potential to significantly exceed RF-CMOS performance already at the device level by realizing high purity and high density aligned CNT layers. In addition, the fundamentally higher transconductance (see Fig. 8) enables faster drive capability in HF circuits.

However, several factors which would deteriorate the uniformity including the diameter-, chirality-, length distribution, tube-to-tube pitch fluctuation and CNT orientation dispersal need to be optimized.

Moreover, for the solution based CNT integration approach, the induced polymer molecules and other impurities around CNT and on the substrate need to be removed more efficiently. A negative impact on the high-speed performance due to charge traps induced hysteresis, an enhanced contact resistance and a reduced CNT conductance have to be avoided. Several approaches have demonstrated hysteresis free devices by, e.g eliminating or avoiding resist residuals and properly conditioning the substrate on which the CNTs are deposited [127].

However, a general approach for realizing hysteresis free CNTFETs with an in-depth and profound analysis of the various possible origins of the hysteresis has not been shown yet. It is believed that a clean interface that is free of charge traps is critical for eliminating the hysteresis. In the meantime,

researchers have demonstrated that reducing the gate oxide thickness of passivated CNTFETs can effectively reduce the hysteresis [128].

B. DEVICE STRUCTURE

A low contact resistance is very important for high performance transistors. A contact resistance less than 50 kΩ per CNT channel with good uniformity across the whole wafer is needed. A key point to be addressed is the overall current per tube, which is still below theoretical predictions and limits the overall device performance.

In addition, due to the absence of dangling bonds on the CNT surface combined with adsorbed polymer molecules a high interface charge density (N_{it}) exists in gate stacks, often resulting in severe hysteresis, reduced transconductance and an ALD (atomic layer deposition) process dilemma. Park *et al.* have suggested a profound approach to analyze charge trap densities in CNTFETs, allowing to differentiate between the impact of interface and surface traps [129]. A pulsed S-parameter measurement set-up with a discussion of duty cycle selection criteria has been described in [130] for obtaining the actual high-frequency small-signal characteristics required for device modeling and process development.

The T-shaped gate-head fabricated in [12], [91], [94] is not wide enough to reduce the gate resistance effectively. An improved gate stack for RF applications should be developed aiming at reduced interface trap density and gate resistance.

Doping of the CNTFETs is another element needed for high performance RF CNTFETs. Presently, electrostatic doping appears to be the only viable option. Contact and channel doping effects have to be separated and independently studied. Several ALD methods have been investigated for CNT doping. These include reactive molecules [38]–[40], which form a dipole layer at the interface between different high-k oxides [80], [131] and generating static intra layer charges using non-stoichiometric ALD [132]. While the last two approaches are the most promising methods to get stable and controllable doping profiles their possible impact onto device hysteresis has to be investigated in more detail. Moreover, an effective passivation technology is especially important for buried-gate geometries. It further allows the reduction of CNT-bundle induced enhanced off-currents [69].

Implementing future devices using a buried-gate structure has multiple benefits. First, moving the CNT deposition step from the beginning towards the end of the process-flow will reduce the potential for contaminant accumulation during the intermediate steps. This is particularly important for CNTs because normal O_2 ashing of the surface is not possible without destroying the CNTs themselves.

In addition, it allows tuning the HF device characteristics (i.e., linearity vs. speed) towards the desired application just by layout. Here, the actual device design with asymmetric gate positions and gate spacers has to be explored in more detail, especially its potential of high linearity.

On the digital side, CNTFETs with their single-atomic channel, optimal channel control, superior temperature stability [3], and well (i.e., Schottky barrier) defined channel lengths are very attractive for extreme scaling and high packing density of digital circuitry possibly on the same chip.

However, corresponding milestones for CNT materials [77] have been only proved on 4-inch wafers but have to be realized in larger scale on 8-inch or even 12-inch wafers for industrial applications.

C. SYSTEM INTEGRATION

To date, compared with RF CNTFET progress, RF system design lags behind because of its complexity especially when frequencies are rising. In order to push CNTFET technology for RF applications, a system design including passives and peripheral components requires accurate device models and compatible processes. Solutions for these problems should promote CNTFET technology and demonstrate its promising features in future RF applications. As a path towards such systems, competitive integrated CNTFET based RF circuits have yet to be built.

A slightly different approach is the heterointegration of CNT technology with incumbent high performance digital technologies to combine the advantages of the different worlds. Especially the heterointegration with CMOS in a hybrid foundry environment is highly promising. For example, the CMOS or other passive elements for mixed-signal applications can be completed on virgin wafers that are then passivated and planarized all within a commercial foundry. The wafers would then be processed in a CNT-approved environment for final CNT deposition and connection with the underlying CMOS circuit through vias. This essentially makes the CNT step a BEOL process.

In contrast to 3D bulk semiconductor technologies the CNTFET technology allows a 3D integration with a high vertical integration density enabling power efficient signal transmission.

This technology is not restricted to rigid substrates. It possesses the potential to transfer the performance of rigid electronics to flexible substrates and flexible applications.

Furthermore, the functionality of RF CNT based circuits can be augmented on chip by a large variety of CNT based devices with different functionality, such as chemical and (i.e., THz [6]) sensors, super-capacitors, transmission lines and inductors. This make CNTFET technology very appealing for realizing high-complexity all-CNT systems on a single chip.

VII. SUMMARY

This review summarizes the different technological approaches and the electrical performance of CNTFETs for analog RF applications. Currently, the CNT integration approaches from organic solution by FESA or DLSA feature the best results in the context of CNT layer morphology and the corresponding electrical performance data. However, realizing highly semiconducting enriched dense CNT layers by CVD in the future potentially alters this trend due to a higher CNT quality. State of the art solution processed RF CNTFETs fabricated by Carbonics Inc. have already achieved

f_T values over 100 GHz which is on par with Si-CMOS at the 130 nm technology node. These results were achieved with a moderate CNT density and current per tube. A group from Peking University has already demonstrated a more than two times higher CNT density for DC CNTFETs. Moreover, a four times higher current per CNT was similarly presented, which together with a device geometry optimization promises a further RF CNTFET performance improvement. Such devices are up to now integrated only into discrete RF circuits. As a next step their applicability in integrated RF circuits needs to be demonstrated. This will promote CNTFET technology to extend into flexible electronics and supports the emergence of competitive RF CNTFET based electronics and potentially an all-CNT SOC.

REFERENCES

[1] A. Javey *et al.*, "High-field quasiballistic transport in short carbon nanotubes," *Phys. Rev. Lett.*, vol. 92, no. 10, 2004, Art. no. 106804.

[2] M. Luisier, M. Lundstrom, D. A. Antoniadis, and J. Bokor, "Ultimate device scaling: Intrinsic performance comparisons of carbon-based, ingaas, and si field-effect transistors for 5 nm gate length," in *Proc. IEEE Int. Electron Devices Meet.*, 2011, pp. 11.2.1–11.2.4.

[3] P. Sakalas, M. Claus, M. Schroter, and A. Rumiantsev, "Experimental characterization of temperature-dependent electron transport in single-wall multi-tube carbon nanotube transistors," *Phys. Status Solidi RRL*, vol. 6, no. 2, pp. 62–64, 2012.

[4] A. Betti, G. Fiori, and G. Iannaccone, "Shot noise suppression in quasi-one-dimensional field-effect transistors," *IEEE Trans. Electron Devices*, vol. 56, no. 9, pp. 2137–2143, Sep. 2009.

[5] T. S. Perry, "Biosensors for on-the-spot tests: Two companies plan to debut new tech for COVID-19 testing by year's end - [News]," *IEEE Spectr*, vol. 57, no. 7, pp. 9–10, Jul. 2020.

[6] M. Bauer *et al.*, "The potential for sensitivity enhancement by the thermoelectric effect in carbon-nanotube and graphene Tera-FETs," *J. Phys., Conf. Ser.*, vol. 647, 2015, Art. no. 12004.

[7] A. Naeemi, R. Sarvari, and J. D. Meindl, "Performance comparison between carbon nanotube and copper interconnects for gigascale integration (GSI)," *IEEE Electron Device Lett.*, vol. 26, no. 2, pp. 84–86, Feb. 2005.

[8] A. Nieuwoudt and Y. Massoud, "Evaluating the impact of resistance in carbon nanotube bundles for VLSI interconnect using diameter-dependent modeling techniques," *IEEE Trans. Electron Devices*, vol. 53, no. 10, pp. 2460–2466, Oct. 2006.

[9] J. Cao, S. T. Bartsch, and A. M. Ionescu, "Large-scale assembly of tunable resonant-body carbon nanotube transistors without hysteresis," in *Proc. Int. Elect. Devices Meet.*, San Francisco, CA, 2012, pp. 15.3.1–15.3.4.

[10] A. D. Franklin *et al.*, "Carbon nanotube complementary wrap-gate transistors," *Nano Lett.*, vol. 13, no. 6, pp. 2490–2495, 2013.

[11] M. M. Shulaker *et al.*, "Three-dimensional integration of nanotechnologies for computing and data storage on a single chip," *Nature*, vol. 547, no. 7661, pp. 74–78, 2017.

[12] C. Rutherglen *et al.*, "Wafer-scalable, aligned carbon nanotube transistors operating at frequencies of over 100 GHz," *Nature Electron.*, vol. 2, no. 11, pp. 530–539, 2019.

[13] M. Schroter *et al.*, "A 4″ wafer photostepper-based carbon nanotube FET technology for RF applications," in *Proc. IEEE MTT-S Int. Microw. Symp.*, Jun. 2011, pp. 1–4.

[14] M. Schroter, M. Haferlach, A. Pacheco-Sanchez, S. Mothes, P. Sakalas, and M. Claus, "A semiphysical large-signal compact carbon nanotube FET model for analog RF applications," *IEEE Trans. Electron Devices*, vol. 62, no. 1, pp. 52–60, Jan. 2015.

[15] C. Rutherglen, D. Jain, and P. Burke, "Nanotube electronics for radiofrequency applications," *Nature Nanotechnol.*, vol. 4, no. 12, pp. 811–819, 2009.

[16] J. Cui, D. Yang, X. Zeng, N. Zhou, and H. Liu, "Recent progress on the structure separation of single-wall carbon nanotubes," *Nanotechnology*, vol. 28, no. 45, 2017, Art. no. 452001.

[17] Q. Cao, S.-J. Han, G. S. Tulevski, A. D. Franklin, and W. Haensch, "Evaluation of field-effect mobility and contact resistance of transistors that use solution-processed single-walled carbon nanotubes," *ACS Nano*, vol. 6, no. 7, pp. 6471–6477, 2012.

[18] A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. Dai, "Ballistic carbon nanotube field-effect transistors," *Nature*, vol. 424, no. 6949, pp. 654–657, 2003.

[19] D. Wang, Z. Yu, S. McKernan, and P. J. Burke, "Ultrahigh frequency carbon nanotube transistor based on a single nanotube," *IEEE Trans. Nanotechnol.*, vol. 6, no. 4, pp. 400–403, Jul. 2007.

[20] M. Schroter, M. Claus, P. Sakalas, M. Haferlach, and D. Wang, "Carbon nanotube FET technology for radio-frequency electronics: State-of-the-art overview," *IEEE J. Electron Devices Soc.*, vol. 1, no. 1, pp. 9–20, Jan. 2013.

[21] S. Huang, X. Cai, and J. Liu, "Growth of millimeter-long and horizontally aligned single-walled carbon nanotubes on flat substrates," *J. Amer. Chem. Soc.*, vol. 125, no. 19, pp. 5636–5637, 2003.

[22] S. Huang, M. Woodson, R. Smalley, and J. Liu, "Growth mechanism of oriented long single walled carbon nanotubes using "fast-heating" chemical vapor deposition process," *Nano Lett.*, vol. 4, no. 6, pp. 1025–1028, 2004.

[23] Z. Yu, S. Li, and P. J. Burke, "Synthesis of aligned arrays of millimeter long, straight single-walled carbon nanotubes," *Chem. Mater.*, vol. 16, no. 18, pp. 3414–3416, 2004.

[24] L. Huang *et al.*, "Cobalt ultrathin film catalyzed ethanol chemical vapor deposition of single-walled carbon nanotubes," *J. Phys. Chem. B*, vol. 110, no. 23, pp. 11103–11109, 2006.

[25] L. Ding *et al.*, "Selective growth of well-aligned semiconducting single-walled carbon nanotubes," *Nano Lett.*, vol. 9, no. 2, pp. 800–805, 2009.

[26] E. Joselevich and C. M. Lieber, "Vectorial growth of metallic and semiconducting single-wall carbon nanotubes," *Nano Lett.*, vol. 2, no. 10, pp. 1137–1141, 2002.

[27] A. Ural, Y. Li, and H. Dai, "Electric-field-aligned growth of single-walled carbon nanotubes on surfaces," *Appl. Phys. Lett.*, vol. 81, no. 18, pp. 3464–3466, 2002.

[28] W. Zhou, C. Rutherglen, and P. J. Burke, "Wafer scale synthesis of dense aligned arrays of single-walled carbon nanotubes," *Nano Res.*, vol. 1, no. 2, pp. 158–165, 2008.

[29] L. Ding, D. Yuan, and J. Liu, "Growth of high-density parallel arrays of long single-walled carbon nanotubes on quartz substrates," *J. Amer. Chem. Soc.*, vol. 130, no. 16, pp. 5428–5429, 2008.

[30] H. Ago, K. Imamoto, N. Ishigami, R. Ohdo, K.-I. Ikeda, and M. Tsuji, "Competition and cooperation between lattice-oriented growth and step-templated growth of aligned carbon nanotubes on sapphire," *Appl. Phys. Lett.*, vol. 90, no. 12, 2007, Art. no. 123112.

[31] C. Kocabas, S.-H. Hur, A. Gaur, M. A. Meitl, M. Shim, and J. A. Rogers, "Guided growth of large-scale, horizontally aligned arrays of single-walled carbon nanotubes and their use in thin-film transistors," *Small (Weinheim an der Bergstrasse, Germany)*, vol. 1, no. 11, pp. 1110–1116, 2005.

[32] S. Han, X. Liu, and C. Zhou, "Template-free directional growth of single-walled carbon nanotubes on a- and r-plane sapphire," *J. Amer. Chem. Soc.*, vol. 127, no. 15, pp. 5294–5295, 2005.

[33] H. Ago, K. Nakamura, K.-I. Ikeda, N. Uehara, N. Ishigami, and M. Tsuji, "Aligned growth of isolated single-walled carbon nanotubes programmed by atomic arrangement of substrate surface," *Chem. Phys. Lett.*, vol. 408, no. 4-6, pp. 433–438, 2005.

[34] A. Ismach, L. Segev, E. Wachtel, and E. Joselevich, "Atomic-step-templated formation of single wall carbon nanotube patterns," *Angew. Chem.*, vol. 116, no. 45, pp. 6266–6269, 2004.

[35] Z. Wang *et al.*, "Large signal operation of small band-gap carbon nanotube-based ambipolar transistor: A high-performance frequency doubler," *Nano Lett.*, vol. 10, no. 9, pp. 3648–3655, 2010.

[36] C. Wang *et al.*, "Synthesis and device applications of high-density aligned carbon nanotubes using low-pressure chemical vapor deposition and stacked multiple transfer," *Nano Res.*, vol. 3, no. 12, pp. 831–842, 2010.

[37] W. Zhou, L. Ding, S. Yang, and J. Liu, "Synthesis of high-density, large-diameter, and aligned single-walled carbon nanotubes by multiple-cycle growth methods," *ACS Nano*, vol. 5, no. 5, pp. 3849–3857, 2011.

[38] J. Li *et al.*, "Growth of high-density-aligned and semiconducting-enriched single-walled carbon nanotubes: Decoupling the conflict between density and selectivity," *ACS Nano*, vol. 8, no. 1, pp. 554–562, 2014.

[39] C.-M. Yang *et al.*, "Preferential etching of metallic single-walled carbon nanotubes with small diameter by fluorine gas," *Phys. Rev. B*, vol. 73, no. 7, pp. 075419-1–075419-7, 2006.

[40] G. Zhang *et al.*, "Selective etching of metallic carbon nanotubes by gas-phase reaction," *Science*, vol. 314, no. 5801, pp. 974–977, 2006.

[41] P. G. Collins, M. S. Arnold, and P. Avouris, "Engineering carbon nanotubes and nanotube circuits using electrical breakdown," *Science*, vol. 292, no. 5517, pp. 706–709, 2001.

[42] H. Huang, R. Maruyama, K. Noda, H. Kajiura, and K. Kadono, "Preferential destruction of metallic single-walled carbon nanotubes by laser irradiation," *J. Phys. Chem. B*, vol. 110, no. 14, pp. 7316–7320, 2006.

[43] H. C. Shim, J.-W. Song, Y. K. Kwak, S. Kim, and C.-S. Han, "Preferential elimination of metallic single-walled carbon nanotubes using microwave irradiation," *Nanotechnology*, vol. 20, no. 6, 2009, Art. no. 65707.

[44] J. Song, Y. Li, F. Du, X. Xie, Y. Huang, and J. A. Rogers, "Thermal analysis for laser selective removal of metallic single-walled carbon nanotubes," *J. Appl. Phys.*, vol. 117, no. 16, 2015, Art. no. 165102.

[45] X. Xie *et al.*, "Microwave purification of large-area horizontally aligned arrays of single-walled carbon nanotubes," *Nature Commun.*, vol. 5, 2014, Art. no. 5332.

[46] J. Song *et al.*, "Modeling of thermocapillary flow to purify single-walled carbon nanotubes," *RSC Adv.*, vol. 4, no. 80, pp. 42454–42461, 2014.

[47] F. Du *et al.*, "Laser-induced nanoscale thermocapillary flow for purification of aligned arrays of single-walled carbon nanotubes," *ACS Nano*, vol. 8, no. 12, pp. 12641–12649, 2014.

[48] S. H. Jin *et al.*, "Using nanoscale thermocapillary flows to create arrays of purely semiconducting single-walled carbon nanotubes," *Nature Nanotechnol.*, vol. 8, no. 5, pp. 347–355, 2013.

[49] S. Hun Jin *et al.*, "Fundamental effects in nanoscale thermocapillary flow," *J. Appl. Phys.*, vol. 115, no. 5, 2014, Art. no. 54315.

[50] B. Liu, F. Wu, H. Gui, M. Zheng, and C. Zhou, "Chirality-controlled synthesis and applications of single-wall carbon nanotubes," *ACS Nano*, vol. 11, no. 1, pp. 31–53, 2017.

[51] J. R. Sanchez-Valencia *et al.*, "Controlled synthesis of single-chirality carbon nanotubes," *Nature*, vol. 512, no. 7512, pp. 61–64, 2014.

[52] K. Y. Amsharov, "Combinatorial approach for the synthesis of precursors for chirality-controlled synthesis of SWCNTs," *Phys. Status Solidi B*, vol. 252, no. 11, pp. 2466–2471, 2015.

[53] J. R. Sanchez-Valencia *et al.*, "Controlled synthesis of single-chirality carbon nanotubes," *Nature*, vol. 512, no. 7512, pp. 61–64, 2014.

[54] N. Abdurakhmanova *et al.*, "Bottom up fabrication of (9, 0) zigzag and (6, 6) armchair carbon nanotube end-caps on the rh(1 1 1) surface," *Carbon*, vol. 84, pp. 444–447, 2015.

[55] S. M. Jafarpour, S. E. Schulz, and S. Hermann, "Tuning of diameter and electronic type of CCVD grown SWCNTs: A comparative study on Co-Mo and Co-Ru bimetallic catalyst systems," *Diamond Related Mater.*, vol. 89, pp. 18–27, 2018.

[56] S. H. Jin *et al.*, "Using nanoscale thermocapillary flows to create arrays of purely semiconducting single-walled carbon nanotubes," *Nature Nanotechnol.*, vol. 8, no. 5, pp. 347–355, 2013.

[57] M. C. Hersam, "Progress towards monodisperse single-walled carbon nanotubes," *Nature Nanotechnol.*, vol. 3, no. 7, pp. 387–394, 2008.

[58] J. Ding, Z. Li, J. Lefebvre, X. Du, and P. R. L. Malenfant, "Mechanistic consideration of pH effect on the enrichment of semiconducting SWCNTs by conjugated polymer extraction," *J. Phys. Chem. C*, vol. 120, no. 38, pp. 21946–21954, 2016.

[59] M. D. Bishop *et al.*, "Fabrication of carbon nanotube field-effect transistors in commercial silicon manufacturing facilities," *Nature Electron*, vol. 3, no. 8, pp. 492–501, 2020.

[60] M. C. LeMieux, M. Roberts, S. Barman, Y. W. Jin, J. M. Kim, and Z. Bao, "Self-sorted, aligned nanotube networks for thin-film transistors," *Science*, vol. 321, no. 5885, pp. 101–104, 2008.

[61] M. Hartmann *et al.*, "Gate spacer investigation for improving the speed of high-frequency carbon nanotube-based field-effect transistors," *ACS Appl. Mater. Interfaces*, vol. 12, no. 24, pp. 27461–27466, 2020.

[62] G. J. Brady, Y. Joo, M.-Y. Wu, M. J. Shea, P. Gopalan, and M. S. Arnold, "Polyfluorene-sorted, carbon nanotube array field-effect transistors with increased current density and high on/off ratio," *ACS Nano*, vol. 8, no. 11, pp. 11614–11621, 2014.

[63] X. Li *et al.*, "Langmuir-blodgett assembly of densely aligned single-walled carbon nanotubes from bulk materials," *J. Amer. Chem. Soc.*, vol. 129, no. 16, pp. 4890–4891, 2007.

[64] A. R. Boccaccini, J. Cho, J. A. Roether, B. J. C. Thomas, E. J. Minay, and M. S. P. Shaffer, "Electrophoretic deposition of carbon nanotubes," *Carbon*, vol. 44, no. 15, pp. 3149–3160, 2006.

[65] R. Krupke, S. Linden, M. Rapp, and F. Hennrich, "Thin films of metallic carbon nanotubes prepared by dielectrophoresis," *Adv. Mater.*, vol. 18, no. 11, pp. 1468–1470, 2006.

[66] C. Rutherglen, D. Jain, and P. Burke, "RF resistance and inductance of massively parallel single walled carbon nanotubes: Direct, broadband measurements and near perfect 50Ω impedance matching," *Appl. Phys. Lett.*, vol. 93, no. 8, 2008, Art. no. 83119.

[67] Q. Cao, S.-J. Han, and G. S. Tulevski, "Fringing-field dielectrophoretic assembly of ultrahigh-density semiconducting nanotube arrays with a self-limited pitch," *Nature Commun.*, vol. 5, 2014, Art. no. 5071.

[68] J. Tittmann-Otto *et al.*, "Effect of cleaning procedures on the electrical properties of carbon nanotube transistors—A statistical study," *J. Appl. Phys.*, vol. 119, no. 12, 2016, Art. no. 124509.

[69] M. Hartmann, R. Schubel, M. Claus, R. Jordan, S. E. Schulz, and S. Hermann, "Polymer-based doping control for performance enhancement of wet-processed short-channel CNTFETs," *Nanotechnology*, vol. 29, no. 3, 2018, Art. no. 35203.

[70] R. Sharma, C. Y. Lee, J. H. Choi, K. Chen, and M. S. Strano, "Nanometer positioning, parallel alignment, and placement of single anisotropic nanoparticles using hydrodynamic forces in cylindrical droplets," *Nano Lett.*, vol. 7, no. 9, pp. 2693–2700, 2007.

[71] M. Engel *et al.*, "Thin film nanotube transistors based on self-assembled, aligned, semiconducting carbon nanotube arrays," *ACS Nano*, vol. 2, no. 12, pp. 2445–2452, 2008.

[72] G. J. Brady, Y. Joo, S. S. Roy, P. Gopalan, and M. S. Arnold, "High performance transistors via aligned polyfluorene-sorted carbon nanotubes," *Appl. Phys. Lett.*, vol. 104, no. 8, 2014, Art. no. 83107.

[73] Y. Joo, G. J. Brady, M. S. Arnold, and P. Gopalan, "Dose-controlled, floating evaporative self-assembly and alignment of semiconducting carbon nanotubes from organic solvents," *Langmuir, The ACS J. Surfaces Colloids*, vol. 30, no. 12, pp. 3460–3466, 2014.

[74] Y. Joo, G. J. Brady, M. S. Arnold, and P. Gopalan, "Dose-controlled, floating evaporative self-assembly and alignment of semiconducting carbon nanotubes from organic solvents," *Langmuir, The ACS J. Surfaces Colloids*, vol. 30, no. 12, pp. 3460–3466, 2014.

[75] G. J. Brady, A. J. Way, N. S. Safron, H. T. Evensen, P. Gopalan, and M. S. Arnold, "Quasi-ballistic carbon nanotube array transistors with current density exceeding si and GaAs," *Sci. Adv.*, vol. 2, no. 9, 2016, Paper e1601240.

[76] D. Zhong, Z. Zhang, and L.-M. Peng, "Carbon nanotube radio-frequency electronics," *Nanotechnology*, vol. 28, no. 21, 2017, Art. no. 212001.

[77] L. Liu *et al.*, "Aligned, high-density semiconducting carbon nanotube arrays for high-performance electronics," *Science*, vol. 368, no. 6493, pp. 850–856, 2020.

[78] T. Lei, I. Pochorovski, and Z. Bao, "Separation of semiconducting carbon nanotubes for flexible and stretchable electronics using polymer removable method," *Accounts Chem. Res.*, vol. 50, no. 4, pp. 1096–1104, 2017.

[79] Y. Joo *et al.*, "Polymer-free electronic-grade aligned semiconducting carbon nanotube array," *ACS Appl. Mater. Interfaces*, vol. 9, no. 34, pp. 28859–28867, 2017.

[80] Y. Li *et al.*, "Preferential growth of semiconducting single-walled carbon nanotubes by a plasma enhanced CVD method," *Nano Lett.*, vol. 4, no. 2, pp. 317–321, 2004.

[81] S. Mothes, M. Claus, and M. Schroter, "Toward linearity in schottky barrier CNTFETs," *IEEE Trans. Nanotechnol.*, vol. 14, no. 2, pp. 372–378, Mar. 2015.

[82] S. Mothes, M. Claus, and M. Schroter, "Toward RF-linearity for planar local back- and top-gate SB-CNTFETs," in *Proc. Int. Conf. Simul. Semicond. Processes Devices*, Sep. 2015, pp. 92–95.

[83] J.-M. Bethoux, H. Happy, G. Dambrine, V. Derycke, M. Goffman, and J.-P. Bourgoin, "An 8-GHz f/sub t/ carbon nanotube field-effect transistor for gigahertz range applications," *IEEE Electron Device Lett.*, vol. 27, no. 8, pp. 681–683, Aug. 2006.

[84] S. J. Kang *et al.*, "High-performance electronics using dense, perfectly aligned arrays of single-walled carbon nanotubes," *Nature Nanotechnol.*, vol. 2, no. 4, pp. 230–236, 2007.
[85] A. Le Louarn *et al.*, "Intrinsic current gain cutoff frequency of 30GHz with carbon nanotube transistors," *Appl. Phys. Lett.*, vol. 90, no. 23, 2007, Art. no. 233108.
[86] C. Kocabas *et al.*, "High-frequency performance of submicrometer transistors that use aligned arrays of single-walled carbon nanotubes," *Nano Lett.*, vol. 9, no. 5, pp. 1937–1943, 2009.
[87] C. Kocabas *et al.*, "Radio frequency analog electronics based on carbon nanotube transistors," *Proc. Nat. Acad. Sci. USA*, vol. 105, no. 5, pp. 1405–1409, 2008.
[88] L. Nougaret *et al.*, "80 GHz field-effect transistors produced using high purity semiconducting single-walled carbon nanotubes," *Appl. Phys. Lett.*, vol. 94, no. 24, 2009, Art. no. 243505.
[89] M. Eron, S. Lin, D. Wang, M. Schroter, and P. Kempf, "L-band carbon nanotube transistor amplifier," *Electron. Lett.*, vol. 47, no. 4, pp. 265–266, 2011.
[90] D. Zhong *et al.*, "Carbon nanotube film-based radio frequency transistors with maximum oscillation frequency above 100 GHz," *ACS Appl. Mater. Interfaces*, vol. 11, no. 45, pp. 42496–42503, 2019.
[91] Y. Che, Y.-C. Lin, P. Kim, and C. Zhou, "T-gate aligned nanotube radio frequency transistors and circuits with superior performance," *ACS Nano*, vol. 7, no. 5, pp. 4343–4350, 2013.
[92] M. Steiner *et al.*, "High-frequency performance of scaled carbon nanotube array field-effect transistors," *Appl. Phys. Lett.*, vol. 101, no. 5, 2012, Art. no. 53123.
[93] C. Wang *et al.*, "Radio frequency and linearity performance of transistors using high-purity semiconducting carbon nanotubes," *ACS Nano*, vol. 5, no. 5, pp. 4169–4176, 2011.
[94] Y. Che *et al.*, "Self-aligned T-gate high-purity semiconducting carbon nanotube RF transistors operated in quasi-ballistic transport and quantum capacitance regime," *ACS Nano*, vol. 6, no. 8, pp. 6936–6943, 2012.
[95] Y. Cao, G. J. Brady, H. Gui, C. Rutherglen, M. S. Arnold, and C. Zhou, "Radio frequency transistors using aligned semiconducting carbon nanotubes with current-gain cutoff frequency and maximum oscillation frequency simultaneously greater than 70 GHz," *ACS Nano*, vol. 10, no. 7, pp. 6782–6790, 2016.
[96] Y. Cao, Y. Che, H. Gui, X. Cao, and C. Zhou, "Radio frequency transistors based on ultra-high purity semiconducting carbon nanotubes with superior extrinsic maximum oscillation frequency," *Nano Res.*, vol. 9, no. 2, pp. 363–371, 2016.
[97] Y. Cao, Y. Che, J.-W. T. Seo, H. Gui, M. C. Hersam, and C. Zhou, "High-performance radio frequency transistors based on diameter-separated semiconducting carbon nanotubes," *Appl. Phys. Lett.*, vol. 108, no. 23, 2016, Art. no. 233105.
[98] Z. Wang *et al.*, "Scalable fabrication of ambipolar transistors and radio-frequency circuits using aligned carbon nanotube arrays," *Adv. Mater.*, vol. 26, no. 4, pp. 645–652, 2014.
[99] J. E. Baumgardner, A. A. Pesetski, J. M. Murduck, J. X. Przybysz, J. D. Adam, and H. Zhang, "Inherent linearity in carbon nanotube field-effect transistors," *Appl. Phys. Lett.*, vol. 91, no. 5, 2007, Art. no. 52107.
[100] A. Curutchet *et al.*, "Nonlinear characterization and modeling of carbon nanotube field-effect transistors," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 7, pp. 1505–1510, Jul. 2008.
[101] A. U. Alam, C. M. S. Rogers, N. Paydavosi, K. D. Holland, S. Ahmed, and M. Vaidyanathan, "RF linearity potential of carbon-nanotube transistors versus MOSFETs," *IEEE Trans. Nanotechnol.*, vol. 12, no. 3, pp. 340–351, May 2013.
[102] S. O. Koswatta, A. Valdes-Garcia, M. B. Steiner, Y.-M. Lin, and P. Avouris, "Ultimate RF performance potential of carbon electronics," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 10, pp. 2739–2750, Oct. 2011.
[103] S. Maas, "Linearity and dynamic range of carbon nanotube field-effect transistors," in *Proc. IEEE MTT-S Int. Microw. Symp.*, 2017, pp. 87–90.
[104] P. F. Marsh and C. Rutherglen, "Solving the linearity and power conundrum: Carbon nanotube RF amplifiers," *Microw. J.*, vol. 62, no. 6, pp. 22–32, 2019.
[105] A. Fediai *et al.*, "Towards an optimal contact metal for CNTFETs," *Nanoscale*, vol. 8, no. 19, pp. 10240–10251, 2016.
[106] S. Mothes and M. Schroter, "Three-dimensional transport simulations and modeling of densely packed CNTFETs," *IEEE Trans. Nanotechnol.*, vol. 17, no. 6, pp. 1282–1287, Nov. 2018.
[107] S. Mothes, "Augmented semiclassical transport models for carbon nanotube field effect transistors," Ph.D. dissertation, Tech. Univ. Dresden, 2019.
[108] M. Claus, S. Mothes, S. Blawid, and M. Schröter, "COOS: A wavefunction based schrödinger–poisson solver for ballistic nanotube transistors," *J. Comput. Electron.*, vol. 13, no. 3, pp. 689–700, 2014.
[109] A. Rahman, J. Guo, S. Datta, and M. S. Lundstrom, "Theory of ballistic nanotransistors," *IEEE Trans. Electron Devices*, vol. 50, no. 9, pp. 1853–1864, Sep. 2003.
[110] I. Bejenari, M. Schroter, and M. Claus, "Analytical drain current model of one-dimensional ballistic schottky-barrier transistors," *IEEE Trans. Electron Devices*, vol. 64, no. 9, pp. 3904–3911, Sep. 2017.
[111] M. Claus, M. Haferlach, D. Gross, and M. Schroter, "Critical review of CNTFET compact models," in *Proc. Int. NanoTechnol. Meet. WCM*, 2012, pp. 110–775.
[112] S. Mothes, F. Wolf, and M. Schroter, "Flexible virtual source compact model for efficient modeling of emerging channel materials and device architectures," in *Proc. Nanotechnol., Workshop Compact Model*, Anaheim, CA, USA, 2018, pp. 244–248.
[113] L. Liu *et al.*, "Carbon nanotube complementary gigahertz integrated circuits and their applications on wireless sensor interface systems," *ACS Nano*, vol. 13, no. 2, pp. 2526–2535, 2019.
[114] Y. Yang, L. Ding, H. Chen, J. Han, Z. Zhang, and L.-M. Peng, "Carbon nanotube network film-based ring oscillators with sub 10-ns propagation time and their applications in radio-frequency signal transmission," *Nano Res.*, vol. 11, no. 1, pp. 300–310, 2018.
[115] S.-J. Han *et al.*, "High-speed logic integrated circuits with solution-processed self-assembled carbon nanotubes," *Nature Nanotechnol.*, vol. 12, no. 9, pp. 861–865, 2017.
[116] D. Zhong *et al.*, "Gigahertz integrated circuits based on carbon nanotube films," *Nature Electron.*, vol. 1, no. 1, pp. 40–45, 2018.
[117] M. M. Shulaker *et al.*, "Carbon nanotube circuit integration up to sub-20 nm channel lengths," *ACS Nano*, vol. 8, no. 4, pp. 3434–3443, 2014.
[118] Z. Chen *et al.*, "An integrated logic circuit assembled on a single carbon nanotube," *Science*, vol. 311, no. 5768, 2006, Art. no. 1735.
[119] K. Jensen, J. Weldon, H. Garcia, and A. Zettl, "Nanotube radio," *Nano Lett.*, vol. 7, no. 11, pp. 3508–3511, 2007.
[120] C. Rutherglen and P. Burke, "Carbon nanotube radio," *Nano Lett.*, vol. 7, no. 11, pp. 3296–3299, 2007.
[121] I. Amlani, J. Lewis, K. Lee, R. Zhang, J. Deng, and H.-S. P. Wong, "First demonstration of AC gain from a single-walled carbon nanotube common-source amplifier," in *Proc. Int. Electron Devices Meet.*, Dec. 2006, pp. 1–4.
[122] J. Pliva, C. Carta, M. Claus, M. Schroter, and F. Ellinger, "On the design of active downconversion mixers for wireless communications on a carbon nanotube FET technology," in *Proc. SBMO/IEEE MTT-S Int. Microw. Optoelectron. Conf.*, 2011, pp. 984–988.
[123] A. Taghavi, C. Carta, F. Ellinger, M. Haferlach, M. Claus, and M. Schroter, "A CNTFET amplifier with 5.6 dB gain operating at 460–590 MHz," in *Proc. SBMO/IEEE MTT-S Int. Microw. Optoelectron. Conf.*, Nov. 2015, pp. 1–4.
[124] A. Taghavi, C. Carta, T. Meister, F. Ellinger, M. Claus, and M. Schroter, "A CNTFET oscillator at 461 MHz," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 6, pp. 578–580, Jun. 2017.
[125] D. Akinwande, Y. Nishi, and H.-S. P. Wong, "Carbon nanotube quantum capacitance for nonlinear terahertz circuits," *IEEE Trans. Nanotechnol.*, vol. 8, no. 1, pp. 31–36, Jan. 2009.
[126] J. N. Ramos-Silva *et al.*, "High-frequency performance study of CNTFET-based amplifiers," *IEEE Trans. Nanotechnol.*, vol. 19, pp. 284–291, 2020.
[127] J. Tittmann, S. Hermann, S. E. Schulz, A. Pacheco-Sanchez, M. Claus, and M. Schröter, "Hysteresis-free carbon nanotube field-effect transistors without passivation," in *Proc. IEEE/ACM Int. Symp. Nanoscale Architectures*, pp. 137–138, Jul. 2014.
[128] R. S. Park, G. Hills, J. Sohn, S. Mitra, M. M. Shulaker, and H.-S. P. Wong, "Hysteresis-free carbon nanotube field-effect transistors," *ACS Nano*, vol. 11, no. 5, pp. 4785–4791, 2017.
[129] R. S. Park *et al.*, "Hysteresis in carbon nanotube transistors: Measurement and analysis of trap density, energy level, and spatial distribution," *ACS Nano*, vol. 10, no. 4, pp. 4599–4608, 2016.
[130] M. Haferlach *et al.*, "Electrical characterization of emerging transistor technologies: Issues and challenges," *IEEE Trans. Nanotechnol.*, vol. 15, no. 4, pp. 619–626, Jul. 2016.

[131] K. Kita and A. Toriumi, "Intrinsic origin of electric dipoles formed at high-k/SiO_2 interface," in *Proc. IEEE Int. Electron Devices Meet.*, 2008, pp. 1–4.
[132] C. Lau, T. Srimani, M. D. Bishop, G. Hills, and M. M. Shulaker, "Tunable n-type doping of carbon nanotubes through engineered atomic layer deposition HfOX films," *ACS Nano*, vol. 12, no. 11, pp. 10924–10931, 2018.

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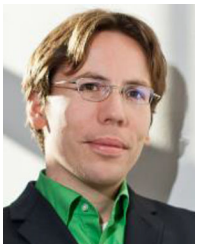

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