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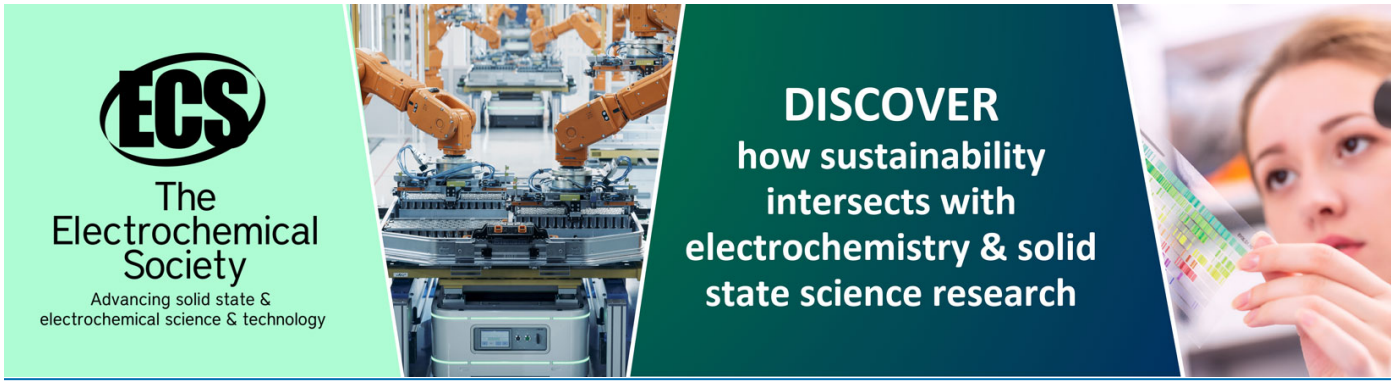

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Mathematical modelling of Bit-Level Architecture using Reciprocal Quantum Logic

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Abstract: Efficiency of high-performance computing is on high demand with both speed and energy efficiency. Reciprocal Quantum Logic (RQL) is one of the technology which will produce high speed and zero static power dissipation. RQL uses AC power supply as input rather than DC input. RQL has three set of basic gates. Series of reciprocal transmission lines are placed in between each gate to avoid loss of power and to achieve high speed. Analytical model of Bit-Level Architecture are done through RQL. Major drawback of reciprocal Quantum Logic is area, because of lack in proper power supply. To achieve proper power supply we need to use splitters which will occupy large area. Distributed arithmetic uses vector- vector multiplication one is constant and other is signed variable and each word performs as a binary number, they rearranged and mixed to form distributed system. Distributed arithmetic is widely used in convolution and high performance computational devices.

1. Introduction

As CMOS technology will get over by 2020 and the Rise of Post Moore law technology will be seeking with low power, high-speed operation. There are many technology which are in development to attain high performance computational devices and low power consumption devices rather using CMOS technology. Over the past two decades CMOS played a vital role in all aspects of computational devices and architectures for many applications in digital and analog worlds. Spintronics, photonics, tunnel junction devices, graphene nano material based devices, superconducting quantum computing devices are forthcoming technology which will overcome moorse law and technology which can work in few 100 GHz frequency speed and can achieve lower power in the range of nanowatts and picowatts. We have chosen superconducting quantum computing based devices, which can work up to 770GHz of speed. We focus our work only on speed rather that area and power. We have taken Reciprocal Quantum Logic (RQL) into consideration to achieve greater speed. The primitive level of logic gates in RQL are AnotB, AndOr, Set-Reset Latch and XOR gates [2]. These gates are designed using Josephson Junction (JJ) and few inductors. RQL uses alternating current rather direct current. For each and every logic design, cryogenic temperature of 10K and below places are required to test the design or samples of superconducting logic. Here we have designed a model using Distributive Arithmetic architecture [7] for RQL based Superconducting logic [8]. In comparison of Superconducting logic over CMOS, the

overall speed and power are far better for designing any logic or Digital Signal Processing architecture's. In Section 2 we have given brief outline about computation logic devices used based on Single Flux Quantum (SFQ), Section 3 consists of DA for RQL and further we have concluded our work with discussing conventional DA based RQL logic.

2. Computational Logic Devices

In early 80's, using Josephson Junction (JJ) and SFQ, a Superconducting quantum logic (RSFQ) has been developed which can work in GHz frequency and picosecond of pulse to complete a task. Rapid Single Flux Quantum (RSFQ) uses cryogenic cooler to reduce the temperature of atmosphere to low temperature superconductors at 4K to test the design. For some application RSFQ have been test with High T_C superconductors. RSFQ consumes more power due to absence of static power analyser. To overcome these condition many logics have been developed like LR based RSFQ, ERSFQ, RQL, and AQFP [2]-[6].

In case of Reciprocal Quantum Logic (RQL) and Adiabatic Quantum Flux Parametron (AQFP), which are modified from RSFQ for energy efficient using AC signal as power input. While in the case of LR-RSFQ and ERSFQ, it is also developed for energy efficient process but it has more static power consumption compared to RQL and AQFP. With the help of multi-phase alternating current signals, RQL gets supplied for both clock and power.

3. Distributive Arithmetic Architecture for RQL

Distributive Arithmetic (DA) are mainly used in designing digital processors due to its huge computational aspects with greater efficiency. Summing of products is the major technique used in DA with the help of inner product computation based on LUT (Look Up Tables) and dot product multiplication. DA comes under Bit-Level serial Architecture which can synthesized using ILP. DA is introduced here to attain area efficient and greater speed. By forming an architecture base on RQL can achieve greater speed as well as area efficient architecture. By considering the conventional DA, the inner product terms will become as follows [1]

$$Z = AX = \sum_{n=0}^{K-1} A_n X_n \qquad (1)$$

Where A is constant and X is coded with bits from 0 to K-1. To design a processor, we need ALU unit, ROM/RAM unit, MAC unit and Control Unit. For ROM unit, just we have to make a LUT with constant A's. For example, if we consider a 8 bit processor, the ROM length (L=8), MAC (M=8) and ALU is formed using 8 bit. To model a DA using bit level serial architecture, we are using equation (1) as base to derive further.

$$Z = \sum_{n=1}^{L} A_n X_n \qquad (2)$$

Where X_n should be less than 1, and it can be re-written as $\{x_{n0}, x_{n1}, x_{n2}, \ldots\ldots, x_{n(M-1)}\}$. Where all variables are 1 bit signed integers.

$$X_n = -x_{n0} + \sum_{m=1}^{M-1} x_{nm} 2^{-m/2} \qquad (3)$$

By substituting (3) in (2), we get

$$Z = -\sum_{n=1}^{L} A_n x_{n0} + \sum_{n=1}^{L} \sum_{m=1}^{M-1} A_n \, x_{nm} 2^{-m/2} \qquad (4)$$

By expanding the equation (4), we get the normalized form of equation

$$\begin{aligned} Z = &-[A_1 x_{10} + A_2 x_{20} + A_3 x_{30} + \cdots + A_L x_{L0}] \\ &+[A_1 x_{11} + A_2 x_{21} + A_3 x_{31} + \cdots + A_L x_{L1}] \cdot 2^{-1/2} \\ &+[A_1 x_{12} + A_2 x_{22} + A_3 x_{32} + \cdots + A_L x_{L2}] \cdot 2^{-2/2} \\ &\vdots \\ &+\left[A_1 x_{1(M-1)} + A_2 x_{2(M-1)} + A_3 x_{3(M-1)} + \cdots + A_L x_{L(M-1)}\right] \cdot 2^{-(M-1)/2} \end{aligned} \qquad (5)$$

With the help of above equation (5), it is clear that it has only 2^L possible values of address can be formed.

4. Conclusion

We have modelled an architecture using distributed arithmetic algorithm by using the Reciprocal Quantum Logic instead of CMOS logic technology. We have formed an equation and LUT to the design and development of RQL. From the above equation it is clear that the architecture requires less area complexity and high speed optimization. With the help of these equation we further develop a processor which can work at ultra-high speed in the range between 150 GHz to 250 GHz. In area optimization, it requires few Josephson Junction (JJ) compared to older architectures.

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