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# Superconducting vanadium/indium-arsenide hybrid nanowires

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#### Superconducting vanadium/indium-arsenide hybrid nanowires

Abstract. We report MBE synthesis of InAs/vanadium hybrid nanowires. The vanadium was deposited without breaking ultra-high vacuum after InAs nanowire growth, minimizing any effect of oxidation and contamination at the interface between the two materials. We investigated four different substrate temperatures during vanadium deposition, ranging from  $-150^{\circ}$ C to  $250^{\circ}$ C. The structural relation between vanadium and InAs depended on the deposition temperature. The three lower temperature depositions gave vanadium shells with a polycrystalline, granular morphology and the highest temperature resulted in vanadium reacting with the InAs nanowire. We fabricated electronic devices from the hybrid nanowires and obtained a high out-of-plane critical magnetic field, exceeding the bulk value for vanadium. However, size effects arising from the nanoscale grains resulted in the absence of a well-defined critical temperature, as well as device-to-device variation in the resistivity vs. temperature dependence during the transition to the superconducting state.

#### 1. Introduction

Growth of III-V semiconductor nanowires offers a rich materials playground due to the ability of the free-standing structures to accommodate lattice mismatch-related strain. This feature in particular enables previously unobtainable material combinations such as Si/Ge [1]. Recently, there has been substantial interest in superconductorsemiconductor nanowires for quantum devices [2]. These nanowires can be used to implement gate tunable superconducting qubits [3] and topological superconducting systems supporting Majorana bound states [4–8]. The new hybrid nanowires are based on a III-V semiconducting core coated with a metallic thin film that is either deposited during device processing [9] or grown directly onto the nanowire facets insitu in the growth chamber [10, 11]. In the latter case, an epitaxial match between the two materials can be achieved as shown for InAs/Al systems grown by Molecular Beam Epitaxy (MBE) under constant ultra-high vacuum (UHV) [10]. Importantly, the clean interface is considered to be the source of "hard" gap superconductivity in the semiconductor due to the superconducting proximity effect [12]. This is the basis for exploiting hybrid nanowires for topologically protected Majorana states that exist within the gap [7,8]. Also, the technique has been extended for planar InAs/Al based heterostructures [13–15]. Turning to other materials, high quality devices have also been obtained by careful *ex-situ* processing of devices based on deposition of e.g. NbTiN on InSb nanowires [9,16]. In-situ MBE growth of Nb on InAs has also been investigated, with evidence of a crystalline interface, but as yet no data on the epitaxy or superconducting properties [11]. The importance of exploring other material combinations is the potential to enhance the superconducting gap, and thereby the critical temperature and field. Larger hard gaps may provide stronger protection of subgap states, and allow spectroscopic transport studies with higher resolution and extended field dependences. Additionally, different material combinations may open

up for new features and functionalities, including higher temperature operation. For a survey of superconducting materials used in hybrid quantum wire devices, see [17].

In bulk, vanadium is superconducting (type II) with a critical temperature,  $T_C = 5.4$  K and critical magnetic field,  $B_c \sim 0.1$  T [18–20] and thus is an interesting candidate towards optimizing the semiconductor-superconductor nanowire platform [16]. Hybrid devices based on III-V nanowires with *ex-situ* e-beam deposited vanadium contacts have previously been used for studies of Andreev bound states [21] and superconducting quantum interference devices (SQUIDs) [22,23]. However, there are no prior reports of *in-situ* integration of III-V nanowire and vanadium thin film growth under UHV conditions and no structural analysis has been reported. Structurally, it is expected that the lattices of vanadium and InAs can match in certain orientations [10, 24], which motivated the current study. One potential challenge we expected was that obtaining monocrystalline growth of vanadium on sapphire by e-beam deposition requires substrate temperatures exceeding 460°C [25]. This temperature regime is incompatible with InAs due to desorption of arsenic at approximately  $400^{\circ}$ C [26].

Here we present a combined analysis of the structural and electronic properties of vanadium deposited on InAs nanowires without breaking ultra high vacuum. The vanadium was deposited at four different temperatures spanning a wide range from liquid nitrogen cooled, up to a temperature where the vanadium alloyed with the InAs. For deposition at substrate temperatures  $-150^{\circ}C < T_{TC} < 100^{\circ}C$ , where  $T_{TC}$ is the temperature measured by a substrate holder thermocouple, we found no clear epitaxial interface match between InAs and vanadium. Instead the vanadium shell consists of polycrystalline grains nucleated with varying orientations related to the InAs facets and governed by the vanadium surface energy. Deposition of vanadium at  $T_{TC} = 250^{\circ}$ C yielded nanowires where the vanadium had reacted with the InAs. The electrical properties of devices fabricated from hybrid InAs/vanadium nanowires were studied at low temperatures. While many devices showed superconducting transitions at T < 4 K we found no clear, consistent  $T_C$  across devices. This may be due to the grain structure effectively giving a random Josephson junction network [27]. The nanoscale superconducting vanadium had a high out-of-plane critical field,  $B_C = 1.8$  T, far exceeding the bulk value [18–20] and that of Al on InAs nanowires [12]. This paper thus provides the first combined structural/electronic study of a hybrid semiconductor nanowire featuring a pristine interface with a superconducting material other than aluminium.

## 2. Nanowire growth and vanadium deposition

The InAs nanowires were grown on InAs (111)B substrates via Au-catalyzed vapourliquid-solid (VLS) growth by MBE. Au was deposited *in-situ* at a thermocouple temperature,  $T_{TC}$ , of 605°C producing Au particles with random diameter (approx. 100 nm) and pitch (approx. 5  $\mu$ m). During growth, the substrate temperature was kept

	$T_{TC}(^{\circ}\mathrm{C})$	t (nm)
S1	-150	19
S2	25	26
S3	25	27*
S4	100	12
S5	250	$\sim 12$

**Table 1.** Overview of vanadium deposition temperatures  $T_{TC}$  (thermocouple) and film thicknesses t for the five InAs nanowire growths S1-S5. Sample marked with \* had an additional 11 nm AlO<sub>x</sub> full shell cap. The film thicknesses were measured from transmission electron micrographs with one of the two vanadium-covered nanowire facets aligned parallel to the electron beam.

constant at  $T_{TC} = 445^{\circ}$ C with a calibrated As<sub>2</sub>/In flux ratio of 15 for 30 minutes and with a projected planar growth rate of  $\sim 0.5$  ML/s. These growth conditions yielded nanowires grown along the [111] direction with typical lengths  $5-8 \ \mu m$  and diameters  $\sim 100$  nm. The nanowires had a predominately wurtzite (WZ) crystal structure with  $(11\overline{2}0)$ , type II facets [28], atypical for InAs nanowires grown under these conditions [29]<sup>‡</sup>. After the axial InAs nanowire growth, the substrate was transferred under UHV to an attached chamber equipped with a cold/hot substrate holder and an electron beam evaporation system [11]. The pressure in the transfer system and metalization chamber was  $P < 10^{-9}$  Torr. The *in-situ* MBE transfer is implemented to not break vacuum in between the axial nanowire growth and radial metalization step in order to minimize contamination and oxidation of the InAs surface. Vanadium was deposited along the  $\{1\overline{1}0\}$  substrate orientation with a rate of ~ 1 Å/s and at an angle of  $28^{\circ}$  with respect to the substrate surface plane. This ensured continuous 2-facet shells on each nanowire, with little to no effects of shadowing from neighboring nanowires, given an average inter-wire pitch above 5  $\mu$ m. Five growths (samples S1-S5) were performed with different vanadium deposition conditions and film thicknesses as shown in Table 1. The substrates were cooled with liquid nitrogen to minimum  $T_{TC} = -150^{\circ}$ C, or heated to maximum  $T_{TC} = 250^{\circ}$ C. We tested different nominal vanadium film thicknesses such that the measured thicknesses ranged from 12-27 nm. In an attempt to protect the vanadium from subsequent oxidation when leaving the MBE system, sample S3 was capped with an 11 nm full shell of amorphous  $AlO_x$ deposited by e-beam evaporation immediately after the vanadium deposition. After the shells were deposited, the samples were left to warm (or cool) to room temperature under vacuum before unloading. Samples were stored in nitrogen, and the time during device processing and transfer to the electron microscopes was minimized as much as practicable.

<sup>‡</sup> We note that after a bake out of the MBE system we now observe type I facets under similar growth conditions. The change between nanowire growth with type I and type II facets is likely related to the presence of Sb in the MBE chamber [30]. We did not deposit vanadium on type I facets.



Figure 1. Structural overview of InAs nanowires coated with vanadium deposited at room temperature (sample S2): (a) Scanning electron micrograph of as-grown InAs/vanadium nanowires. The nanowires are bent towards the vanadium halfshell. Scale bar represents 5  $\mu$ m and the image was acquired with the substrate tilted by  $30^{\circ}$ . (b) Scanning electron micrograph of a single InAs nanowire with vanadium half-shell (false-colored blue). Inset shows a schematic cross-section of the hexagonal InAs nanowire with 2 facet vanadium deposition. Scale bar represents 500 nm and substrate tilt was  $30^{\circ}$ . (c) Transmission Electron micrograph showing vanadium (top laver) on InAs (bottom). Scale bar represents 50 nm. (d) Selected Area Diffraction signal from (c), showing the bi-crystal overlapping of the InAs  $[1\overline{1}00]$ zone axis and vanadium. The arrow indicates the diffraction ring signal from the family of (110) planes of polycrystalline vanadium. Scale bar represents 50 pm<sup>-1</sup>. See Supplementary Information A for enlarged version. (e) High-resolution transmission electron micrograph showing the InAs/V interface. The image was acquired with a vanadium covered nanowire facet aligned parallel to the electron beam (inset). The white arrow indicates the [100] direction in the vanadium, closest to the out-of-plane direction. Scale bar represents 5 nm.

## 3. InAs/V hybrid characterisation

Figures 1(a)-(b) show scanning electron micrographs of hybrid InAs/V nanowires after growth and subsequent vanadium deposition at room temperature (sample S2). The nanowires from the S1-S4 growths bend towards the direction of the vanadium halfshell. In S1-S3, we confirmed that the vanadium shells caused the bending by observing regions on the same growth wafer where the vanadium deposition was shadowed by the substrate holder; the uncoated nanowires remained straight on all 3 growth substrates.

#### Superconducting vanadium/indium-arsenide hybrid nanowires

The bending may be a result of e.g. difference in thermal expansion coefficients between InAs and vanadium or strain in the crystal structure due to interface mismatch [10,31]. As the thermal expansion coefficient of vanadium is larger than that of InAs [18,32], in the case of the cold deposition (S1), the effect from thermal expansion upon returning to room temperature after growth would make the nanowires bend away from the vanadium. Thus, we believe that lattice mismatch at the interface is likely the main contributor to the observed strain.

Insights into the InAs/V interface and overall morphology of the hybrid nanowire crystal were obtained by detailed Transmission Electron Microscopy (TEM) analysis, using a JEOL 3000F microscope operated at 300 kV. For all micrographs in the following, the InAs WZ [1100] zone axis was used for aligning a vanadium covered nanowire facet parallel to the electron beam. An overview of the hybrid structure morphology is illustrated in the low-magnification TEM in Fig. 1(c). The InAs nanowires are crystalline, exhibiting a very low density of stacking faults. The vanadium shell, by contrast, shows an overall polycrystalline, granular morphology. This is also evident in the diffraction signal where no single vanadium-related diffraction pattern is visible. Rather, there is a continuous ring with distinct spots from  $\{110\}$  planes due to a large number of differently oriented grains (see Supplementary A for enlarged version). The film morphology for S1-S3 exhibited a glancing column-like structure (see Supplementary B), similar to that reported for InAs/Nb hybrids in Ref. [11]. The high-resolution TEM (HRTEM) micrograph of the vanadium film shown in Fig. 1(e) exhibits crystal grains with a [100] orientation transverse to the nanowire growth direction. In this region, the crystal direction closest to the facet out-of-plane direction is the [100] direction, indicated by an arrow. The bright and dark regions on the length scale of  $\sim 5$  nm across the image are consistent with the presence of overlapping nanoscale crystalline grains with different orientations. Additionally, the large scale fringes, Moiré fringes, observed in the image are usually signatures of polycrystalline films with translational displacement or rotational variation amongst overlapping grains of the same lattice [33].

The grain sizes, which ranged from 2 nm up to approx. 21 nm – i.e. close to the film thickness – were estimated from 33 HRTEM images and varied with the deposition temperature. The grain structure of vanadium films grown on nanowires is expected to depend on temperature for several reasons. Firstly, the initial stage of growth yields clusters with sizes and spacings that depend on the surface adatom diffusion length, which in turn depends on temperature. For two vanadium depositions on similar nanowire facets with the same deposition rate but at different substrate temperatures, it is expected that the lowest substrate temperature produces the smallest initial average cluster size. The orientation of the individual clusters is determined mainly by the minimization of surface energy, InAs/V interface energy, and strain energy contributions to the overall excess energy. In the subsequent surface driven reconstruction stage a kinetically limited coalescence process can occur. The result is strongly dependent on the initial cluster sizes, the thermodynamical driving forces change as function of shell



Figure 2. Transmission electron micrographs of the InAs/V interfaces from vanadium deposition at various substrate temperatures. ((a),(b)) show examples of the resulting interface when cooling the substrate to  $T_{TC} = -150^{\circ}$ C (S1). ((c),(d)) show examples of the resulting film deposited at room temperature (S2). ((e),(f)) show the result when heating the substrate to 100°C (S4) and 250°C (S5), respectively. In the -150°C–100°C range, the hybrids had regions both with ((a),(c),(e)) and without ((b),(d)) crystalline interfaces. (f) At 250°C the InAs and vanadium reacts. Coloured dots provide a guide to the observed crystal structure. White arrows indicate the locally observed direction closest to the out-of-plane direction. All images were acquired with alignment parallel to an InAs nanowire facet covered by vanadium (i.e. viewing the InAs [1100] zone axis). Scale bars represent 2 nm in ((a)-(e)) and 10 nm in (f).

thickness and an additional re-crystallization of the vanadium film may occur. However, the films investigated here had grain sizes that were smaller than the film thickness. This means that re-crystallization was unlikely to occur, and the variation of film thickness likely had little to no impact on the structural properties. For a full description of the above processes see Ref. [29].

A comparison of the InAs/V interfaces obtained for the 4 different deposition temperatures is given in Figs 2(a)-(f). The colored circles provide a guide to the observed crystal structure and the white arrows indicate the locally observed lowindex direction closest to the out-of-plane direction. Interestingly, the crystalline vanadium grains always grew with particular crystal planes parallel to the  $(1\bar{1}00)$ crystal planes of the nanowire. However, no typical match along the nanowire (0001)

/9

Superconducting vanadium/indium-arsenide hybrid nanowires

planes (i.e. the growth planes) was apparent and therefore also no typical out-of-plane grain growth direction was observed. The planes parallel to the (1100) crystal planes appeared to change with increasing temperature being (111) in the cold deposition S1 (Figs 2((a),(b))) and (100) for S2-S4 (Figs 2((c),(d))). Figs 2((a),(b)) and 2((c),(d))exemplifies the observed variation in out-of-plane direction. Depending on the local grain morphology, the [111] zone axis was also observed in the S2-S4 on rare occasions, but [100] dominated. A common feature to the hybrids from all deposition temperatures in this study is the absence of a coherent crystal lattice match at the InAs/V interface. While some of the crystalline grains did grow from the InAs interface (Figs 2(a), (c), (e)). the most commonly observed growth mode was the initial formation of an amorphous interfacial layer without epitaxial match to the InAs from which crystalline vanadium grains nucleated and grew (Figs 2(b),(d)). Such an amorphous interface morphology is consistent with the ring-formed  $\{110\}$  diffraction signal found in Fig. 1(d). On our nanowires, we observed the most abundant grain sizes (> 65%) in the 6-12 nm range for  $T_{TC} = 25^{\circ}$ C room temperature deposition (S2) while it was 11-17 nm for the cold  $T_{TC} = -150^{\circ}$ C deposition (S1). For deposition at  $T_{TC} = 100^{\circ}$ C (S4), the grain sizes were evenly distributed and ranged from 5-12 nm (i.e. up to the entire film thickness). Depositing vanadium with a substrate temperature of  $T_{TC} = 250^{\circ}$ C (S5) resulted in a reaction between the vanadium and InAs nanowire (see Fig. 2(f)). The nanowires developed indentations where the InAs was replaced by an alloy. From HRTEM analysis we found that this alloy had a face-centered cubic crystal phase with lattice constant  $a = 4.7 \pm 0.1$ . One possible alloy that matches these properties is AsV<sub>3</sub> [34]. However, properly determining the composition of the alloy would require Electron Energy Loss Spectroscopy, Energy-dispersive X-ray Spectroscopy or other x-ray techniques. We did not do an in-depth study of the alloy, since the general morphology shown in supplementary figure C was unsuitable for making semiconductor-superconductor hybrid devices. Further we expect that the alloying is determined mainly by the substrate temperature and will occur regardless of film thickness. Therefore, we did not perform any more depositions at  $T_{TC} = 250^{\circ}$ C.

## 4. Electrical properties of InAs/V hybrids

The superconducting properties of the InAs/V hybrids were studied using four terminal devices such as that shown in Fig. 3(a). Device fabrication proceeded by transferring selected nanowires from the growth substrate to a substrate consisting of highly doped Si with a SiO<sub>2</sub> overlayer. Ti/Au contacts were defined by electron beam lithography and e-beam evaporation. Evaporation was preceded by *in-situ* Ar<sup>+</sup> milling to remove the native oxide and ensure ohmic contact. The resistance was measured in a dilution refrigerator using phase sensitive ac lock-in techniques with the circuit shown in Fig. 3(a). A constant ac current was sourced along the nanowire, and the voltage drop between the two inner contacts measured. Contacting the nanowire device in this way was aimed at determining how the crystal structure and morphology impacted

#### Superconducting vanadium/indium-arsenide hybrid nanowires

the electrical properties of the vanadium. With the four-terminal geometry, we cannot study properties of the InAs itself since the metallic vanadium film will short out any possible conduction pathway through the InAs. We return to possible implications for this after presenting the results. Device dimensions used for the resistivity calculation were measured from scanning electron micrographs of each device.

Resistivity,  $\rho$ , as a function of temperature for two representative devices is shown in Fig. 3(b). Red and blue data points are from different devices fabricated from S3 and S1, respectively, with the vanadium deposited at  $T_{TC} = \text{RT}$  and  $T_{TC} = -150^{\circ}\text{C}$ . Each device exhibited a transition from the normal ( $\rho = 4 - 6 \times 10^{-4} \Omega$ m) to superconducting phase ( $\rho = 0$ ). However, neither device exhibited a clear, single transition with a well defined critical temperature. Rather, the transition of these and all other measured devices was gradual and no two devices behaved identically. Additionally, 4 of the 10 measured devices showed no zero resistance state at base temperature of the cryostat  $(T \sim 20 \text{ mK})$ . Since the hybrids from growth S3 were coated in AlO<sub>x</sub>, and therefore protected from oxidation, we can likely exclude the formation of vanadium oxide as the major reason many devices did not show superconductivity. Note also that we expect the resist used for electron beam lithography to protect the nanowires during device processing, minimizing the exposure to oxygen. Instead, the observed behaviour could be explained by the grain structure observed in Figs 1 and 2. Obtaining a single, well-defined  $T_C$  in polycrystalline superconductors relies on effective proximitization of the insulating grain boundaries to form a series of Josephson junctions [35, 36]. This was clearly not achieved for the vanadium films studied here and we therefore propose the following possible explanation. For vanadium, size effects lower  $T_C$  as grain size is reduced [25,37], and thus each grain is expected to undergo a superconducting transition at a different temperature. The smallest grains may not turn superconducting at all due to the Anderson criterion [38]. Naturally, observing a zero resistance superconducting state cannot occur if portions of the nanowire remain in the normal state, either due to a small grain size or poor proximitization of the grain boundaries. Additionally, the particular  $\rho$  vs. T behavior would strongly depend on the exact grain configuration in the measured segment. The behavior observed in Fig. 3(b) is consistent with this picture, and the range of the transition region (T = 1 - 4 K) is similar to previous reports of the size-related  $T_C$  variation in vanadium thin films [25, 37]. Note that thin, two dimensional films of vanadium with a similar granular structure are more likely to exhibit bulk-like superconducting properties, including a clear critical temperature. This is because the additional dimension increases the likelihood of forming a percolating pathway between superconducting grains. The reduced dimensionality of our quasi-1D nanowires limits this possibility, hence obtaining much more variable results between devices. One possibility for obtaining a higher number of superconducting devices would be to increase film thickness to be much greater than the grain size (t >> 20 nm), although this may further increase the nanowire bending for much thicker films.

Fig. 3(c) shows the response to a magnetic field applied perpendicular to the substrate, as illustrated in Fig. 3(a). As expected, the value of  $B_C \sim 1.8$  T





Figure 3. (a) False-color scanning electron micrograph of a four terminal InAs/V device with Ti/Au ohmic contacts (yellow) to the vanadium (blue). Scalebar represents 2  $\mu$ m. (b) Resistivity  $\rho$  vs. temperature T showing superconducting transitions for two example devices, one with RT vanadium deposition (red) and the other with a cooled substrate holder  $T_{TC} = -150^{\circ}$ C (blue). (c) Resistivity vs. out-of-plane magnetic field for the RT InAs/V device.

exceeds the reported bulk value [19, 20, 39] due to the nanoscale morphology of the films. We expect even larger critical fields for *B* applied parallel to the nanowire. Importantly, the perpendicular critical field is far greater than that reported for aluminium covered InAs nanowires [12], which is highly desirable in applications towards topological superconductivity [4, 7], superconducting qubits [3, 40] and fundamental physics [21,41,42]. Exploring these applications would require the vanadium to reliably and consistently induce superconductivity into the InAs. This could be determined using experiments on tunnel probe devices [12]. However, the fact that we do not observe a clear, consistent critical temperature strongly suggests that our films would not be a suitable material for reliably obtaining induced superconductivity in the InAs. It may be of interest in future works if further optimization of the vanadium is performed.

## 5. Conclusions

In conclusion, we have studied the structural and superconducting properties of vanadium shells on InAs nanowires, motivated by a desire to understand the possibilities for forming high quality bi-crystal interfaces with materials beyond aluminium and form hybrid electronic devices based on these. To do so, we deposited the vanadium at a wide range of temperatures, from liquid nitrogen cooled,  $T_{TC} \approx -150^{\circ}$ C to above the point where the two materials formed an alloy, at  $T_{TC} = 250^{\circ}$ C. Deposition at temperatures  $-150^{\circ}$ C  $\leq T_{TC} \leq 100^{\circ}$ C favoured growth of grains where the vanadium (100) or (111) planes grew parallel with the underlying InAs nanowire crystal (110) planes.

#### Superconducting vanadium/indium-arsenide hybrid nanowires

However, a typical bi-crystal interfacial match was not found along the axial direction, limiting the potential for large-scale epitaxy between the two materials. Rather, the vanadium films consisted of polycrystalline grains with diameters 2-21 nm. The wide variety of grain sizes dominated the electrical behaviour of devices fabricated from these growths. In some, but not all cases, the nanowire hybrids turned superconducting at cryogenic temperatures, and exhibited a higher critical magnetic field than aluminiumbased hybrids with similar film thickness. The gradual nature of the transition to the superconducting state and the device-to-device variation is consistent with the films consisting of a large number of small grains with varying size. This is because the critical temperature of each grain is expected to decrease with decreasing grain size [35]. Observation of an induced superconducting gap in future hybrids will likely depend on achieving films with a well-defined, macroscopic  $T_{\rm C}$ . This encourages further optimisation towards entirely crystalline, epitaxially matched vanadium/semiconductor hybrids. Doing so would likely involve substrate temperatures between 100°C and 250°C during vanadium deposition to promote formation of larger crystalline grains, which may exhibit a more well-defined collective  $T_C$ . Deposition at such temperatures naturally would require a different semiconductor nanowire material, since we found alloying occurred for  $T_{TC} = 250^{\circ}$ C. Alternatively, other semiconductor materials may have more favourable surface energy configurations for vanadium growth at lower temperatures. Finally, an intermediate crystalline layer could be grown on the InAs prior to vanadium deposition, such that an epitaxial match would be possible between each layer.

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Superconducting vanadium/indium-arsenide hybrid nanowires

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Superconducting vanadium/indium-arsenide hybrid nanowires

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Superconducting vanadium/indium-arsenide hybrid nanowires

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