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Bipolar effects in unipolar junctionless transistors

Mukta Singh Parihar,[1] Dipankar Ghosh,[1] G. Alastair Armstrong,[2] Ran Yu,[3] Pedram Razavi,[3] and Abhinav Kranti[1,a)]
[1]*Low Power Nanoelectronics Research Group, Electrical Engineering Discipline, Indian Institute of Technology (IIT), Indore 452017, India*
[2]*School of Electronics, Electrical Engineering and Computer Science, Queen's University Belfast, Belfast BT9 5AH, United Kingdom*
[3]*Tyndall National Institute, University College Cork, Cork, Ireland*

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In this work, we analyze hysteresis and bipolar effects in unipolar junctionless transistors. A change in subthreshold drain current by 5 orders of magnitude is demonstrated at a drain voltage of 2.25 V in silicon junctionless transistor. Contrary to the conventional theory, increasing gate oxide thickness results in (i) a reduction of subthreshold slope (*S*-slope) and (ii) an increase in drain current, due to bipolar effects. The high sensitivity to film thickness in junctionless devices will be most crucial factor in achieving steep transition from ON to OFF state. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4748909]

Scaling down of conventional metal–oxide–semiconductor (MOS) transistors into the nanoscale regime is being hindered due to several technological and process issues.[1] One such parameter limiting the downscaling is the abruptness of source/drain (S/D) junctions as it impacts short channel effects and parasitic series resistance.[1,2] To overcome the technological difficulties in the formation of ultra-steep S/D profiles, the concept of the junctionless (JNL) MOS transistor in silicon-on-insulator (SOI) and bulk technologies has been proposed.[2–4] As the channel doping is the same as that of the S/D regions in JNL devices, the need for steep S/D profile is alleviated. As shown in Figure 1, JNL metal-oxide-semiconductor field effect transistor (MOSFET) is a unipolar device as it is doped with only one type of impurity. The performance of JNL transistors, like inversion mode devices, is degraded by short channel effects which result in increasing the subthreshold slope (*S*-slope). A lower *S*-slope is desirable as it governs the transition from OFF to ON state. It has been demonstrated[5,6] that *S*-slope can further be reduced from 60 mV/decade in MOSFETs by impact ionization phenomenon. Indeed somewhat surprisingly, JNL devices exhibit higher impact ionization rate, and the length over which impact ionization takes place is also larger in JNL MOSFETs as compared to inversion mode (INV) devices.[5]

In order to evaluate bipolar effects, JNL and undoped INV mode double gate (DG) MOSFETs with same subthreshold characteristics were simulated with ATLAS simulation software[7] using the Lombardi mobility model[8] and including modules for doping, bipolar, and impact ionization effects. JNL MOSFETs with gate length (L_g) of 50 nm with a width of 1 μm were analyzed with silicon film thickness (T_{si}) varying from 6 nm to 10 nm and oxide thickness (T_{ox}) from 0.8 nm to 2.4 nm. In JNL device, doping concentration (N_d) was fixed at 10^{19} cm^{-3} and drain bias (V_{ds}) was varied from 1.5 V to 2.25 V. Figures 2(a)–2(d) show the hysteresis effect in I_{ds}–V_{ds} characteristics (forward and backward sweep mode) in JNL devices. INV mode devices do not exhibit hysteresis phenomena for the same gate and drain voltages, and device parameters mentioned in the figure. This simulation depicts a change of 5 orders of magnitude in drain current with an *S*-slope <1 mV/decade at $V_{ds} = 2.25$ V for silicon transistors. The hysteresis window (ΔV), being directly proportional to the number of decades of transition in the drain current, i.e., steepness of I_{ds}–V_{gs} curve at the transition voltage, increases from 8 mV at $V_{ds} = 1.75$ V to about 163 mV for $V_{ds} = 2.25$ V. While sweeping in forward direction, at a particular gate voltage, the carriers gain sufficient energy to start impact ionization[14] and the avalanche chain mechanism increases the carrier density leading to steep *S*-slope and sharp increment in drain current. Due to impact ionization, a large number of electron–hole pairs are generated in the silicon film. The generated electrons contribute to the drain current while holes accumulate at the minimum potential region. The consecutive accumulation of holes forward biases the source-channel (p-type accumulated region) hence enhancing the drain current due to a virtual bipolar mechanism. The high drain current again increases avalanche multiplication leading to the generation of electron–hole pairs. This positive feedback mechanism actuates the parasitic "bipolar" effect in parallel, resulting in the sharp increase of drain current.[9–19] In the reverse sweep mode, i.e.,

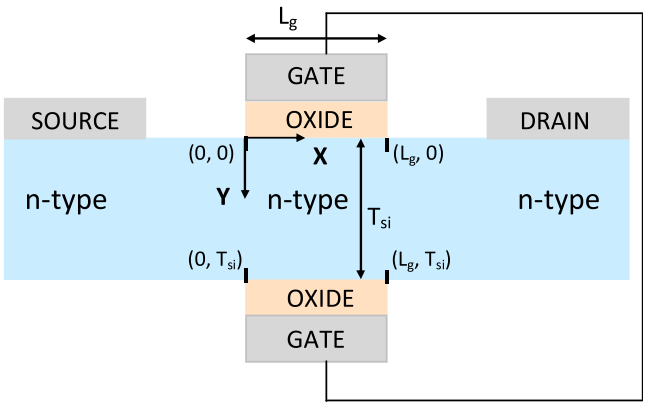

FIG. 1. Schematic diagram of a DG SOI JNL MOSFET.

a)Author to whom correspondence should be addressed. Electronic mail: akranti@iiti.ac.in.

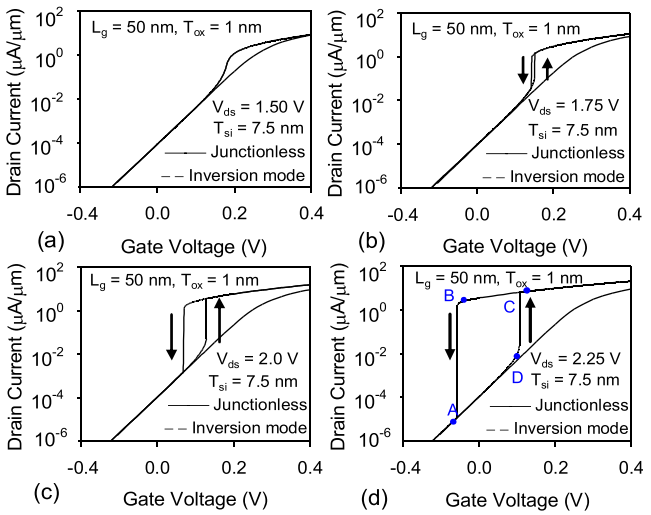

FIG. 2. Dependence of drain current on gate voltage in JNL and INV mode devices at (a) $V_{ds} = 1.50$ V, (b) $V_{ds} = 1.75$ V, (c) $V_{ds} = 2.00$ V, and (d) $V_{ds} = 2.25$ V. Points B and A represent the gate voltage just before and after steep transition in reverse sweep, respectively, whereas points D and C correspond to gate bias just before and after steep transition in forward sweep, respectively. Voltages corresponding to points A, B, C, and D marked in (d) are −0.055 V, −0.065, 0.110, and 0.100 V, respectively.

reducing gate voltage, larger negative voltage is required to overcome the effect of feedback loop and additional drain current, which results in the hysteresis effect.

In order to understand hysteresis effect in JNL devices, potential distribution, electron, and hole concentration, along a cut-line (shown in Fig. 3(a)) from $x = L_g/2$, $y = 0$ to $x = L_g/2$, $y = T_{si}$, have been extracted for four structures corresponding to bias points A, B, C, and D marked in Fig. 2(d). As shown in Figs. 3(b) and 3(c), the potential distribution and electron concentration are maximum at the centre of the film as compared to the surface. Conversely, the hole concentration is higher at the surface rather than at the centre of the film (Fig. 3(d)). In classical bulk MOSFETs, holes generated due to impact ionization move towards the substrate region which is at minimum potential. However, in DG JNL devices, electrons flows through the center of the film ($y = T_{si}/2$) and holes move to the surface as it is the region of minimum potential (Fig. 3(b)). Although, both electrons and holes are generated due to impact ionization, the voltage applied at the gate causes electrons to deplete for gate voltages below the steep transition of drain current, while holes accumulate at the surface as they cannot flow through the oxide. This can cause the surface hole concentration to be greater than maximum electron concentration at the centre, i.e., for points A and D (shown in Fig. 2(d)). For V_{gs} above the steep drain current transition (i.e., points B and C in Fig. 2(d)), electron concentration at centre is higher than hole concentration, whereas, at surface, hole concentration is higher (Figs. 3(c) and 3(d)). Progressive accumulation increases the concentration of holes at the surface to a level $>10^{19}$ cm^{-3}. The potential, electron, and hole concentrations are highest for point C (in comparison to A, B, and D) as it corresponds to voltage where the number of electrons and holes, generated due to impact ionization, are maximum.

The sensitivity of steep S-slope on device parameters (T_{ox} and T_{si}) is shown in Figs. 4(a)–4(c). As shown in Fig. 4(b), for the same off-current ($I_{off} = I_{ds}$ at $V_{gs} = 0$ V), an increase in T_{ox} results in an increase in the on-current ($I_{on} = I_{ds}$ at $V_{gs} = 0.2$ V). This increase is contrary to the conventional scaling theory and is only possible due to the additional current component because of bipolar effects in JNL devices. An impressive I_{on}/I_{off} of five orders of magnitude can be achieved for T_{ox} lying between the range 1.2 nm to 2.4 nm at $V_{gs} = 0.2$ V. For a device with $T_{ox} = 0.8$ nm, the steep S-slope is obtained at $V_{gs} = 0.215$ V (Fig. 4(a)). An increase in T_{ox} shifts the threshold voltage in the negative direction and all other devices achieve the steep transition below 0.2 V resulting in the saturation of I_{on}/I_{off} ratio for $T_{ox} > 1.2$ nm. The rate of change of threshold voltage (V_{th}) with oxide thickness ($\Delta V_{th}/\Delta T_{ox}$) is $\geq$60 mV/nm for steep S-slope JNL devices. V_{th} is taken to be the gate voltage corresponding to the steep increase of drain current.

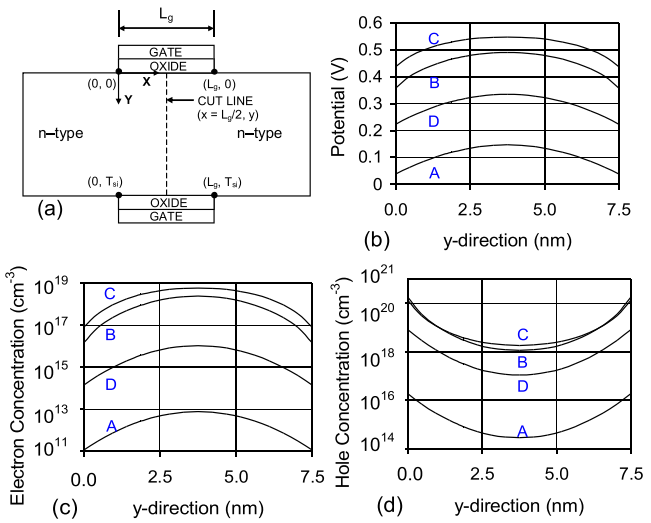

FIG. 3. (a) Position of cut-plane for the evaluation of (b) potential distribution, (c) electron concentration, and (d) hole concentration in junctionless devices at bias voltages corresponding to points A, B, C, and D shown in Figure 2(d). Device parameters are same as in Figure 2.

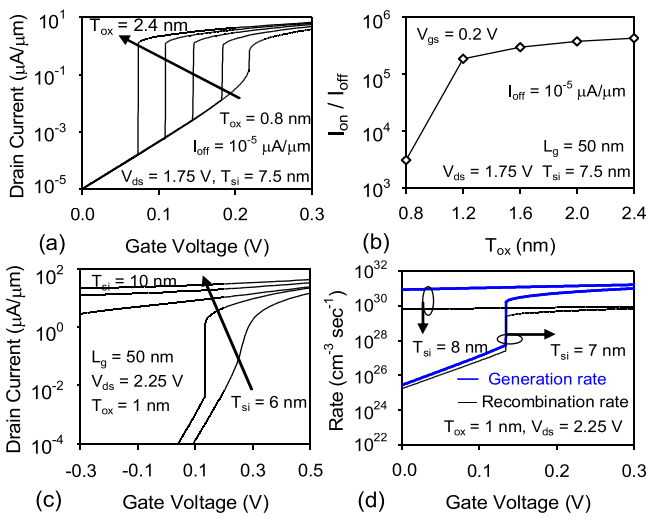

FIG. 4. (a) Dependence of drain current on gate voltage for various values of gate oxide, (b) on–off current ratio (I_{on}/I_{off}) as a function of gate oxide thickness, (c) drain current–gate voltage graph for various film thickness values, and (d) generation and recombination rates as a function of gate voltage (V_{gs}).

JNL devices exhibiting steep *S*-slope are also extremely sensitive to film thickness as an increment of 1 nm at $T_{si} = 6$ nm can introduce a significant shift in the threshold voltage ($\Delta V_{th}/\Delta T_{si} \geq 160$ mV/nm) and *S*-slope (26 mV/decade to 0.5 mV/decade). As shown in Fig. 4(c), increasing the film thickness from 6 nm to 7 nm improves the number of decades of change in drain current at the transition gate voltage as it results in an increased impact ionization, which leads to excess carrier generation. The electrons have to be depleted to turn OFF the device. An additional negative voltage is required for the same and hence a reduction threshold voltage is observed leading to a progressive shifting of the I_{ds}–V_{gs} characteristics in the direction of lower gate voltages (Fig. 4(c)).

An increase in T_{si}, i.e., from 7 nm to 8 nm results in the condition that the transistor latches to the ON state and does not turn OFF. The reason for device turning OFF at $T_{si} = 7$ nm and the latching to the ON state for $T_{si} \geq 8$ nm can be understood with Fig. 4(d). At higher gate voltages (above the steep drain current transition), a constant difference between generation and recombination (G–R) rates is observed for $T_{si} = 7$ nm and 8 nm. Before the steep transition, the magnitude and difference between G–R rates decreases for $T_{si} = 7$ nm, while for $T_{si} = 8$ nm both rates maintain a constant magnitude and difference over the entire reverse sweep of gate voltage. At $T_{si} = 7$ nm, generated electrons can be depleted at the transition gate voltage leading to the device being turned OFF. This is also reflected in the reduction in G–R rates which are broadly in agreement at lower gate voltages. The holes generated by impact ionization, if possible, recombine with electrons and overall current remains low. For film thickness $\geq$8 nm, more number of carriers are generated (indicated by higher magnitude of G–R rates) in the reverse gate bias sweep, which cannot be depleted by the applied gate voltage. This results in the device being latched to the ON state. The constant difference in G–R rates is observed (i) beyond the sharp increase in drain current and (ii) when the device is unable to turn OFF. This constant difference between G–R rates for $T_{si} = 8$ nm (over entire V_{gs} range) is the indicative of enhanced drain current (unable to turn OFF) due to high concentration of generated electron–hole pairs caused by impact ionization. The level of impact ionization at which the generation rate has a significant effect on current is of the order of 10^{28} cm^{-3}s^{-1}. The balance between generation and recombination is crucial in what is essentially the "base" of an equivalent bipolar transistor under extremely high injection conditions and no base contact. This phenomenon of transistor not being able to turn off has been previously reported and analyzed for fully and partially depleted INV devices operating at high drain bias[15,16,18,19] but not for JNL devices. The higher sensitivity of steep *S*-slope junctionless MOSFET on film and oxide thickness coupled with the challenge of fabrication of high quality defect free thin mono-crystalline silicon film imposes severe limitations on the usefulness of the steep *S*-slope junctionless transistor. The crucial challenge in the fabrication of JNL transistors will be to control film thickness within $\pm$0.5 nm of the optimal value to achieve the benefit of steep switching from OFF to ON state and avoiding the two extremes:

(i) *S*-slope close to 60 mV/decade (theoretical minimum at room temperature) and
(ii) Device latching on to the ON state and failing to turn OFF.

This sensitive dependence on film thickness is expected to be valid for channel materials like germanium where steep *S*-slope is expected to be observed at lower V_{ds} (in comparison to Silicon) due to lower energy bandgap (0.7 eV).

In conclusion, bipolar effects appear to be more severe in unipolar junctionless devices. It is possible to achieve a change of 5 decades in subthreshold drain current due to impact ionization in junctionless devices. However, the most crucial challenge for junctionless devices benefitting from steep *S*-slope at lower voltages will be the control of silicon film thickness. Bipolar effects in junctionless transistors lead to anomalous increase in drain current for thicker gate oxides and the reduction of *S*-slope with increase in gate oxide and film thickness (within a certain range).

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[1]I. Ferain, C. A. Colinge, and J.-P. Colinge, Nature (London) **479**, 310 (2011).
[2]J.-P. Colinge, C.-W. Lee, A. Afzalian, N. Dehdashti Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, and R. Murphy, Nat. Nanotechnol. **5**, 225 (2010).
[3]A. Kranti, R. Yan, C.-W. Lee, I. Ferain, R. Yu, N. D. Akhavan, P. Razavi, and J.-P. Colinge, in *Proc. European Solid State Device Research Conference (ESSDERC)* (2010), p. 357.
[4]A. Kranti, C.-W. Lee, I. Ferain, R. Yan, N. Akhavan, P. Razavi, R. Yu, G. A. Armstrong, and J.-P. Colinge, Electron. Lett. **46**, 1491 (2010).
[5]C.-W. Lee, A. N. Nazarov, I. Ferain, N. Akhavan, R. Yan, P. Razavi, R. Yu, R. T. Doria, and J.-P. Colinge, Appl. Phys. Lett. **96**, 102106 (2010).
[6]R. Yu, S. Das, I. Ferain, P. Razavi, N. Akhavan, C. A. Colinge, and J.-P. Colinge, in *Proc. Workshop of the Thematic Network on Silicon on Insulator technology, devices and circuits (EuroSOI)* (2012), p. 37.
[7]ATLAS Users Manual, Silvaco.
[8]C. Lombardi, S. Manzini, A. Saporito, and M. Vanzi, IEEE Trans. Comput.-Aided Des. **7**, 1154 (1992).
[9]J. R. Davis, A. E. Glaccum, K. Reeson, and P. L. F. Hemment, IEEE Electron Device Lett. **7**, 570 (1986).
[10]M. A. Pavanello, J. A. Martino, and D. Flandre, Solid-State Electron. **44**, 917 (2000).
[11]B. Y. Mao, R. Sundaresan, C. E. D. Chen, M. Matloubian, and G. P. Pollack, IEEE Trans. Electron Devices **35**, 629 (1988).
[12]E.-H. Toh, G. H. Wang, L. Chan, G. Samudra, and Y.-C. Yeo, Semicond. Sci. Technol. **23**, 015012 (2008).
[13]K. E. Moselund, D. Bouvet, V. Pott, C. Meinen, M. Kayal, and A. M. Ionescu, Solid-State Electron. **52**, 1336 (2008).
[14]B. Eittan, D. Frohman-Bentckowsky, and J. Shappir, J. Appl. Phys. **53**, 1244 (1982).
[15]A. Boudou and B. S. Doyle, IEEE Electron Device Lett. **8**, 300 (1987).
[16]C.-E. D. Chen, M. Matloubian, R. Sundaresan, B.-Y. Mao, C. C. Wei, and G. P. Pollack, IEEE Electron Device Lett. **9**, 636 (1988).
[17]P. S. Liu and G. T. Liu, J. Appl. Phys. **74**, 1410 (1993).
[18]G. A. Armstrong and W. D. French, in *Proc. IEEE SOI Conference* (1991), p. 46.
[19]G. A. Armstrong and W. D. French, Microelectron. Eng. **22**, 375 (1993).