Capacitance switching in SiO_2 thin film embedded with Ge nanocrystals caused by ultraviolet illumination

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A structure of indium tin oxide/SiO_2 embedded with Ge nanocrystal (nc-Ge)/*p*-Si substrate was fabricated. The capacitance of the structure can be switched to a high-capacitance or low-capacitance state by an ultraviolet (UV) illumination. The increase (or decrease) in the capacitance is accompanied with the decrease (or increase) in the oxide resistance. The capacitance switching is explained in terms of the UV illumination-induced charging and discharging in the nc-Ge. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3224191]

Ge nanocrystals (nc-Ge) embedded in SiO_2 have recently received enormous interest for the potential applications in nonvolatile memory (NVM) devices[1–4] and optoelectronic devices.[5–10] By replacing the conventional polysilicon floating gate with the nc-Ge acting as isolated charge traps, a new type of NVM with fast program and erase speed, long data retention time, and good endurance has been demonstrated.[1] The observations of visible photoluminescence[5–7] and electroluminescence[8–10] from the SiO_2 films embedded with nc-Ge have also opened up a new possibility to fabricate the light-emitting devices compatible to the mainstream silicon technology. Ion implantation is a promising technique to synthesize nc-Ge in the gate oxide of a metal-oxide-semiconductor structure because of its good control over the nc-Ge distribution and the full compatibility with the Si technology.[10] Recently, the conduction modulation induced by ultraviolet (UV) illumination in the gate oxide embedded with nc-Ge was reported.[11] In this work, we report the capacitance switching in the oxide embedded with nc-Ge induced by UV illumination.

A 30-nm-thick SiO_2 film was thermally grown on *p*-type (100) Si wafer by dry oxidation at 950 °C. The SiO_2 film was then implanted with a dose of 2×10^{15} cm^{-2} Ge ions at the energy of 6 keV. Based on the stopping and range of ions in matter simulation, the distribution of implanted Ge ions extends from the oxide surface to a depth of ~20 nm with a Ge concentration peak at a depth of ~10 nm. A postimplantation annealing was carried out in the N_2 ambient at 800 °C for 1 h. The formation of nc-Ge in the SiO_2 matrix is confirmed by the cross-sectional transmission electron microscopy image, which has been reported in our previous work.[11] Afterward, a 130-nm-thick layer of indium tin oxide (ITO) was deposited onto the thin film with a pad diameter of 1.2 mm. The ITO film serves as a semitransparent gate electrode which allows for penetration of UV light through the gate electrode. The wafer backside was coated with 1 μm Al backside contact. The dc resistance measurements were conducted with a Keithley-4200 semiconductor characterization system. The capacitance-voltage (*C-V*) and time-domain capacitance measurements were performed with an HP4284 *LCR* meter at a frequency of 1 MHz. All the electrical measurements were carried out at room temperature. The wavelength used for the UV illumination is 365 nm, and it was provided by an Oriel-66011 arc lamp together with an Oriel-77250 monochromator.

In Fig. 1, the comparison between the *C-V* characteristics before and after the UV illumination for 5 s is shown. The *C-V* measurement was performed in a voltage range of −4 to 0 V in order to avoid the charging/discharging effect caused by the measurement itself. The repeated *C-V* measurements before the UV illumination show no significant change in the capacitance, indicating that no significant charging or discharging occurred during the measurement. After the UV illumination for 5 s, it can be observed that the accumulation capacitance was dropped drastically from a high-capacitance state of ~350 pF to a low-capacitance state of ~250 pF. On the other hand, the effect of UV illumination on the dc resistance of the oxide layer for the elec-

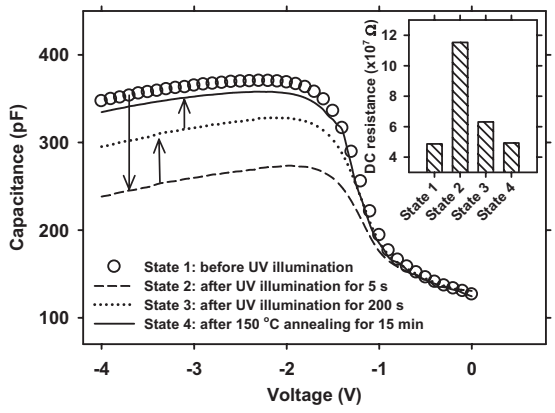

FIG. 1. Reduction in the capacitance from state 1 to state 2 caused by the UV illumination for 5 s, and recoveries in the capacitance from state 2 to state 3 after a second UV illumination and to state 4 after a further low-temperature annealing at 150 °C for 15 min. The inset shows the corresponding dc resistance of the oxide layer for the electron current from the Si substrate measured at +4 V for each state.

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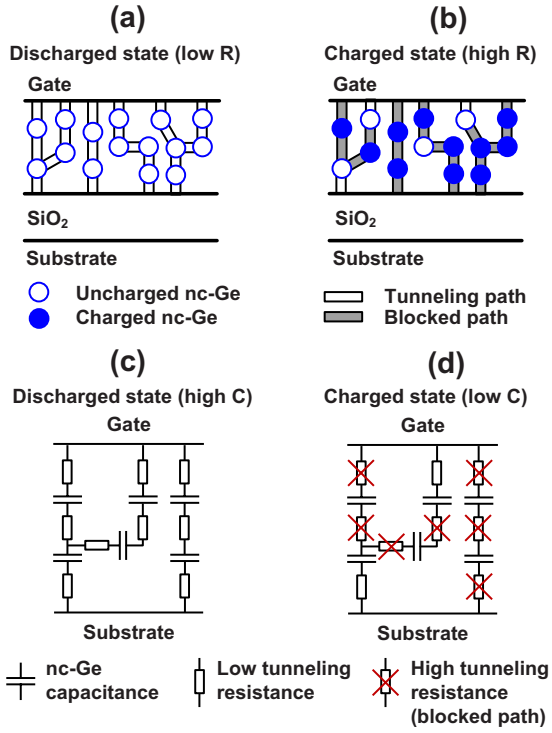

FIG. 2. (Color online) (a) Schematic of the formation of tunneling paths by uncharged nc-Ge for the low-resistance state (i.e., the discharged state); (b) blockade in the tunneling paths due to electron trapping in nc-Ge for the high-resistance state (i.e., the charged state); and circuit representation of the (c) discharged state and (d) the charged state.

tron current from the Si substrate was also measured at 4 V. The measurement voltage was sufficiently low such that there was no significant charging/discharging effect caused by the measurement itself. As shown in the inset of Fig. 1, after the UV illumination of 5 s, the dc resistance was increased by more than 50%. The results indicate that the reduction in the oxide capacitance and the increase in the dc resistance happened simultaneously after the UV illumination of 5 s.

The increase in the resistance (i.e., decrease in the dc conductance of the gate oxide for the electron current) can be explained in terms of the breaking of some tunneling paths for electron transport in the oxide due to electron trapping in some nc-Ge caused by the UV illumination.[11] Electron tunneling (and/or other conduction mechanisms) can take place between adjacent uncharged nanocrystals, and a large number of such nanocrystals in the oxide can form many conductive tunneling paths, which significantly reduce the resistance of the oxide for the electron current from the Si substrate under a positive gate voltage. The effects of charging and discharging in the nc-Ge on the resistance are illustrated in Figs. 2(a) and 2(b), respectively. Before UV illumination, most of the nc-Ge are uncharged, and thus many tunneling paths are formed, leading to a low resistance of the oxide, as shown in Fig. 2(a). However, if the sample is exposed to UV light, some of the electrons generated by the UV illumination can be trapped in the nc-Ge. As a result of the charging in the nc-Ge, the tunneling paths related to the charged nc-Ge could be blocked due to the Coulomb blockade effect, leading to an increase in the resistance, as shown in Fig. 2(b). As a nc-Ge is located at a random position, the formation of tunneling paths could be described with a percolation theory, similarly to the situation of tunneling paths of neutral oxide traps generated by electrical stress in SiO_2 thin films.[12]

The reduction in the oxide capacitance can be attributed to the increase in the oxide resistance due to the charge trapping in nc-Ge caused by the UV illumination, as explained in the following. An uncharged nc-Ge acts as a capacitor as electrons can move into or out of it via tunneling or other mechanisms under the influence of external electric fields. Therefore, a single nc-Ge can be represented with the nc-Ge capacitance together with the tunneling resistance, which describes the difficulty level for electrons moving into the nc-Ge, as depicted in Fig. 2(c). Thus, the networks of the conductive paths formed by the uncharged nc-Ge shown in Fig. 2(a) can be modeled by the RC networks of the nc-Ge capacitance and the tunneling resistance shown in Fig. 2(c). The Al gate and the Si substrate are electrically connected by the RC networks. The tunneling resistance is low when the nc-Ge is uncharged; however, it is high when the nc-Ge is charged with electrons because it is difficult for electrons to move into the nc-Ge due to the Coulomb interaction with the trapped electrons. When most of the nc-Ge are uncharged (we call it "discharged state"), the oxide resistance is low, and thus the nc-Ge capacitors can respond to the small ac signal applied to the gate. As a result, the measured capacitance of the oxide is high while the total oxide resistance is low. On the other hand, when most of nc-Ge are charged up (we call it "charged state"), as shown in Fig. 2(d), most of the tunneling paths are blocked by the trapped electrons (i.e., the tunneling resistance is high), and the nc-Ge capacitors cannot respond to the small ac signal. Thus, the measured capacitance is small while the oxide resistance is high.

When the sample is exposed to the UV illumination, some of the electrons generated by the UV illumination could be trapped in the nc-Ge; however, at the same time, the UV illumination could also cause the release of the trapped electrons from the nc-Ge. Charging and discharging in the nc-Ge due to UV illumination are two competing processes which occur simultaneously. If the charging process is dominant, the oxide resistance is increased while the capacitance is reduced; however, if the discharging effect is dominant, the oxide resistance is reduced while the capacitance is increased. Both of these two situations have been observed in our experiment. As shown in Fig. 1, an UV illumination for 5 s can lead to a large decrease in the accumulation capacitance. However, a further UV illumination for 200 s can result in a partial recovery in the oxide capacitance, i.e., the oxide capacitance was increased as compared to the situation after the 5 s illumination. This indicates that some of the electrons trapped in the nc-Ge due to the first UV illumination were released after the second UV illumination. The oxide resistance as shown in the inset of Fig. 1 also demonstrates the partial recovery after the UV illumination of 200 s. On the other hand, the oxide capacitance and resistance can recover almost to the level of the virgin situation (i.e., before the UV illumination) after a low-temperature annealing at 150 °C for 15 min in addition to the UV illumination for 200 s. This suggests that almost all the charges trapped in the nc-Ge were released after the operation of the second UV illumination plus the low-temperature annealing.

The phenomenon that the oxide capacitance can be changed by UV illumination and low-temperature annealing could be used in optoelectronic memory device applications, where information can be stored as a high-capacitance or

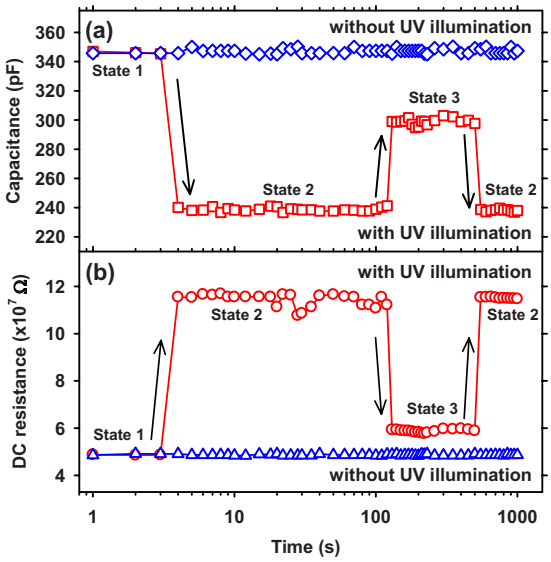

FIG. 3. (Color online) (a) Time-domain measurements of the capacitance at −4 V (b) and the dc resistance at 4 V with and without the UV illumination.

low-capacitance state. For example, an optoelectronic write-once-read-many-times memory could be realized based on the phenomenon. The memory could be programmed with the UV illumination and erased with a low-temperature annealing.

As mentioned above, the charging and discharging of nc-Ge could occur simultaneously under the UV illumination. This suggests that a switching in both the capacitance and resistance could be observed in time-domain measurement under the UV illumination at a constant voltage. This is confirmed in our experiment. Figure 3 shows the time-domain capacitance and dc resistance measurements with and without the UV illumination. Without the UV illumination, no significant changes in both the capacitance and the resistance can be observed in Fig. 3, indicating that no significant charging or discharging in nc-Ge occurred during the measurement. However, both the capacitance and resistance showed switching among different states under the exposure of UV light. As shown in Fig. 3(a), after the UV illumination for 4 s, the oxide capacitance was reduced significantly from a high-capacitance state (state 1) to a low-capacitance state (state 2). State 1 represents a discharged state while state 2 represents a charged state. State 2 was maintained for about 120 s under the UV illumination. Then the oxide was switched to another state (state 3) with a capacitance much larger than that of state 2 but slightly lower than that of state 1. This indicates that not all of the trapped charges associated with state 2 have been released, and thus only a partial recovery of the capacitance could be achieved. State 3 was maintained for about 370 s, and then the oxide was switched back to state 2 due to the charging of nc-Ge caused by the UV illumination. A resistance switching corresponding to the capacitance switching can also be observed, as shown in Fig. 3(b). As discussed earlier, the capacitance switching was just a consequence of the resistance switching. If the timescale is extended, switching between different states can be observed continuously. It should be pointed out that the amount of the trapped charges and the trapping sites are not necessarily the same for every switching since the charge trapping and detrapping are random processes. Therefore, the switching in both the capacitance and the resistance is a random event. However, for a fresh device, a short UV illumination tends to reduce the capacitance.

In conclusion, the capacitance switching of the gate oxide embedded with nc-Ge induced by UV illumination has been reported. The oxide could be switched to a lower-capacitance or higher-capacitance state by the UV illumination, which corresponds to a higher-resistance or lower-resistance state of the gate oxide, respectively. The switching in both the capacitance and the resistance is attributed to the charging and discharging in the nc-Ge caused by the UV illumination.

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