# A pentacene-based organic thin film memory transistor

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(Received 18 March 2009; accepted 7 April 2009; published online 27 April 2009)

An organic memory device based on a pentacene thin film transistor is demonstrated. Gold nanoparticles have been used as the charge storage elements while a thin film of polymethylmethacrylate formed the gate insulator. The electrical characteristics and the memory behavior of the organic thin film memory transistor (OTFMT) are reported. Under an appropriate gate bias (1 s pulses), the gold nanoparticles are charged and discharged, resulting in significant threshold voltage shifts of the OTFMT. The detailed programing and erasing procedures are reported. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3126021]

Research in organic electronics is now leading to advances in many electronic and optoelectronic devices. Applications such as light emitting displays,[1] solid state lighting,[2] organic solar cells,[3] sensors,[4] and organic thin film transistors (OTFTs)[5] are the focus of intense study. Such devices have attracted both academic and industrial researchers due to their low cost, low temperature processing, and mechanical flexibility. There is now a growing interest in organic memory devices, which can combine the property of nonvolatility with high speed, high density, low power, and low cost. Organic memory devices exploiting bistable switching[6] and based on charge storage in metal-insulator-semiconductor structures (MIS)[7–9] and organic thin film memory transistors (OTFMTs)[10] have been reported. The development of reliable and robust OTFMTs is an important goal because of the nondestructive write/erase processes. The main approach to fabricate such devices has been to introduce charge traps by means of nanoparticles[11] or nanocrystals[12] embedded within the gate insulator of the transistors.

The memory transistors reported to date generally use hybrid silicon-organic structures, with $SiO_2$ as a tunneling oxide and an organic insulator as the control dielectric.[11–14] Here, we report the properties of pentacene-based OTFMTs using polymethylmethacrylate (PMMA) as the insulator. We have shown that the pentacene/PMMA organic semiconductor/insulator combination leads to good transistor devices, with little hysteresis in either their transfer or output characteristics.[15] Gold nanoparticles, deposited by a self-assembly process at room temperature, are used as the charge storage elements.

The following materials were purchased from Sigma-Aldrich: (3-aminopropyl)-trimethoxysilane (APTMS), PMMA (molecular weight 93 000) and pentacene. The preparation of the gold nanoparticle solution has been described previously.[8] The devices, depicted schematically in Fig. 1, were fabricated by first thermally evaporating an Al bottom gate electrode (100 nm thickness) through a shadow mask onto a clean glass substrate. A 150 nm thick insulating layer was formed by spin coating an anisole (methoxybenzene, obtained from MicroChem) solution of PMMA on top of the gate electrode. This was cured at 120 °C for 1 h. The PMMA solution concentration and spin coating speed were 5 wt % and 5000 rpm, respectively. To deposit the Au nanoparticles, the glass substrates were placed in a dilute solution of APTMS (0.1 ml of APTMS in 1 ml methanol) for about 4 h before rinsing with methanol. The substrates were subsequently immersed in the Au solution for 20 min and were again rinsed with water. Pentacene was thermally evaporated at a pressure of $7.5\times10^{-7}$ mbar, at a rate of 0.05–0.1 nm $s^{-1}$, through a shadow mask to a thickness of 30 nm. Following deposition of the pentacene, the source and drain contacts were defined by thermal evaporation of 30 nm of Au through a shadow mask (the channel width $W$ to length $L$ ratio was 80, $L=50$ $\mu$m and $W=4000$ $\mu$m). Control devices without the nanoparticles were also fabricated. Double sweep current $I$ versus voltage $V$ characteristics of the transistors were recorded at room temperature ($21\pm2$ °C) using a Keithley 485 picoammeter and 2400 source meter.

Figure 2 shows (a) the dependence of drain-source current $I_{DS}$ on the drain-source voltage $V_{DS}$ (OTFT output characteristics) and (b) the dependence of $I_{DS}$ on the gate-source voltage $V_{GS}$ (transfer characteristics) for the OTFMT and the control OTFT devices. In each measurement, both forward and reverse scans are shown, at a voltage scan rate of 1 V $s^{-1}$. The $V_{GS}$ value was −30 V for the output characteristics and $V_{DS}$ was set at −30 V for the transfer characteris-

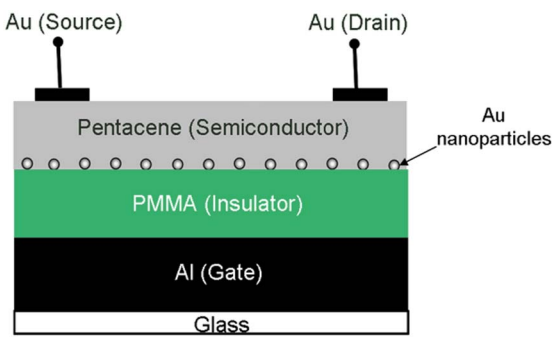


FIG. 1. (Color online) Schematic diagram of the pentacene-based OTFMT with a PMMA gate dielectric.

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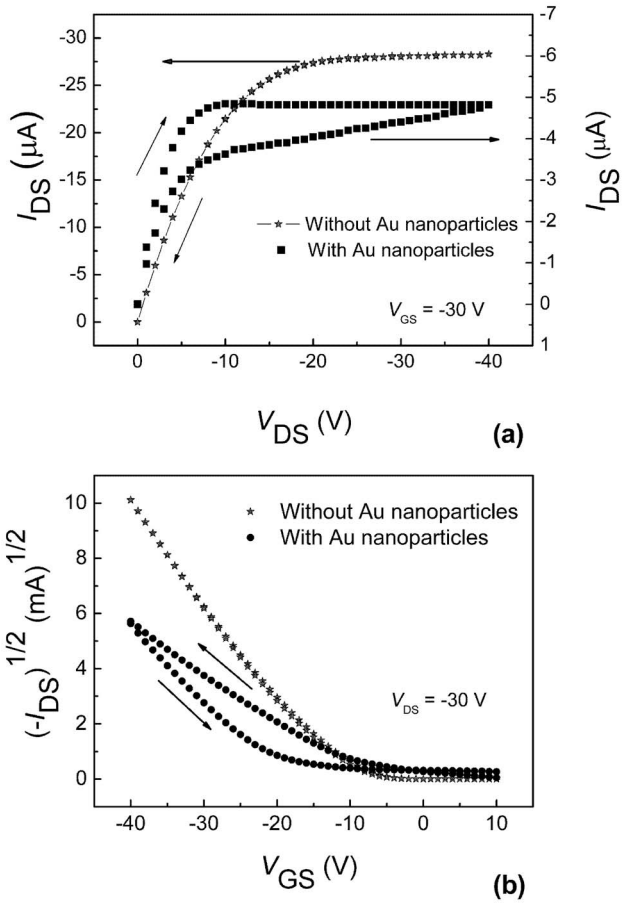


FIG. 2. The output characteristics of the memory transistor with and without gold nanoparticles. (b) Transfer characteristics of the memory device with and without gold nanoparticles.

tics. All the devices (with and without nanoparticles) exhibited typical transistor behavior. Holes accumulate at the pentacene surface when a large negative voltage is applied to the gate, and a high source-drain voltage results in saturation of $I_{DS}$ as the conductive channel becomes pinched off. The field effect mobility $\mu$ of the devices can be estimated from[5]

$$I_{DS} = \frac{\mu W C_i}{2L}(V_{GS} - V_T)^2, \quad (1)$$

where $C_i$ is the insulator capacitance per unit area and $V_T$ is the threshold voltage. The threshold voltage represents the value of the $V_{GS}$ at which the transistor is turned on and can be determined from the intercept of a plot of $(I_{DS})^{1/2}$ versus $V_{GS}$ as in [Fig. 2(b)]. The calculated value of $\mu$ for the control OTFT devices was 0.2 $cm^2 V^{-1} s^{-1}$, similar to our previously reported figures.[15] In contrast, the OTFMTs (containing nanoparticles) possess lower mobility values ($0.05-0.1$ $cm^2 V^{-1} s^{-1}$). This suggests that the presence of the gold nanoparticles adjacent to the pentacene surface has affected the current flow in the transistor channel. More significantly, the addition of the nanoparticles produces a distinct hysteresis in both the output and transfer characteristics of the transistor. It is important to note that the forward and reverse output and transfer characteristics scans for the control device are almost superimposed in Fig. 2. Since the control devices have the same processing procedure as the devices containing gold nanoparticles, the hysteresis in the OTFMTs is attributed to the presence of the nanoparticles and is almost certainly the result of their charging and discharging with the applied voltage. These results are consistent with our recent capacitance $C$ versus voltage $V$ studies of pentacene/PMMA devices, in which hysteresis in the $C$-$V$ curves was attributed to the presence of nanoparticles at the semiconductor/insulator interface.[16]

The counterclockwise hysteresis direction of the transfer characteristics in Fig. 2(b) indicates that charging and discharging of the memory transistor take place through the pentacene surface. When a negative gate bias is applied, holes are injected from the pentacene layer into the nanoparticles layer, charging up the latter and programing the memory device. In contrast, when a positive gate voltage is applied, holes are ejected from the nanoparticle layer through the pentacene layer resulting in an erase process. The injection/ejection of charges into/from the nanoparticles layer will lead to a shift in the transistor threshold voltage $V_T$; this represents the memory window of our OTFMT. When a large negative voltage is applied to the gate electrode (negative pulse), holes are transferred from the channel to the gold nanoparticle layer through the semiconductor. This charging process generates an internal electric field in the opposite direction to the applied negative voltage. As a consequence, a higher negative gate voltage is required to turn on the transistor, resulting in a shift in the threshold voltage to a more negative value compared to the unstressed device. This corresponds to the "write" state. Similarly, when a large positive voltage is applied to the gate electrode (positive pulse), the holes stored in the gold nanoparticles are ejected into the transistor channel. A smaller negative gate voltage is then needed to turn on the transistor. This situation corresponds to the "erase" state.

Accordingly, to test the memory properties of our OTFMTs, successive positive and negative voltage pulses were applied on the gate electrode with $V_{DS}$ maintained at 0 V. The magnitude of the voltage pulse was increased for each step but the pulse duration was kept at 1 s. At each stage, and after the application of the voltage pulse, the transfer characteristics of the device were measured to calculate the shift in the threshold voltage compared to the unstressed device. Figure 3(a) shows the dependence of threshold voltage shift, $\Delta V_T$, on the height of the applied voltage pulses. The device characteristics in Fig. 3(a) exhibit a clear memory window for voltage pulses over 20 V. The amount of charge stored in the nanoparticles $Q$ can be estimated from $Q = C_i \Delta V_T$, where $C_i$ was measured using a simple pentacene/PMMA MIS structure. This gives a value of $3.75 \times 10^{-10}$ F $m^{-2}$; thus, the number of charge carriers stored is approximately $5 \times 10^9$ $cm^{-2}$ for a programing voltage of 30 V.

Figure 3(b) shows the effect of programing pulses on the value of $I_{DS}$ when a voltage was applied to the gate electrode. The write state was achieved by the application of a voltage pulse of $-30$ V for 1 s while, for the erase state, a voltage pulse of 30 V was used with the same period of time. When a gate voltage of 10 V was applied, it was possible to distinguish if the device was in the write or erase state from the value of the drain-source current, evident from Fig. 3(b). The nonvolatile behavior of the OTFMT was investigated by monitoring the drain-source current after the application of voltage pulses for write and erase states. The $I_{DS}$ was periodically measured at regular time intervals; a fixed gate voltage of 10 V was used as the reading voltage. Figure 4 reveals

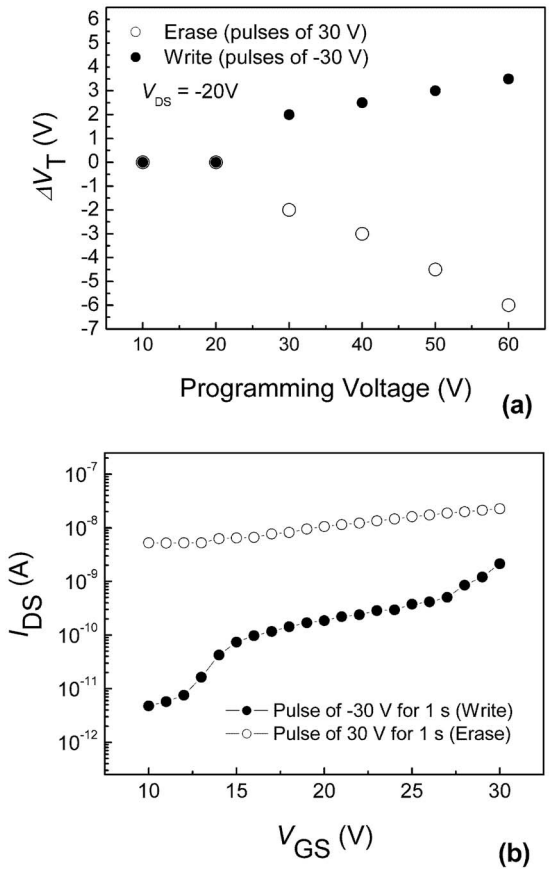


FIG. 3. Programing characteristics of the pentacene-based OTFMT. (a) The effect of the programing voltage (1 s pulses) on the threshold voltage shift, $\Delta V_T$. (b) Write and erase processes by applying a negative and positive pulse voltage, respectively.

that the memory charge is retained for at least 3 h. The memory behavior was, in fact, retained for at least 6 months in the case of devices stored under vacuum. However, under normal laboratory conditions, the device lifetime was less than 1 day.

In summary, we have demonstrated an organic memory device based on a pentacene/PMMA thin film transistor and using self-assembled gold nanoparticles as charge storage elements. Using appropriate voltage pulses applied to the gate electrode, the nanoparticles may be charged and discharged, resulting in shifts in the device threshold voltage and changes in the channel current. Furthermore, the memory devices exhibited good charge retention properties for devices stored in vacuum. The results augur well for the development of all-organic signal processing circuitry.

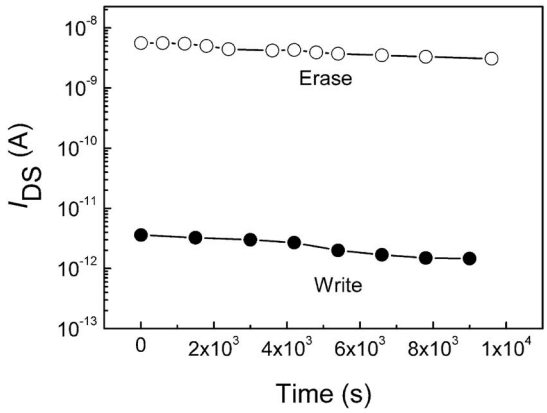


FIG. 4. Charge retention characteristics of the pentacene-based OTFMT.

We would like to thank the Science and Engineering Research Council for funding this work (Grant No. EP/D039924/1). Y.Y. would also like to thank the School of Engineering, Durham University for the provision of a studentship.

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