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## Fabrication of Buried Co-Planar Metal-Insulator-Metal Nanojunctions with a Gap Lower than 10 nm

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**Résumé.** — Un procédé de fabrication est proposé pour obtenir des nanojonctions métal-insulant-métal co-planaires d'une largeur d'isolant bien inférieure à 10 nm en utilisant un masqueur électronique à 20 keV et un "lift-off" à l'or-palladium. Les électrodes de la nanojonction enterrées dans la silice ont une largeur de moins de 100 nm et sont distantes de 8 nm. En optimisant l'étape de sous gravure, il est possible de conserver de la silice comme isolant entre les électrodes.

**Abstract.** — An improvement of a process to fabricate co-planar metal-insulator-metal nanojunctions is presented to reach a gap length much lower than 10 nm using a 20 keV e-beam and an AuPd lift-off. The electrodes of the nanojunction are less than 100 nm in width and are buried in the SiO<sub>2</sub> substrate. For the 8 nm nanojunctions, the gap is still filled with SiO<sub>2</sub> if care is taken about the SiO<sub>2</sub> etching step of the process.

### 1. Introduction

To measure the electrical resistance of a molecular wire, this molecule must be a jumper over a Metal-Insulator-Metal (MIM) junction. There are at least three requirements for such a junction. (a) The separation between the metallic electrodes must be small enough to accommodate the state of the art oligomer length i.e. between 5 to 10 nm [1]. (b) The molecule jumping over the gap and adsorbed by its ends to the electrodes has to be imaged to detect its presence and orientation without destruction. (c) The electrodes section must be small enough to minimize the direct tunnel current between the electrodes compared to the one through the molecular wire.

(a) and (c) can be fulfilled using modern electron beam nanolithography [2, 3]. But (b) is more difficult to address. One popular, and in principle non destructive way to image a single molecule on a surface, is the Scanning Tunneling (STM) or the Atomic Force (AFM) Microscope [4]. For such techniques, the insulating gap between the two electrodes must be filled with some material to planarize the surface. In that way, the AFM or STM tip scanning on the surface of the gap will not be perturbed by the border of the electrodes because of its

finite radius. Furthermore, the insulating surface of the gap must be flat enough to be able to image the molecule grafted on the nanojunction.

There are two ways to fabricate a co-planar MIM nanojunction with a filled gap: bury the electrodes in the surface of an insulating material or grow some insulating material in the gap between the electrodes already fabricated on the substrate with a standard nanolithography process [2,3]. We have shown recently that 30 nm buried MIM co-planar nanojunctions can be fabricated using an e-beam nanolithography process [5]. In these nanojunctions, the surface of the SiO<sub>2</sub> gap was imaged with an AFM, and the surface corrugation was less than 1 nm [6]. We present here a new fabrication process which results in gaps well below 10 nm which are still buried metallic electrodes.

## 2. From 30 nm to 10 nm Gaps

A pixel jump technique was used to fabricate 30 nm buried co-planar MIM junctions using an e-beam lithography lift-off process [5]. The junction was made, during the e-beam exposure, by stopping the exposure over a distance (measured in pixels length) larger than the e-beam spot diameter. The smaller gaps were obtained by adjusting the electron dose with the polymethylmethacrylate (PMMA) resist development time to play with proximity effects [5]. To bury the electrodes, the SiO<sub>2</sub> substrate was etched after the PMMA resist development.

The 30 nm gaps were fabricated using a pixel length of 18.75 nm corresponding approximately to our effective 20 nm e-beam spot diameter [5]. A simple way to reduce the distance between the two electrodes of the nanojunction is to use the smallest possible pixel length available on our standard Thomson EPG 102 electron pattern generator. For a 12.5 nm pixel length, the result is presented in Figure 1. Well defined nanojunctions were fabricated down to a gap of 20 nm in length using the process optimized for a 18.75 nm pixel length [5]. The only difference was the number of pixels jumped: between 6 to 8 compared to 3 and 4 for a 18.75 nm pixel length. Notice that for the nanojunction presented in Figure 1, the metallization height was chosen in such a way that the SiO<sub>2</sub> in the gap is easily scanned over with an AFM, as shown in Figure 1b. After optimization, the yield of the process was approximately 20% for a standard deviation of 20 nm. This large deviation may be attributed to the difficulties of having an homogeneous SiO<sub>2</sub> etching rate in the vicinity of the SiO<sub>2</sub> gap protected by the PMMA. Often, the SiO<sub>2</sub> in the gap between the electrodes is cut as shown in Figure 2.

For the 6.25 nm smallest possible pixel length available on the standard EPG 102, a 10 nm gap size is reached as shown in Figure 3. But this length is too small compared to the interferometry stabilization of the EPG 102 which is limited to a 40 nm precision, enabling this to be achieved reproducibly. In these processes, we have also tried to adjust the metallization in such a way that the electrodes are at the same level as the SiO<sub>2</sub> surface in the gap.

## 3. Fabrication of Gaps Below 10 nm

To be able to fabricate gaps below 10 nm in a reproducible manner, we have first worked on the EPG 102. The optics and the electronics of the interferometer were modified to reach a 3 nm stabilization precision [7]. Furthermore, we have decreased the gain of the *x* and *y* e-beam scanning control units to reach a 3 nm minimum pixel length. One negative consequence of such a reduction is that the pixel length is now smaller than the e-beam diameter leading to a large over-exposure of the PMMA resist if our standard process is used [5]. Therefore, a new process was optimized to take advantage of the stabilized EPG 102.

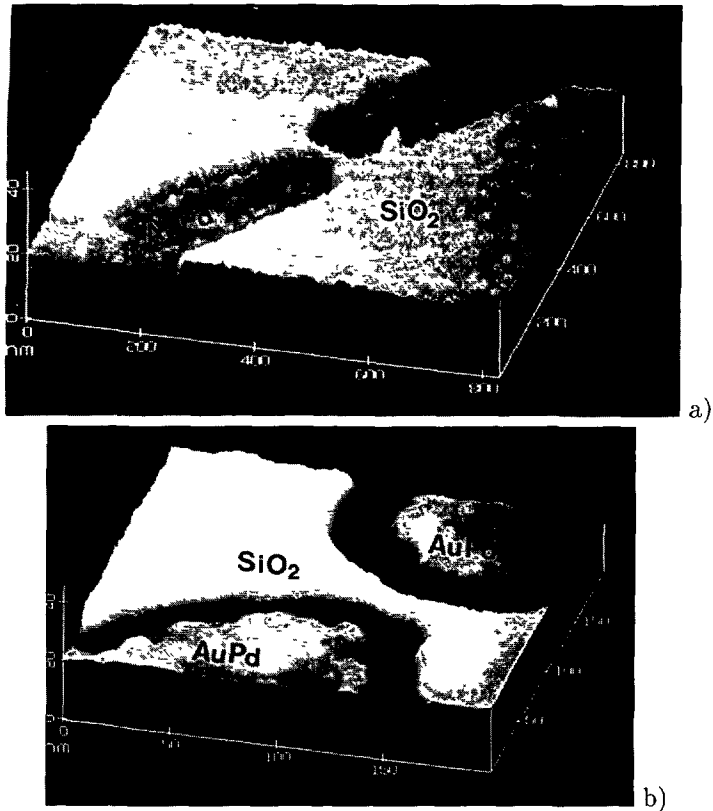


Fig. 1. — a) A 3D view AFM constant force image of a 20 nm gap in a 100 nm in width AuPd wire. The image size is  $0.8 \times 0.8 \mu\text{m}^2$ . The metal is recessed by 4 nm in the SiO<sub>2</sub> surface giving a clear access to the SiO<sub>2</sub> surface in the gap. b) A 3D view AFM constant force image of a smaller scan in Figure 1a nanojunction. The image size is  $0.2 \times 0.2 \mu\text{m}^2$ .

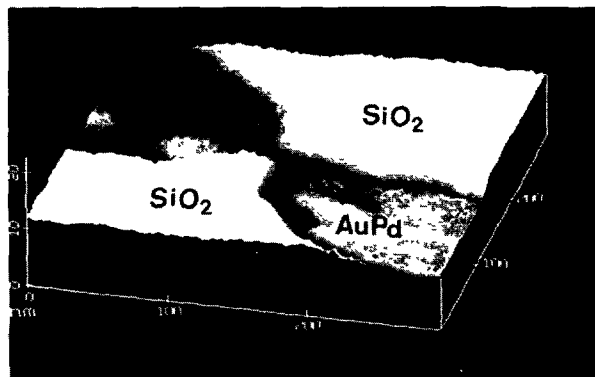


Fig. 2. — A 3D view AFM constant force image of a 20 nm gap where the SiO<sub>2</sub> in the gap was cut by the HF etching. The junction is still there, but there is no longer flat surface in the gap. The image size is  $0.3 \times 0.3 \mu\text{m}^2$ .

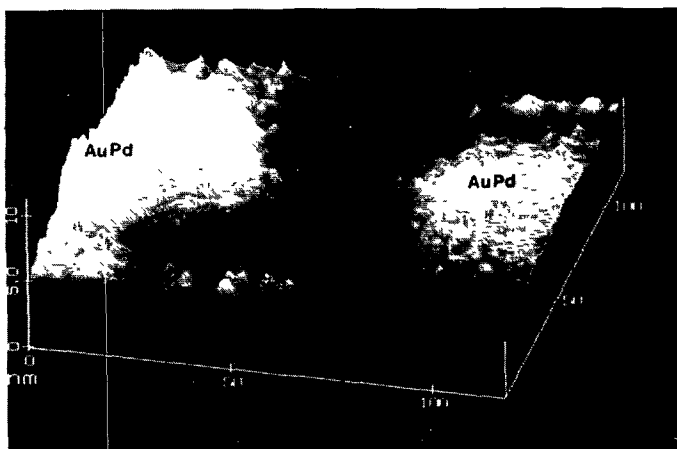


Fig. 3. — A 3D view AFM constant force image of a 10 nm gap. The  $\text{SiO}_2$  in the gap is still there. The two pads of the junction are 2.5 nm higher compared to the  $\text{SiO}_2$  substrate. The image size is  $0.12 \times 0.12 \mu\text{m}^2$ .

A PMMA resist layer, 50 nm in thickness, is spin coated on a Si(100) wafer on which 100 nm of  $\text{SiO}_2$  has been thermally grown. The wafer is then baked for 90 s at 150 °C. For the exposure of this resist, the scanning frequency of the 20 keV e-beam is 300 kHz with a 30 pA beam current and a 20 nm effective e-beam diameter [5]. This gives a dose of  $31.8 \mu\text{C}/\text{cm}^2$ . This dose is four times smaller than in our previous process [6]. Each pattern is  $41 \mu\text{m}$  long and  $2 \mu\text{m}$  in width. In the middle, there is a  $1 \mu\text{m}$  long and less than 100 nm in width wire. The gap is fabricated in the middle of the wire. A single e-beam scan is used to expose this wire. Since the elementary pixel length is now 3 nm, the writing field reduces to a  $12.0 \times 12.0 \mu\text{m}^2$  square divided in  $4000 \times 4000$  pixels. This means that the  $41 \mu\text{m}$  long pattern must be exposed using five fields instead of one. Due to the increase in stability of the EPG 102, there is however no problem of mismatching between these fields over the whole wafer.

After the exposure, the PMMA is developed with a methylethylketone diluted in ethanol solution for 12 s. The temperature of the solution is held at 19 °C. This short development duration is optimized to compensate pixel overlapping during the exposure of the 100 nm central wire. The exposure of the  $2 \mu\text{m}$  large pads is also realized by exposing only one scan over six to limit the overexposure because the beam diameter is larger than the scanning increment. Then, the wafer is rinsed in an isopropanol solution.

After the development, the  $\text{SiO}_2$  is etched for 90 s using a HF solution held at 20 °C. This etching time has been reduced compared to the standard process [5] to avoid the cut of the  $\text{SiO}_2$  in the gap as shown in Figure 2. Finally, 10 nm of AuPd is evaporated on the wafer and lifted off.

The number of pixel jumps in the middle of the exposure of the 100 nm wire was varied between 12 and 25. Taking into account the e-beam diameter, a jump of 15 pixels of 3 nm each is at the limit of a gap fabrication. The first gaps appear for a jump of at least 20 pixels. Their length is lower than 10 nm as shown in Figure 4. But the yield of the process is small, around 5%, corresponding to 8 successful nanojunctions for a fabrication of 150 junctions. For a jump of 25 pixels, the fabricated gaps are comparable in length with the one obtained using a 12.5 nm pixel length with a jump of 6 to 8 pixels (Fig. 1) with the standard process [5].

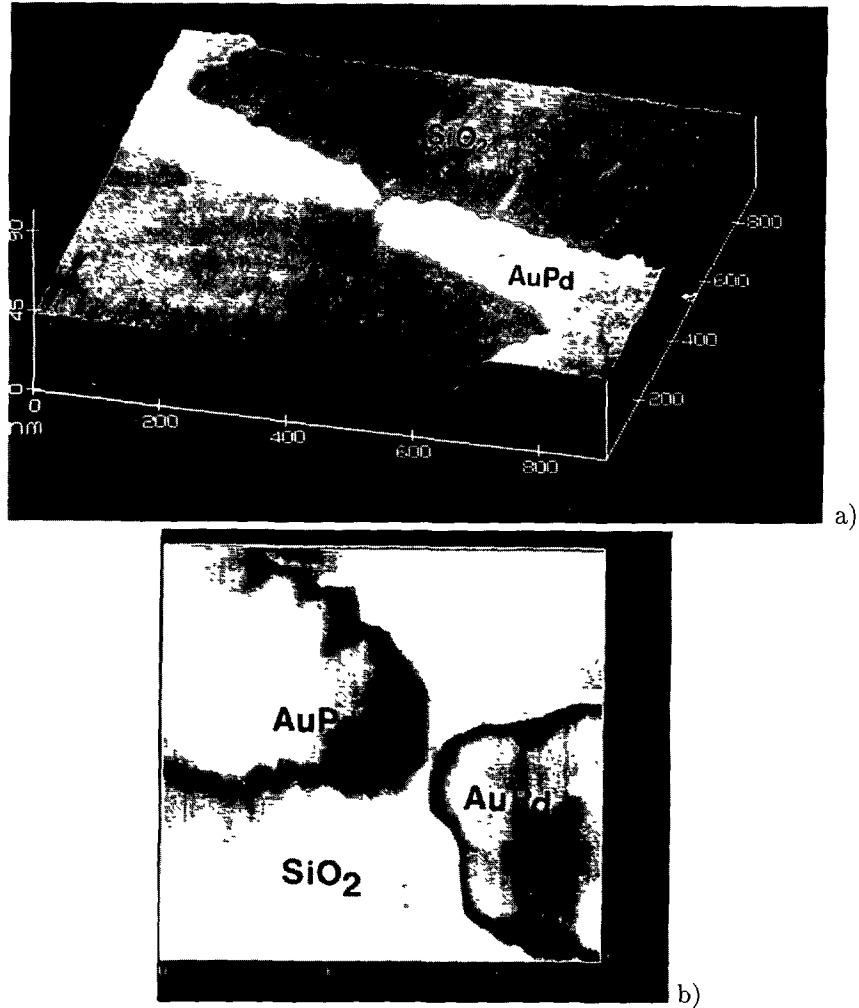


Fig. 4. — a) A 3D view AFM constant force image of a 8 nm gap where there is still SiO<sub>2</sub> in the gap. The two electrodes of the nanojunction are higher by 4.5 nm compared to the SiO<sub>2</sub> substrate. The end of the 2 μm in width pads is also imaged. The image size is 0.9 × 0.9 μm<sup>2</sup>. b) A top view of a smaller scan in Figure 4a nanojunction. The end of each electrode is clearly delimited creating a nanojunction with a 8 nm distance between its electrodes. The image size is 0.25 × 0.25 μm<sup>2</sup>.

The small yield may be attributed to the easy diffusion of the SiO<sub>2</sub> etching solution which destabilizes the PMMA resist protecting SiO<sub>2</sub> in the gap. Due to the minimal 2 nm diameter of the PMMA molecular size [3], one needs a length of at least, two or three times this diameter to stabilize the PMMA in the gap of the nanojunction.

The AFM characterization of the 8 nm nanojunction in Figure 4 shows that the electrodes are not totally buried in the SiO<sub>2</sub> layer. There is a 4.5 nm height difference between the top of the electrodes and the SiO<sub>2</sub> surface. This is due to the small HF etching duration chosen to protect SiO<sub>2</sub> in the gap. If a standard 120 s etching time is used, the electrodes are buried but there is no SiO<sub>2</sub> in the gap as shown in Figure 5.

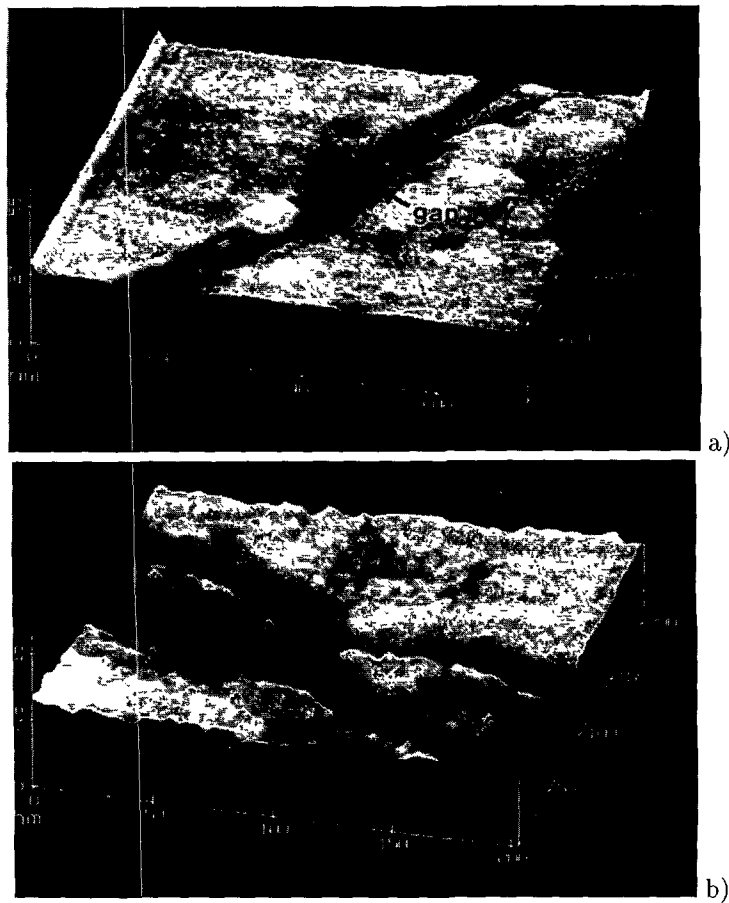


Fig. 5. — a) A 3D view AFM constant force image of a 8 nm gap fabricated with the electrodes fully buried in the  $\text{SiO}_2$  surface. The image size is  $0.7 \times 0.7 \mu\text{m}^2$ . b) A 3D view of a smaller scan in the center of the Figure 5a nanojunction to show the end of the two AuPd electrodes and the missing  $\text{SiO}_2$  material in the gap. The image size is  $0.2 \times 0.2 \mu\text{m}^2$ .

#### 4. Conclusion

An optimized process has been proposed to fabricate co-planar MIM nanojunctions with a gap length lower than 10 nm and with the electrodes buried in an insulating surface. Co-planar nanojunctions with a 8 nm distance between their electrodes have been fabricated on  $\text{SiO}_2$  and characterized with an AFM. When the  $\text{SiO}_2$  etching duration is reduced, there is still  $\text{SiO}_2$  material in the gap. For completely buried electrodes, 8 nm gaps can be obtained but without  $\text{SiO}_2$  in the gap. We are currently working to increase the process yield.

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