

Directed self-organization of graphene nanoribbons on SiC

M. Sprinkle,¹ M. Ruan,¹ X. Wu,¹ Y. Hu,¹ M. Rubio-Roy,¹
J. Hankinson,¹ N.K. Madiomanana,¹ C. Berger,^{1,2} and W.A. de Heer¹

¹*Georgia Institute of Technology, Atlanta, Georgia 30332-0430, USA*

²*CNRS/Institut Néel, BP166, 38042 Grenoble, France*

Abstract

Realization of post-CMOS graphene electronics requires production of semiconducting graphene, which has been a labor-intensive process.¹⁻⁵ We present tailoring of silicon carbide crystals via conventional photolithography and microelectronics processing to enable templated graphene growth on $4H$ -SiC $\{1\bar{1}0n\}$ ($n \approx 8$) crystal facets rather than the customary $\{0001\}$ planes. This allows self-organized growth of graphene nanoribbons with dimensions defined by those of the facet. Preferential growth is confirmed by Raman spectroscopy and high-resolution transmission electron microscopy (HRTEM) measurements, and electrical characterization of prototypic graphene devices is presented. Fabrication of $> 10,000$ top-gated graphene transistors on a 0.24 cm^2 SiC chip demonstrates scalability of this process and represents the highest density of graphene devices reported to date.

Epitaxial graphene on SiC is an exciting new electronic material that presents the possibility of room temperature ballistic devices.^{6–8} Extremely high carrier mobilities, exceeding $250,000 \text{ cm}^2/(\text{V} \cdot \text{s})$ at room temperature, have been observed,⁹ and epitaxial graphene has been shown to be compatible with traditional top-down processing techniques.¹⁰ Its linear semi-metallic band structure¹¹ allows ambipolar tuning of conduction and direct application to RF devices,¹² while other devices require modification of the graphene sheet to induce a band gap. The latter has received significant attention, and has been accomplished by selective chemical treatment,^{13,14} and nanoribbon fabrication,^{1–5} which results in a band gap inversely proportional to ribbon width.^{15–17} The nanoribbon approach is promising in that it has shown large gating effects, but production methods documented thus far, including e-beam lithography^{1–3} and other approaches,^{4,5} are too slow and not controllable enough for technological application.

Morphology of epitaxial graphene on SiC is highly influenced by the structure of the underlying substrate. In well-controlled growth conditions,^{7,8,18,19} nominally on-axis SiC retains an ordered terrace structure that originates in the miscut angle of the SiC wafer. Many interpret these steps as being problematic,²⁰ but scanning tunneling microscopy measurements have consistently observed that the graphene lattice is continuous over such steps. This is true of 0.5 nm 4*H*-SiC half-unit cell steps and few-nm steps where step bunching occurs.^{6,21} We find [see Fig. 1] that this remains true at a much larger scale; graphene pleats typically present on the SiC(000 $\bar{1}$) plane¹⁸ are observed traversing prepared SiC steps as large as 150 nm, indicating continuity of graphene over the step. These observations explain transport measurements in which underlying SiC steps appear to have little effect on mobility^{7,22} or observation of the quantum Hall effect,²² and suggest exploitation of the effect to produce nanoribbons by novel fabrication methods.

It has long been known²³ that SiC{0001} surfaces exhibit step bunching in various environments. Recent systematic studies have found a greater propensity for step bunching on the (0001) face,^{24–27} with vicinal miscuts toward $\langle 1\bar{1}00 \rangle$ displaying bunching of parallel steps into $(1\bar{1}0n)$ “nanofacets” up to 4–5 unit cells in height, oriented at an angle of $\sim 25^\circ$ to the basal plane.^{25,26} It has been suggested that such nanofacet formation may be understood as a minimization of surface free energy.^{25,28} Steps perpendicular to the directions $\langle 1\bar{1}00 \rangle$ are strongly favored on (0001), such that steps formed macroscopically perpendicular to $\langle 11\bar{2}0 \rangle$ are microscopically zigzagged, with segments perpendicular to $\langle 1\bar{1}00 \rangle$ directions.^{24–27}

The $(000\bar{1})$ face, by contrast, seems to form steps at almost any orientation.²⁶ Step-bunched nanofaceting has not been observed there previously,^{26,27} but we show in Fig. 1 that a $(1\bar{1}0n)$ facet is induced by pre-processing (see below). These results are qualitatively true of both $6H$ - and $4H$ -SiC polytypes.²⁶ It is perhaps expected that graphene growth should proceed first on facets, given the lesser bonding of Si atoms, and this has been observed on etching-induced $(1\bar{1}0n)$ ²⁰ and $(11\bar{2}n)$ ²⁹ nanofacets.

We propose exertion of control over the natural step bunching mechanism to prepare a crystal facet for self-organized graphene growth [see Fig. 2]. Given the discussion above, the best choice for this purpose may be $(1\bar{1}0n)$. Controlled facets are achieved by photolithographic definition of Ni lines on a SiC substrate perpendicular to the $\langle 1\bar{1}00 \rangle$ direction; these lines are transferred into the SiC by a fluorine-based reactive ion etch (RIE), which, while relatively simple technologically, allows nm-precision in the etch depth. As depicted in Fig. 2, it is the etch depth that ultimately defines the width of nanoribbons prepared. 15 nm etch depths were readily achieved in this work, which resulting ribbon width (~ 30 nm) is sufficiently narrow to result in a sizable band gap at room temperature. Much narrower widths should be reachable with minimal effort. We have nevertheless chosen to focus here on ~ 200 nm ribbon widths that allow convincing demonstration of the concept via accessibility to characterization probes including Raman spectroscopy, yet narrow enough to exhibit a band gap at low temperature. After removal of the Ni mask and cleaning, the crystal is heated to elevated temperatures (1200 – 1300 °C) at intermediate vacuum (10^{-4} Torr) for 30 min., inducing SiC step flow; the abrupt step relaxes to a $(1\bar{1}0n)$ facet, and the temperature is elevated to > 1450 °C for graphene growth as described previously.^{6,7,18}

Preferential growth on the facet is confirmed by Raman mapping as shown in Fig. 3b. The intensity of the 2D Raman band (2700 cm^{-1}) characteristic of graphene is mapped over a ~ 100 nm SiC step and adjacent (0001) faces. Little to no intensity is observed on the horizontal surfaces, but significant intensity is seen at the step edge, indicating presence of graphene there. Note that the lateral resolution of the Raman instrument, at $\sim 1\ \mu\text{m}$, is much larger than the facet width and the mapping grid spacing. Optimization of growth temperature and time will foreseeably enhance selectivity.

Cross-sectional HRTEM images [see Fig. 3c] also evidence preferential growth. Multiple layers of graphene are observed on the facet, with only partial layers on the horizontal (0001) plane. The facet angle observed, 24° , is in agreement with AFM measurements (not shown)

of $24\text{--}28^\circ$ across multiple samples and locations, corresponding to the high-index SiC facet ($1\bar{1}0n$), where $n \approx 8$. The precise facet obtained is dependent on processing temperature.²⁴

Ribbon samples were prepared for electrical measurement by exposure to an extremely short directional O_2 RIE to remove any graphene fragments from the horizontal (0001) surface. This was verified by Raman mapping, as shown in Fig. 4b. Extensive electrical probing confirmed lack of measurable conductivity on the horizontal surfaces. Note that this processing step will very likely become unnecessary with refinement of preferential growth parameters. Metal contacts were deposited for four-terminal measurements without gate and two-terminal measurements with top gate. In the latter case, an Al_2O_3 dielectric was deposited by atomic layer deposition (ALD) followed by deposition of the metal gate [see Fig. 2].

Measurement of four-terminal test structures [see inset, Fig. 4c] yielded sheet resistances of $180\text{--}500\ \Omega/\text{sq.}$, values typically observed in as-grown planar graphene,⁸ suggesting that the quality of these ribbons does not differ dramatically from that of the planar material. Fig. 4c shows a series of conductance vs. source-drain voltage curves taken between 77 K and 4 K. The behavior is metallic at high temperatures, but quantum confinement is clearly manifested in the nonlinearity observed at 4 K, indicating presence of a small band gap, as expected of this ~ 200 nm ribbon and in agreement with previous reports.⁷

Photolithographic processing allows fabrication of a large number of devices at higher density. An array of top-gated graphene transistors prepared on the (000 $\bar{1}$) face of a 4×6 mm SiC chip with SiC etch depth ~ 100 nm is shown in Fig. 5b. A single device (source, drain, channel, and gate, as illustrated in Fig. 2) occupies a $35 \times 65\ \mu\text{m}$ area, so the $0.24\ \text{cm}^2$ chip accommodates more than 10,000 transistors. This density was limited primarily by the size of the probe tips used for electrical measurement, but it is, to our knowledge, the highest density of graphene transistors achieved to date. The room temperature gating effect is plotted in Fig. 5b. While transport characteristics of the various devices are reasonably consistent, there is work to be done in improving the selective growth and patterning. Two imminent changes will dramatically enhance this effect: reducing the growth temperature and time to in turn reduce the number of graphene layers on the facet, significantly improving gating efficiency, and reducing the SiC etch depth to narrow the ribbon, inducing a band gap at room temperature.

It should be noted that there are likely fundamental differences in the graphene growth

among the possible SiC facets, analogous to the dramatic differences in growth speed and layer orientation observed on the (0001) and (000 $\bar{1}$) faces,^{8,18} and the (1 $\bar{1}0n$) facet chosen here is possibly not the most desirable in terms of selectivity and quality of graphene produced. This is particularly true of facets prepared on the (000 $\bar{1}$) surface, where there is apparently more freedom in facet choice. This is a topic of ongoing research, but the directions are clear.

These results show that graphene growth on non-traditional crystal faces is viable and incredibly useful in device fabrication, particularly for production of nanoribbons on a large scale, and fabrication of graphene transistors at a density greater than 40,000 per cm² represents a milestone in the development of graphene electronics. Refinement of this approach appears imminent, as ribbon width is reduced, facet selection and selective graphene growth is optimized, and damage to ribbon edges by violent cutting processes is therefore eliminated. Pre-patterning of the SiC substrate is, in general, a new and promising direction in the development of epitaxial graphene electronics, as more complex structures and applications are readily envisaged. It is furthermore an important coalescence of top-down and bottom-up lithographies.

Methods

Substrates were nominally on-axis research-grade semi-insulating 4H-SiC from Cree, Inc. Arrays of Ni lines were defined on the (0001) or (000 $\bar{1}$) SiC crystal face by a standard photolithographic lift-off process, and transferred into the SiC by a 43% SF₆/23% O₂/33% Ar RIE operating at 30 mTorr. RF power was tuned to give a SiC etch rate of 8 Å/s, allowing precisely controllable etching. Ultrasonic treatment in nitric acid removed Ni from the SiC surface, and further cleaning and graphene growth proceeded as described previously.^{6,7,18} O₂ RIE operating at 100 mTorr was tuned to give a graphene etch rate of ~ 1 Å/s, and etch time was several to a maximum of ten seconds. Samples were mounted with (1 $\bar{1}0n$) facet parallel to ion flux. Pd/Au contacts were defined by e-beam or photo-lithographic lift-off. Atomic layer deposition (ALD) of Al₂O₃ was performed as described by Williams et al.³⁰ in a commercial Cambridge Nanosystems Savannah ALD system prior to photolithographic lift-off of an Al top-gate. Inclusion of an NO₂ functionalization step as specified by Williams was critical for uniform Al₂O₃ coverage. Raman mapping was performed with excitation wavelength 532 nm, lateral resolution ~ 1 μ m, and 0.25 – 0.5 μ m grid spacing. 2D intensity

was taken at 2D maxima near 2725 cm^{-1} . HRTEM measurements were performed by Evans Analytical Group in Raleigh, NC, USA.

Acknowledgements: We acknowledge helpful conversations with A. Zangwill, V. Borovikov and F. Ming. This research was supported by the W.M. Keck Foundation and the NSF under grant No. DMR-0820382.

-
- ¹ Han, M. Y., Ozyilmaz, B., Zhang, Y. & Kim, P. Energy band-gap engineering of graphene nanoribbons. *Phys. Rev. Lett.* **98**, 206805 (2007).
 - ² Chen, Z., Lin, Y.-M., Rooks, M. J. & Avouris, P. Graphene nano-ribbon electronics. *Physica E* **40**, 228 – 232 (2007).
 - ³ Han, M. Y., Brant, J. C. & Kim, P. Electron transport in disordered graphene nanoribbons (2009). <http://arxiv.org/abs/0910.4808>.
 - ⁴ Tapasztó, L., Dobrik, G., Lambin, P. & Biró, L. P. Tailoring the atomic structure of graphene nanoribbons by scanning tunnelling microscope lithography. *Nat. Nano.* **3**, 397–401 (2008).
 - ⁵ Jiao, L., Zhang, L., Wang, X., Diankov, G. & Dai, H. Narrow graphene nanoribbons from carbon nanotubes. *Nature* **458**, 877–880 (2009).
 - ⁶ Berger, C. *et al.* Ultrathin epitaxial graphite: 2D electron gas properties and a route toward graphene-based nanoelectronics. *J. Phys. Chem. B* **108**, 19912–19916 (2004).
 - ⁷ Berger, C. *et al.* Electronic confinement and coherence in patterned epitaxial graphene. *Science* **312**, 1191–1196 (2006).
 - ⁸ de Heer, W. A. *et al.* Epitaxial graphene. *Solid State Commun.* **143**, 92–100 (2007).
 - ⁹ Orlita, M. *et al.* Approaching the dirac point in high-mobility multilayer epitaxial graphene. *Phys. Rev. Lett.* **101**, 267601 (2008).
 - ¹⁰ Kedzierski, J. *et al.* Epitaxial graphene transistors on SiC substrates. *IEEE T. Electron Dev.* **55**, 2078–2085 (2008).
 - ¹¹ Sprinkle, M. *et al.* First direct observation of a nearly ideal graphene band structure. *Phys. Rev. Lett.* **103**, 226803 (2009).
 - ¹² Moon, J. *et al.* Epitaxial-graphene RF field-effect transistors on Si-face 6H-SiC substrates. *IEEE Electron Dev. Lett.* **30**, 650–652 (2009).
 - ¹³ Wu, X. S. *et al.* Epitaxial-graphene/graphene-oxide junction: An essential step towards epitaxial

- graphene electronics. *Phys. Rev. Lett.* **101**, 026801 (2008).
- ¹⁴ Bekyarova, E. *et al.* Chemical modification of epitaxial graphene: Spontaneous grafting of aryl groups. *J. Am. Chem. Soc.* **131**, 1336 (2009).
- ¹⁵ Nakada, K., Fujita, M., Dresselhaus, G. & Dresselhaus, M. S. Edge state in graphene ribbons: Nanometer size effect and edge shape dependence. *Phys. Rev. B* **54**, 17954–17961 (1996).
- ¹⁶ Fujita, M., Wakabayashi, K., Nakada, K. & Kusakabe, K. Peculiar localized state at zigzag graphite edge. *J. Phys. Soc. Jpn.* **65**, 1920–1923 (1996).
- ¹⁷ Wakabayashi, K. Electronic transport properties of nanographite ribbon junctions. *Phys. Rev. B* **64**, 125428 (2001).
- ¹⁸ Hass, J., de Heer, W. A. & Conrad, E. H. The growth and morphology of epitaxial multilayer graphene. *J. Phys.: Condens. Matter* **20**, 323202 (2008).
- ¹⁹ Emtsev, K. V. *et al.* Towards wafer-size graphene layers by atmospheric pressure graphitization of silicon carbide. *Nat. Mater.* **8**, 203–207 (2009).
- ²⁰ Robinson, J. *et al.* Nucleation of epitaxial graphene on SiC(0001). *ACS Nano* **4**, 153 (2010).
- ²¹ Hass, J. R. *Structural characterization of epitaxial graphene on silicon carbide*. Ph.D. thesis, Georgia Institute of Technology (2008). <http://hdl.handle.net/1853/26654>.
- ²² Wu, X. *et al.* Half integer quantum Hall effect in high mobility single layer epitaxial graphene. *Appl. Phys. Lett.* **95**, 223108 (2009).
- ²³ Kong, H. S., Glass, J. T. & Davis, R. F. Chemical vapor deposition and characterization of 6H-SiC thin films on off-axis 6H-SiC substrates. *J. Appl. Phys.* **64**, 2672–2679 (1988).
- ²⁴ Syväjärvi, M., Yakimova, R. & Janzn, E. Step-bunching in SiC epitaxy: anisotropy and influence of growth temperature. *J. Cryst. Growth* **236**, 297 – 304 (2002).
- ²⁵ Nakajima, A., Yokoya, H., Furukawa, Y. & Yonezu, H. Step control of vicinal 6H-SiC(0001) surface by H₂ etching. *J. Appl. Phys.* **97**, 104919 (2005).
- ²⁶ Nie, S. *et al.* Step formation on hydrogen-etched 6H-SiC{0001} surfaces. *Surf. Sci.* **602**, 2936 – 2942 (2008).
- ²⁷ Borovikov, V. & Zangwill, A. Step bunching of vicinal 6H-SiC{0001} surfaces. *Phys. Rev. B* **79**, 245413 (2009).
- ²⁸ Nakagawa, H., Tanaka, S. & Suemune, I. Self-ordering of nanofacets on vicinal SiC surfaces. *Phys. Rev. Lett.* **91**, 226107 (2003).
- ²⁹ Tanaka, S., Morita, K. & Hibino, H. Anisotropic layer-by-layer growth of graphene on vicinal

SiC(0001) surfaces. *Phys. Rev. B* **81**, 041406 (2010).

- ³⁰ Williams, J. R., DiCarlo, L. & Marcus, C. M. Quantum Hall effect in a gate-controlled p-n junction of graphene. *Science* **317**, 638–641 (2007).

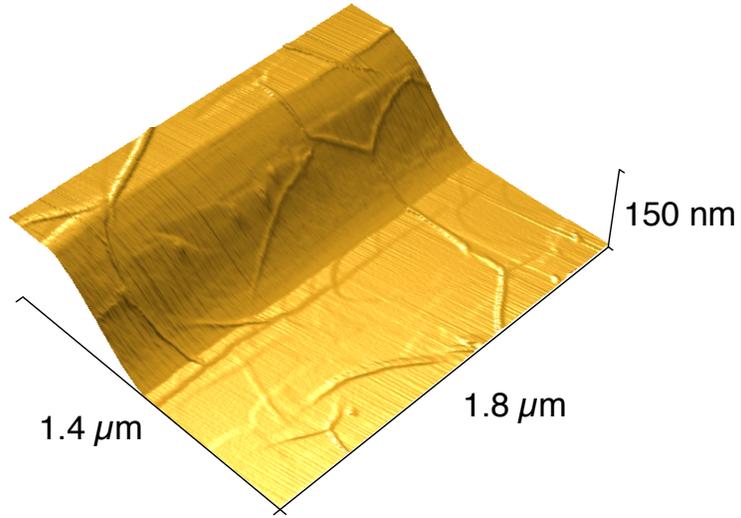


FIG. 1: AFM scan demonstrating continuity of multilayer epitaxial graphene over a ~ 145 nm step on the SiC(000 $\bar{1}$) plane. Raised pleats are caused by relative contraction of SiC as the sample cools from elevated growth temperatures,¹⁸ and their traversal of the step clearly indicates continuity of graphene over the step.

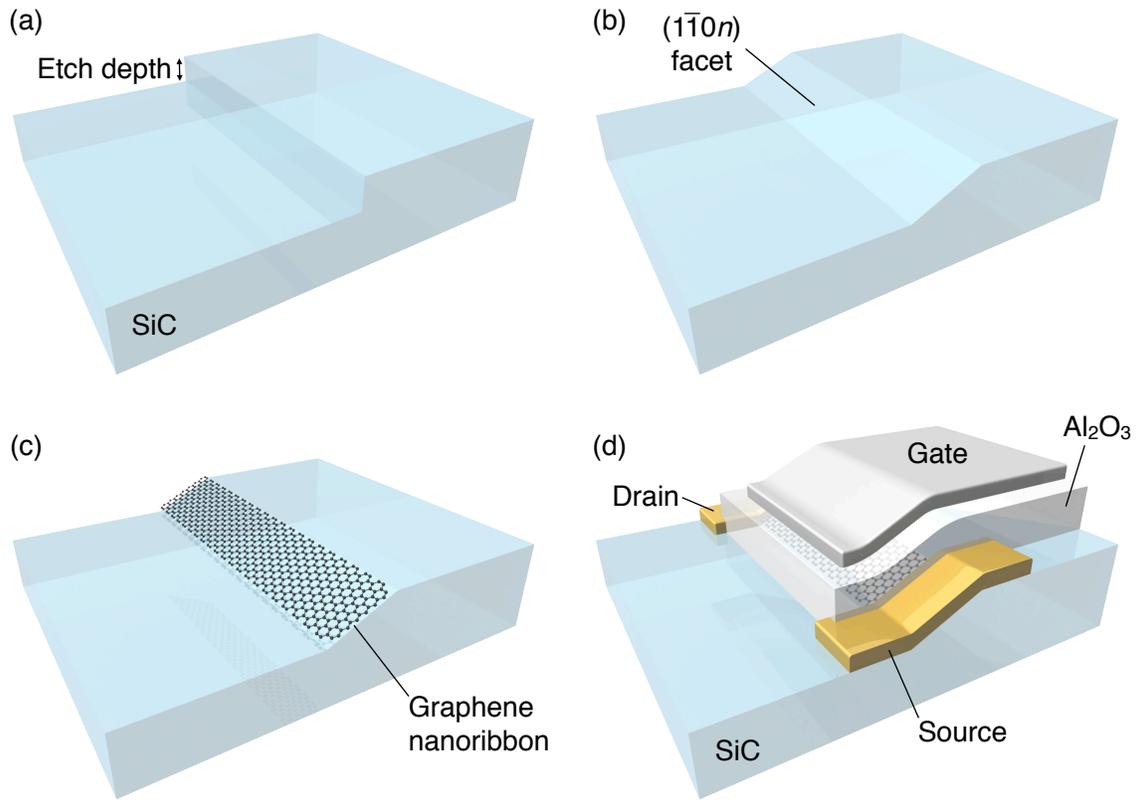


FIG. 2: Process for tailoring of the SiC crystal for selective graphene growth and device fabrication. (a) nm-scale step is etched into SiC crystal by fluorine-based RIE. (b) Crystal is heated to 1200 – 1300 °C (at low vacuum), inducing step flow and relaxation to the $(1\bar{1}0n)$ facet. (c) Upon further heating to $\sim 1450^\circ\text{C}$, self-organized graphene nanoribbon forms on the facet. (d) Complete device with source and drain contacts, graphene nanoribbon channel, Al_2O_3 gate dielectric, and metal top gate, as pictured in Fig. 5.

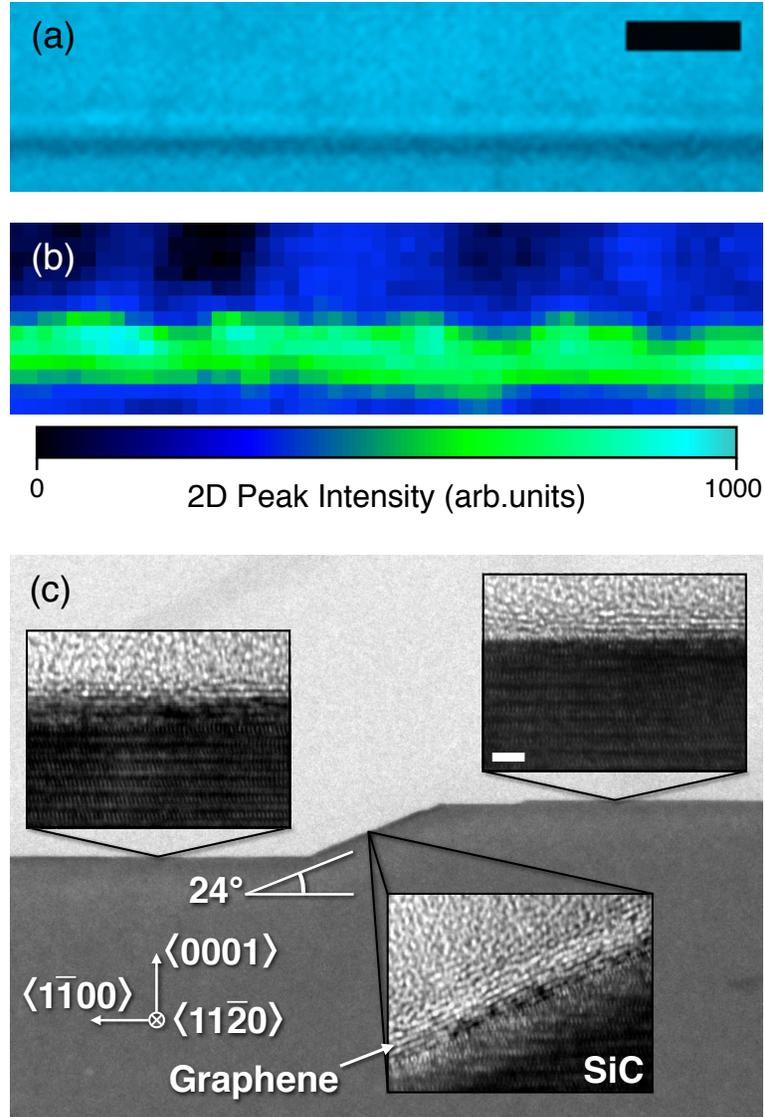


FIG. 3: (a) Optical micrograph of a pre-patterned ~ 100 nm step on the SiC(0001) face following graphene growth. Scale bar is $2 \mu\text{m}$. (b) Raman map ($\sim 1 \mu\text{m}$ lat. res., $0.25 \mu\text{m}$ grid) of the 2D peak intensity at this location indicates preferential graphene growth on the $(1\bar{1}0n)$ facet. (c) HRTEM cross-sectional images of a similar step confirm preferential growth on the $(1\bar{1}0n)$ facet. Scale bar is 2 nm, and applies to all insets.

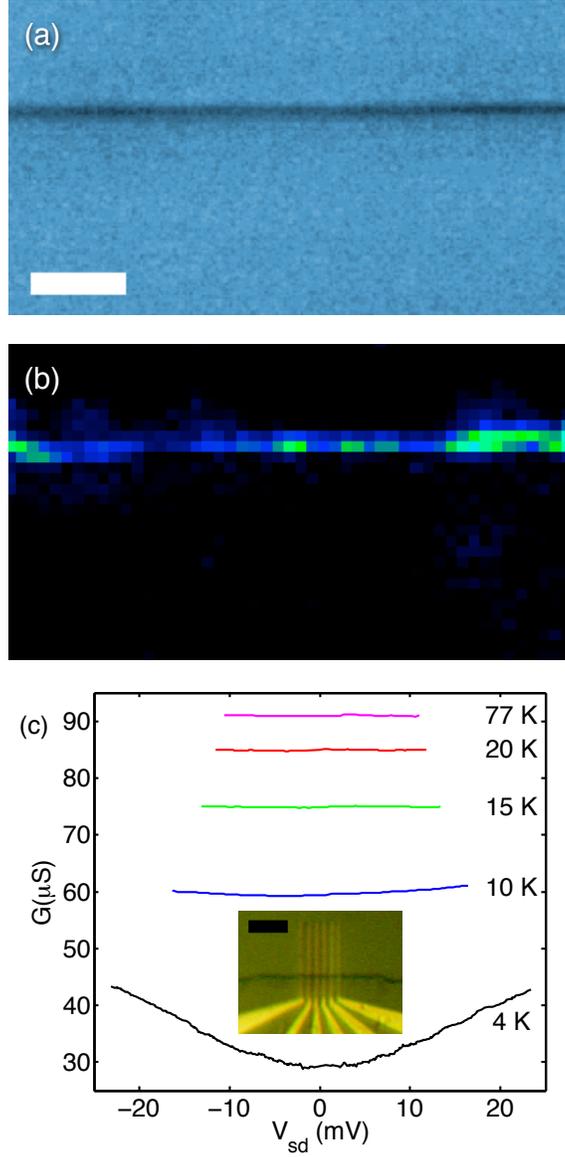


FIG. 4: (a) Optical micrograph of $(1\bar{1}0n)$ facet with graphene ribbon. Scale bar is $2\ \mu\text{m}$. (b) Raman map ($\sim 1\ \mu\text{m}$ lat. res., $0.5\ \mu\text{m}$ grid) of graphene 2D intensity at this location indicates presence of graphene essentially exclusively on the facet. (c) Conductance vs. source-drain voltage as a function of temperature. Band gap is observed at 4K as expected for a ribbon of this width (200 nm). Inset: optical micrograph of test structure. Scale bar is $5\ \mu\text{m}$.

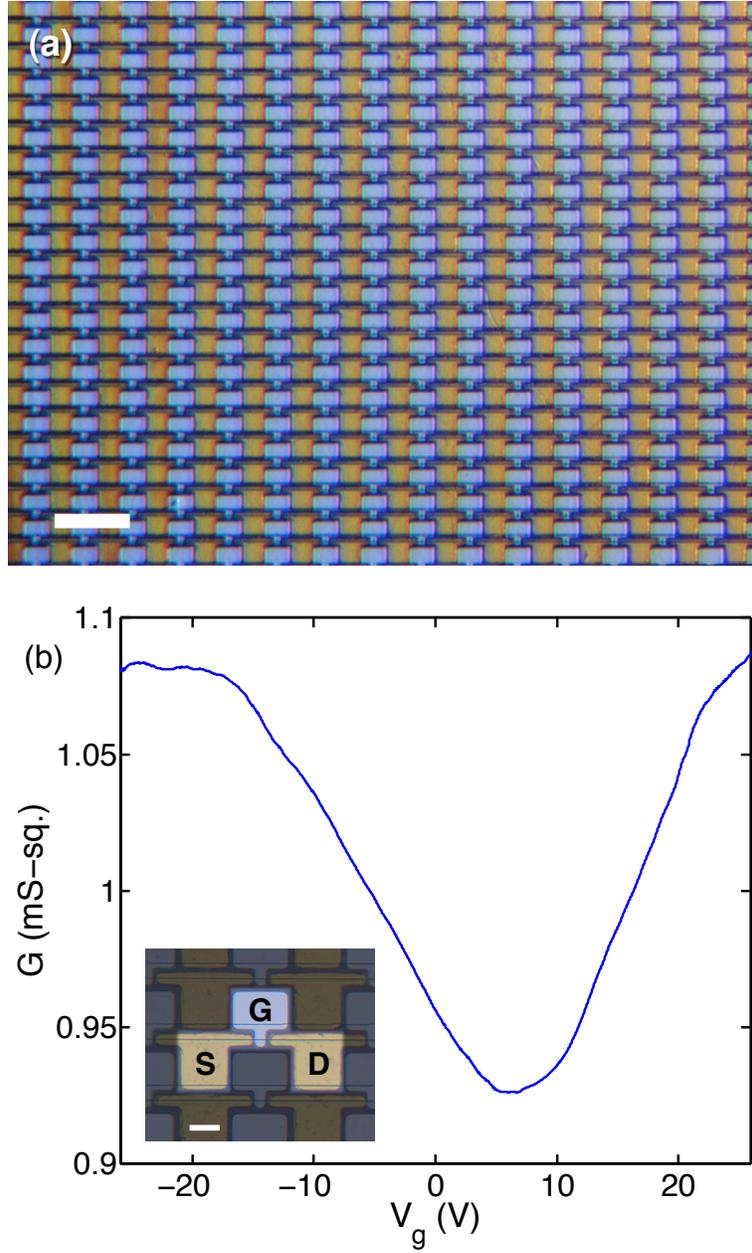


FIG. 5: (a) Graphene transistor array with density 40,000 devices per cm^2 . Scale bar is $100\ \mu\text{m}$. (b) Room temperature ambipolar gating effect: conductance G vs. gate voltage V_{sd} . Inset: an individual FET consisting of source (S), drain (D), graphene channel, and gate (G). Scale bar is $20\ \mu\text{m}$.