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Two-dimensional flexible nanoelectronics

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2014/2015 represents the tenth anniversary of modern graphene research. Over this decade, graphene has proven to be attractive for thin-film transistors owing to its remarkable electronic, optical, mechanical and thermal properties. Even its major drawback—zero bandgap—has resulted in something positive: a resurgence of interest in two-dimensional semiconductors, such as dichalcogenides and buckled nanomaterials with sizeable bandgaps. With the discovery of hexagonal boron nitride as an ideal dielectric, the materials are now in place to advance integrated flexible nanoelectronics, which uniquely take advantage of the unmatched portfolio of properties of two-dimensional crystals, beyond the capability of conventional thin films for ubiquitous flexible systems.

Two-dimensional (2D) atomic sheets are atomically thin, layered crystalline solids with the defining characteristics of intralayer covalent bonding and interlayer van der Waals bonding[1–3]. The expanding portfolio of atomic sheets illustrated in Fig. 1a currently include the archetypical 2D crystal graphene[3–14], transition metal dichalcogenides (TMDs)[1,2,15–21], diatomic hexagonal boron nitride (h-BN)[3,22–25], and emerging monoatomic buckled crystals collectively termed Xenes, which include silicene[2,26,27], germanene[2] and phosphorene[28–31]. These materials are considered 2D because they represent the thinnest unsupported crystalline solids that can be realized, possess no dangling surface bonds and show superior intralayer (versus interlayer) transport of fundamental excitations (charge, heat, spin and light). The portfolio is expected to grow as more elemental and compound sheets are uncovered.

The outstanding properties of 2D crystals have generated immense interest for both conventional semiconductor technology and the nascent flexible nanotechnology because, amongst other considerations, these atomic sheets afford the ultimate thickness scalability desired in a variety of essential material categories, including semiconductors, insulators, transparent conductors and transducers[3,16,18]. In particular, flexible nanoelectronics stand to greatly benefit from the development of 2D crystals because their unmatched combination of device physics and device mechanics is accessible on soft polymeric or plastic substrates[17,18,32,33], which can enable the long sought after large-area high-performance flexible devices that can be manufactured at economically viable scales. As a result, existing flexible technology is expected to be transformed from low-cost commodity applications, such as radio-frequency identification tags and sensors, to integrated nanosystems with electronic performance comparable to silicon devices, in addition to affording mechanical flexibility and manufacturing form-factor beyond the capability of conventional semiconductor technology[34]. Hence, a new era in integrated flexible technology founded on 2D crystals is emerging.

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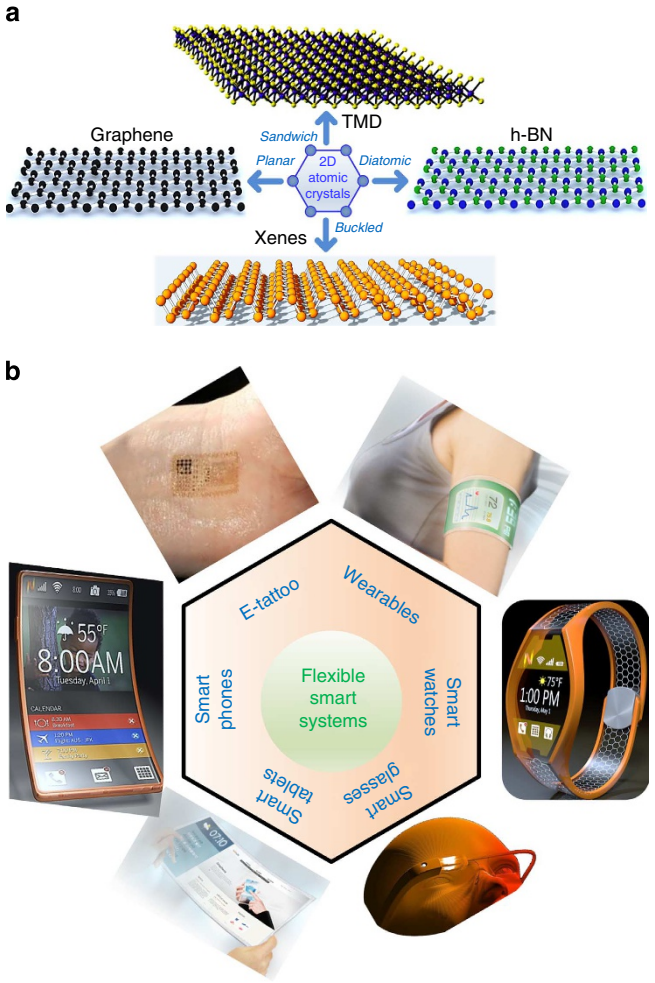

Figure 1 | Illustration of 2D monolayer materials and examples of flexible smart systems. (**a**) Three-dimensional illustrations of contemporary 2D monolayers revealing diverse physical structures based on an underlying hexagonal lattice. (**b**) 2D atomic sheets can fulfil many of the electronic, optical and mechanical functions required in a flexible smart system, and especially enable 'RF wireless communication & connectivity,' which has become an indispensable feature in modern smart systems. (Image of the smart tablet and wearable system courtesy of Graphene Square Inc.; Image of smart glasses courtesy of E. Guy; Image of E-tattoo courtesy of N. Lu, University of Texas—Austin).

This article serves as a general, albeit focused, review of flexible 2D nanoelectronics covering their progress, prospects and contemporary challenges. Remarkably, in the 10 years since basic academic studies of small graphene flakes was pioneered, commercial products are now available including smart phones with graphene touch panels. In general, 2D atomic sheets are under rapid development leveraging the understanding gained from graphene.

A soft introduction

One might wonder: why flexible nanoelectronics? Can ubiquitous silicon electronics not fulfil the evolving technology aspirations of modern society? For some new technologies at the forefront of the innovation horizon, 2D atomic sheets offer a unique and compelling capability. A case in point is wearable electronics such as smart glasses, smart watches, smart fabrics and electronic tattoos[35], which ideally require large-area nanomanufacturing of devices based on ultra-thin functional materials that are transparent and energy efficient, and can afford radio-frequency (RF) wireless connectivity on a flexible substrate. Another new example is an integrated communication and computation system, such as a universal ultra-portable gadget that can transform into several user-reconfigurable form factors including a smart phone, smart tablet and computer with the desirable benefits of low-cost manufacturing on soft substrates that are foldable, rollable, environmentally benign and recyclable. This sort of universal gadget has attracted the imagination of technology companies, embodied by Nokia's 'Morph' concept[34]. In addition, the applications of 2D atomic sheets towards other emerging concepts, such as origami inspired foldable systems, flexible bioelectronics and wireless structural health monitors, could also substantially benefit from the atomic profile and high-performance transport properties. For clarity, we note that a 'smart system' can be understood simply as any gadget with embedded wireless connectivity that at a minimum can interact with the user or environment. Examples of some highly anticipated flexible smart systems are shown in Fig. 1b.

The importance of mobility. Historically, organic, amorphous and metal oxide thin-film transistors (TFTs) have been explored for flexible electronics; however, their low charge mobility (μ) has limited their prospects to specific low-frequency applications such as tags and control electronics for displays[34]. Figure 2 compares the charge mobility of several candidate semiconducting materials, clearly demonstrating that large-bandgap TMDs (for example, MoS_2 and WSe_2) offer experimental mobilities approaching single-crystal silicon TFTs, with two orders of magnitude thinner profile and higher strain limits. Encouragingly, recent reports have shown that another 2D semiconductor, phosphorene, can afford even higher transistor mobilities around 1,000 $cm^2 V^{-1} s^{-1}$ at room temperature[28], a significant advancement for TFTs. The mobility of TFT materials is of great interest because it influences several performance metrics, such as current density, energy efficiency, switching delay and cutoff or transit frequency (f_T), a critical parameter for realizing GHz wireless connectivity. At low electric fields, the intrinsic $f_T = \mu E_{DS}/(2\pi L)$, where L is the transistor channel length and E_{DS} is the drain-source lateral electric field described by $E_{DS} = V_{DS}/L$ within the gradual channel approximation[36]. V_{DS} is the drain-source voltage. It follows that the charge mobility directly determines the low-power frequency capability and the likely applications comprising connectivity, communication and computation that can be realized in practice.

Achieving high mobilities in films that are atomically thin (Fig. 2c) is also noteworthy because the 2D thickness limit represents the ideal conditions for realizing maximum electrostatic control[16], maximum optical transparency[6,18,37], maximum chemical sensor sensitivity[1] and maximum mechanical flexibility[7,20,32].

A role for graphene for flexible nanoelectronics. In Fig. 2, it can be seen that graphene affords the highest field-effect transistor (FET) mobilities, owing to its small effective mass (m^*). However, the lack of a bandgap and the associated inability to electrically switch off precludes its use for digital transistors[4]. Nevertheless, its high charge mobility and saturation velocity ($>10^7$ cm s^{-1}) coupled with its intrinsic ambipolar character make it an attractive material for flexible RF analogue TFTs[32,38], which have already been employed to demonstrate several RF circuit blocks such as frequency multipliers[39], and multi-modulation wireless circuits[37]. In addition, non-transistor applications including transparent conductive films, heat spreaders, acoustic

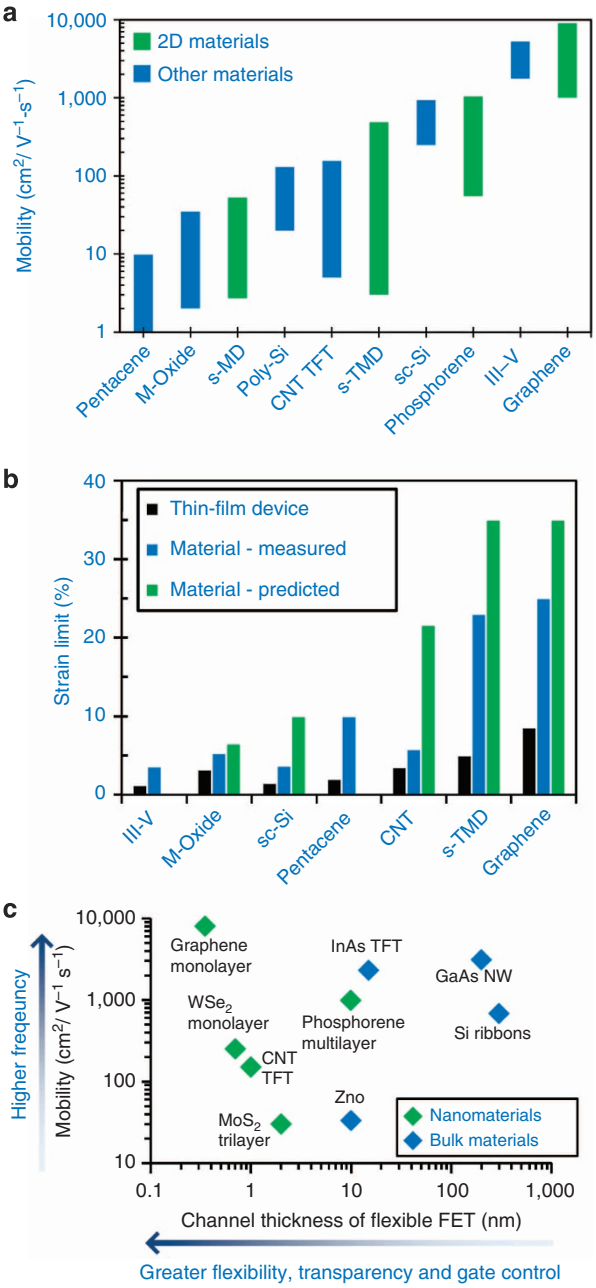

Figure 2 | Mobility and strain comparison of candidate materials for flexible TFTs. (**a**) Comparison of experimentally reported FET mobilities of candidate synthetic materials for flexible TFTs, including mobility variations reported across a wide variety of experimental samples at room temperature. Semiconducting TMDs (s-TMDs) offer mobilities higher than ordinary TFTs, and comparable to single-crystal Si (sc-Si). The first report of phosphorene (non-flexible) FETs offers maximum mobility around 1,000 $cm^2 V^{-1} s^{-1}$, while graphene affords the highest mobilities, though it lacks a bandgap. Data taken from refs 17,18,28,32,34,38,40,43–45,60,62,76,78–83. (**b**) Maximum elastic strain limits of candidate materials for flexible TFTs. 2D materials offer higher theoretical and measured strain limits than conventional bulk semiconductor materials. Data taken from refs 7,11,20,32,66,84–91. (**c**) Comparison of the thicknesses of selected high-mobility TFTs. The thinner profile of 2D atomic sheets can result in better device electrostatic control and mechanics while affording mobility similar to bulk semiconductors. 'Bulk materials' denote bulk solids made to be or deposited to be thin, while nanomaterials refer to van der Waal-layered materials that are intrinsically scalable to a single layer. Data taken from refs 16,18,28,32,43,45,79,81,83.

speakers and mechanical actuators can all be enabled by flexible graphene, where the lack of a bandgap is not a limitation.

Table 1 summarizes the basic optical, electrical, mechanical and thermal properties of several 2D atomic sheets that span the range from semimetals to insulators. This table is a useful reference for guiding the selection of material(s) and device design for flexible nanoelectronics. As a general material, graphene offers the fastest charge transport, stiffness and thermal conductivity. Phosphorene and semiconducting TMDs are well suited to serve as the semiconducting channel for digital electronics. In addition, direct bandgap monolayer TMDs can be used for optoelectronics. For atomically thin insulating sheets, multilayer h-BN has been proven to be the ideal dielectric for enhanced charge transport for 2D TFTs, owing to its atomically smooth surface, large phonon energies, high dielectric breakdown field and high in-plane thermal conductivity compared with conventional dielectrics[3,18,39].

In addition, semiconducting metal dichalcogenides (for example, SnS_2 and $SnSe_2$) and buckled graphene analogues (Xenes) have recently emerged as candidate 2D crystals for flexible nanoelectronics and are currently under growing theoretical and experimental studies[26–28,40]. At the moment, the study of Xenes is at a nascent state compared to the other 2D crystals, with many basic questions of interest, including their air stability and further understanding of the effects of a wide range of interfaces on their electronic properties.

Beyond the glass ceiling

The desire to integrate electronics onto novel, non-planar and malleable surfaces has motivated the need for flexible devices, which demonstrate uniform electronic properties across a wide range of applied strains. Using pliable electronic materials, such as semiconducting polymers and organic molecules, to fabricate TFTs on soft substrates has had limited applications due to the low-field-effect mobilities[34,41,42]. Enhanced device performance has been achieved by utilizing thin films or membranes of conventional semiconductor materials, including crystalline and polycrystalline Si and III–V semiconductors that offer improved electronic properties albeit at the cost of overall device flexibility and thickness scalability[43–45] (see Fig. 2).

Strain on the surface of a material subject to flexural bending decreases linearly with substrate thickness; hence, even materials that are brittle in bulk form can be flexed to a degree when produced as a thin film. Under pure bending, the strain, ε, at any given point in the substrate is a function of both the bending radius, ρ, and the perpendicular distance, z, from the neutral axis (axis running through the geometric centre of the device), given by the relationship $\varepsilon = z/(2\rho)$. From this relationship, it is evident that the minimum bending radius that a flexible device can be subjected, before mechanical failure, is limited by both the material's elastic strain limit, as well as by the geometry of the device and substrate. Thus, increased device flexure can be achieved in two ways: (i) by utilizing materials with a high strain limit and (ii) by modifications to device design that minimize the distance of the TFT from the neutral axis of the substrate. Strategies to minimize this distance include thinning the substrate or moving the device from the substrate surface (where strains reach a maximum) nearer to the neutral axis (where strains vanish), for instance by two-sided encapsulation. Although practical design requirements may complicate the ability to move the TFT device plane to coincide with the neutral axis of the substrate, in principle it is possible to design a highly flexible device out of a relatively brittle material. Indeed, TFTs fabricated from crystalline Si on 25-μm thick substrates and encapsulated to maintain the device plane within 2 μm of the substrate's neutral

Table 1 | Room temperature solid-state properties of selected 2D crystalline materials.

2D Material	Optical		Electrical		Mechanical		Thermal		References
	Band gap (eV)	Band Type	Device Mobility ($cm^2 V^{-1} s^{-1}$)	v_{sat} ($cm s^{-1}$)	Young's Mod. (GPa)	Fracture strain (%) Theor (Meas)	κ ($W m^{-1} K^{-1}$)	CTE ($10^{-6} K^{-1}$)	
Graphene	0	D	10^3–5×10^4	1–5×10^7	1,000	27–38 (25)	600–5,000	−8	4–11
1L MoS_2	1.8	D	10–130	4×10^6	270	25–33 (23)	40	NA	1,19–21,27,92
Bulk MoS_2	1.2	I	30–500	3×10^6	240	NA	50 (||), 4 ($_\perp$)	1.9 (||)	1,15,62,92–95
1L WSe_2	1.7	D	140–250	4×10^6	195	26–37 (NA)	NA	NA	1,16,84,96
Bulk WSe_2	1.2	I	500	NA	75–100	NA	9.7 (||), 2 ($_\perp$)	11 (||)	1,93,97–100
h-BN	5.9	D	NA	NA	220–880	24 (3-4)	250–360 (||) 2 ($_\perp$)	−2.7	22–25
Phosphorene	0.3–2*	D	50–1,000	NA	35–165	24–32	10–35 (||)	NA	28–30

h-BN, hexagonal boron nitride; NA, not available; 2D, two-dimensional.
All listed values should be considered estimates. In some cases, experimental or theoretical values are not available (NA).
*The precise value for the bandgap, which is a maximum for a monolayer is a matter of ongoing research.
The || symbol signifies the in-plane direction; ⊥ signifies the out of plane direction.

axis have achieved bending radii below 400 μm while maintaining tensile strains of less than 0.2% in the active devices[46].

However, highly bendable devices are not necessarily equivalent to highly flexible devices. In general, device stretchability is also desired to enable applications such as conformal electronics, surface-mountable smart sensors or bioelectronics[35,47]. In stretching, it is purely the elastic properties of the component materials that determine the strain limits of the overall flexible device. While techniques such as prestraining or texturing materials used in the fabrication of flexible TFTs can reduce strain transferred from a deformed substrate to the active electronic components[42], the flexibility of a device under stretching is ultimately limited by material properties. Design criteria for highly bendable and stretchable electronics thus require materials that possess high strain limits and can be processed in thin layers.

The difference in strain limits between three-dimensional ionically bound semiconductors and 2D covalently bound semiconductors can be understood from simple interatomic force models. These models calculate the bond strength of covalently bound crystals to be significantly higher than those in ionic crystals, translating to typical yield strains in ionic crystals ranging from 7 to 18% (ref. 48), whereas the rupture of covalent bonds occurs at strains typically ranging between 20 and 40%, but up to 60% for H–H bonds[49]. For example, crystalline Si has a theoretical yield strain of ~10%, above which plastic deformation results in irreversible degradation to the lattice. In contrast, covalently bonded 2D crystals can show fully elastic behaviour up to strains of ~25–30%, at which point brittle fracture occurs at the ultimate strain limit of the constituent bonds[11,20]. Thus, the potential elastic limit for 2D crystals is significantly higher than that of bulk semiconductors. However, reaching this limit requires minimization of both internal grain boundaries and highly strained crystal edges, both of which can initiate fracture at strains significantly lower than the bulk[50]. Furthermore, the practical channel thickness of a 2D TFT can be significantly less than that of thin films of bulk semiconductors (see Fig. 2c), affording a further advantage for flexible electronics. Thus, 2D materials possess clear advantages, both in material thickness and elastic limit, in comparison with traditional semiconductors for flexible nanoelectronics, which demonstrate high electronic performance as well as high flexibility and stretchability.

Contemporary flexible performance

Over the last decade of intense focus and investigation, graphene material understanding and devices have advanced sufficiently to substantiate its potential for analogue RF circuits[4,13,32,37,39]. However, the limitation of graphene to realize a digital switch owing to its lack of a bandgap caused great concern[4]. Hearteningly, this concern has been laid to rest by the emergence of semiconducting 2D crystals, namely TMDs and phosphorene, which can offer a sizeable bandgap above 1 eV (refs 1,2,28). The heterogeneous cointegration of graphene and semiconducting 2D crystals on the same flexible substrate can collectively fulfil all primitive electronic functions at the thin-film limit.

The earliest work on flexible graphene TFTs was reported by Williams and coworkers[51] in 2007, based on exfoliated graphene and a lithography-free transfer printing method that avoids chemical contamination, resulting in transistor mobilities of $10{,}000\ cm^2 V^{-1} s^{-1}$ and $4{,}000\ cm^2 V^{-1} s^{-1}$ for holes and electrons, respectively, under ambient conditions. Their results indicated that the outstanding transport properties of graphene were indeed accessible on soft substrates, though large-area synthesized sheets are required for practical applications. Since then, synthesized graphene TFTs and circuits have made remarkable progress, featuring state-of-the-art TFT mobilities of $\sim 8{,}000\ cm^2 V^{-1} s^{-1}$, enabled by advancements in: (i) large-area chemical vapour deposited synthesis[52], (ii) post-synthesis transfer[53] and (iii) transistor device structure[32,38,54]. Readers interested in graphene synthesis will find the 2010 review article by Chhowalla and coworkers[55] an excellent resource. For large-area graphene, monolayers grown on copper surfaces have afforded outstanding material quality with post-transfer devices showing electronic performance comparable to devices made from exfoliated single-crystal flakes[5,13].

Initial graphene TFTs featured a top-gate device structure. Thereafter, it was realized that fabricating a top-gate stack directly on graphene presented several challenges, owing to the complex post-transfer gate dielectric integration and device lithography, which often resulted in reduced yield and degraded performance[54]. One approach to overcoming these challenges is to fabricate the gate stack separately on another substrate with subsequent transfer onto graphene for device completion. This method has been successfully employed to demonstrate outstanding graphene devices on rigid substrates[56]. Alternatively, by embedding the gate in or on the flexible sheet (Fig. 3a), based on a gate-first process[32,54], many of the fabrication challenges can be resolved, including: (i) seed-less gate dielectric deposition, (ii) thickness scalability of gate dielectric that is not limited by a seed layer, (iii) ease of realizing an arbitrarily large number of gate fingers for increased current drive with reduced gate resistance and noise, and

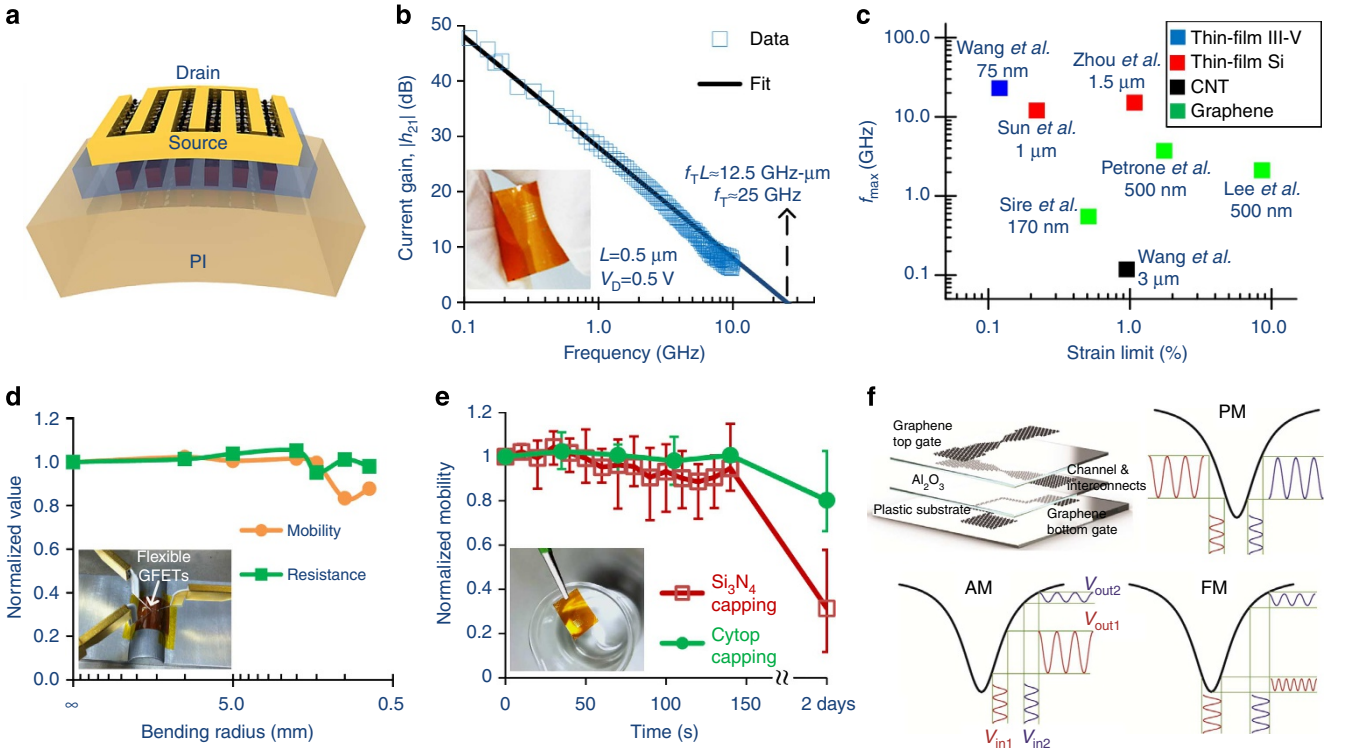

Figure 3 | High-performance room-temperature flexible graphene TFTs. (**a**) Illustration of multifinger embedded-gate graphene device structure that can afford high current drive, thin gate dielectrics, low gate resistance, surface passivation and simple post-transfer fabrication. (**b**) Measured current gain of high-frequency flexible graphene GFET with intrinsic f_T of ~25 GHz, corresponding to device metric, $f_T L$ ~12.5 GHz-μm. Inset is an optical image of flexible GFETs on a PI sheet. (**c**) Comparison of f_{max} and strain limits of flexible high-frequency FET technologies. Channel lengths of the associated devices are noted. Adapted, with permission, from ref. 38 (copyright 2012 American Chemical Society.) (**d**) Robustness of GFET mobility and contact resistance to mechanical bending down to 0.7 mm bending radius (~8% tensile strain). Inset is a photograph of a flexible sample attached to the bending fixture. (**e**) Robustness of passivated GFETs to immersion in deionized water. A bilayer capping consisting of fluoropolymer (Cytop) and nitride was found to be more effective than nitride capping alone, owing to the larger hydrophobicity of fluoropolymer. Inset is a photograph of encapsulated GFETs on PI after immersion in water. (© 2013 IEEE. Reproduced, with permission, from ref. 58.) (**f**) Demonstration of flexible and transparent all-graphene circuit capable of phase (PM), amplitude (AM) and frequency (FM) modulations. (Adapted from ref. 37). (**b**,**d**) Adapted, with permission, from ref. 32 (copyright 2013 American Chemical Society).

(iv) simpler post-transfer device completion with two lithographic steps. In addition, the embedded-gate process may be more adaptable to large-area nanomanufacturing on rolls or sheets using nanoimprint lithography because the entire fabrication is done on a single soft substrate.

Graphene TFTs employing the embedded-gate structure with a 500-nm channel length have achieved intrinsic f_T ~25 GHz at a modest lateral field of 1 V μm^{-1} on plastics (Fig. 3b)[32], corresponding to $f_T L$ ~12.5 GHz-μm, the current state-of-the-art for flexible graphene. This result compares favourably with f_T ~53 GHz at a similar channel length on crystalline SiC substrate[57] at a much higher field of ~4.5 V μm^{-1}. Increased lateral fields on flexible substrates should in principle afford commensurate increases in f_T. However, the associated Joule heating can lead to channel peak temperatures that exceed the glass transition temperature (T_g) of soft substrates (T_g ~350–400 °C for polyimide (PI), lower temperatures for other plastic substrates), resulting in local deformation of the plastic and ensuing device damage. This irreversible damage limits investigation of the ultimate high-field performance of high-mobility TFTs on plastic substrates, an issue that has only recently been brought to light[58]. We shall discuss the thermal management challenge in a later section.

An equally important frequency metric is the so-called maximum frequency of oscillation, f_{max}. While f_T can be viewed as the upper frequency limit on the amplification of elementary electronic signals (for example, current), f_{max} can be interpreted as the upper frequency limit for achieving power gain. An eloquent discussion of these two frequency metrics can be found in the review article by Schwierz[4]. In general, simultaneously achieving both high f_T and f_{max} is essential for analogue and RF electronics. In addition, f_T and f_{max} should be (approximately) greater than 3–5 × the desired operating circuit frequency. Figure 3c shows a graphene TFT with extrinsic f_{max} ~3.7 GHz (ref. 38). The true intrinsic f_{max}, commonly obtained by de-embedding the measurement probe pad parasitics, is likely higher. Promisingly, the high experimental f_T and ongoing efforts to improve f_{max} into the microwave regime by contact and gate resistance reduction paints a positive prospect for graphene TFTs to enable future smart flexible systems with wireless connectivity. Experimental results on rigid (diamond-like carbon) substrates supports this optimism, with reported f_T and f_{max} of about 120 and 45 GHz, respectively, an f_T/f_{max} ratio ~2.7 at a modest channel length of ~150 nm (ref. 14). Further improvements of the frequency response have been achieved at sub-100-nm channel lengths by using physically transferred gate stacks[56].

Regarding mechanical flexibility, tensile strains of up to 8% have been applied to high-frequency graphene TFTs[32,59], which is substantially larger than what has been achieved with thin-film Si and III–V flexible transistors (Fig. 3c). Figure 3d details the

electromechanical robustness of the mobility and contact resistance of a graphene TFT down to a bending radius of 0.7 mm. Even higher strains are expected to be possible since the intrinsic breaking strain of graphene is >20% (see Table 1).

Furthermore, several encapsulation coatings have been explored to improve the robustness of embedded-gate flexible graphene TFTs immersed in water or subjected to harsh conditions. The motivation for this type of investigation is that future smart systems have to be designed from the bottom-up to withstand common harsh conditions such as liquid spills and drops. Lee *et al.*[32] determined that a top-side bilayer coating of a hydrophobic fluoropolymer and a chemically inert silicon nitride diffusion barrier coupled with the low moisture absorption of PI substrate can provide effective protection against continuous immersion in water for up to 2 days (Fig. 3e).

By taking advantage of the unique ambipolar properties of graphene, several workers have demonstrated reconfigurable modulation circuits useful for wireless communication systems[37,39]. One particular example by Zhong and coworkers[37] is shown in Fig. 3f, in which a flexible all-graphene circuit on a transparent plastic sheet was employed to achieve three information modulation schemes: amplitude, phase and frequency modulation that would otherwise take a more complex circuit based on conventional semiconductors to realize.

Mind the gap. A primary limitation of graphene is the strength of semiconducting TMDs; the sizeable bandgap exhibited by TMDs affords near ideal electronic switches with on/off current ratios typically exceeding seven orders of magnitude. Combined with thickness scalability down to a monolayer that allows ideal electrostatic switches, TMDs are highly attractive for flexible digital electronics[1,2,16]. Early work on monolayer and multilayer flexible TMD transistors, mostly exploring MoS_2 TFTs, has been encouraging[17,18,60]. Figure 4a shows the electronic performance of a bendable *n*-type MoS_2 TFT on PI with integrated high-k dielectric in a back-gated device structure featuring on/off ratio $>10^7$ and near ideal sub-threshold slope. The device low-field carrier mobility and contact resistance are $\sim 30\,cm^2\,V^{-1}\,s^{-1}$ and $<40\,K\Omega$-μm, respectively, extracted from the modified Ghibaudo Y-function method, a technique that provides the benefit of independent estimation of both parameters from two-point transistor measurements[61]. The carrier mobilities of contemporary flexible MoS_2 TFTs are still several times lower than that of comparable state-of-the-art devices on hard Si substrates[15]. This might be related to several factors, including the optimum film thickness and dielectric environment, in addition to differences in material quality and residual stresses.

For optoelectronic devices, monolayer thick (~0.7 nm) semiconducting TMDs are preferred, owing to their direct bandgap character[1]. However, for transistor electronics, the optimum number of layers for the usual device parameters of interest, such as carrier mobility, current drive, contact resistance and electrostatic control, remains unclear. In this context, Appenzeller and coworkers[15] investigated unpassivated MoS_2

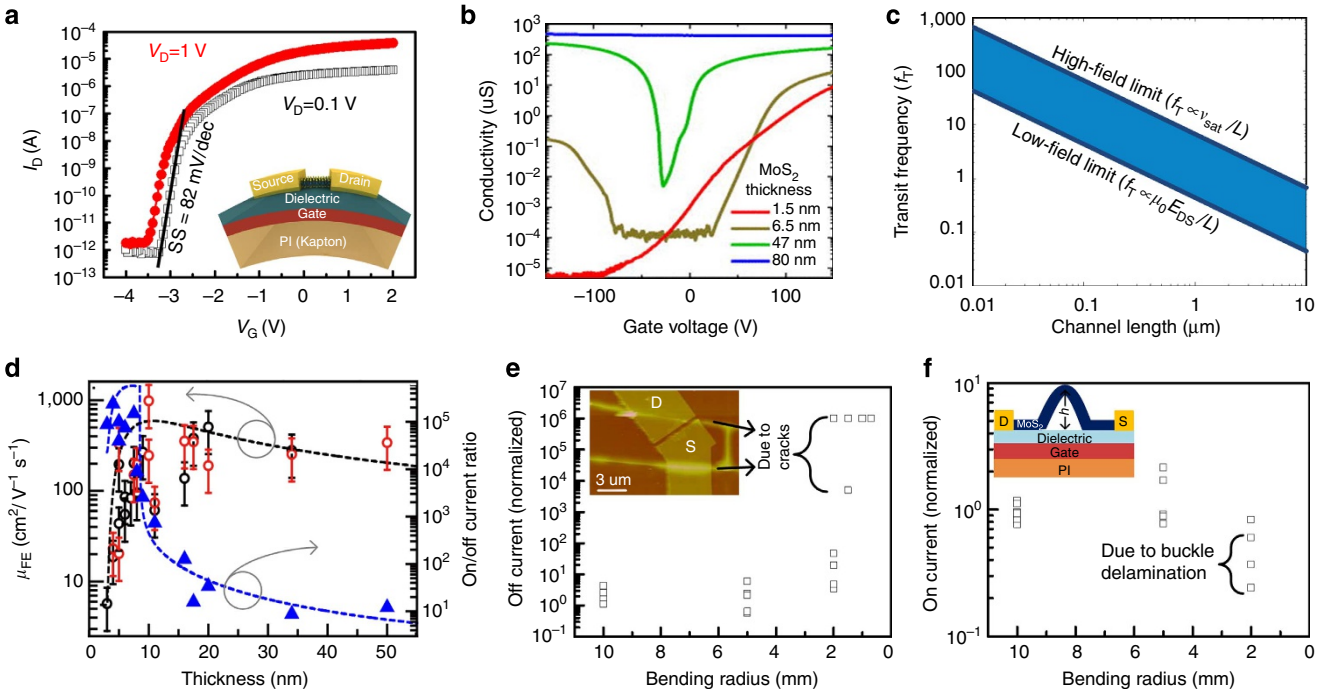

Figure 4 | High-performance room-temperature 2D TFTs. (**a**) Transfer characteristics of a multilayer MoS_2 FET ($W/L = 3/1\,\mu m$) with high-k gate dielectric featuring an on/off switching ratio $>10^7$ and sub-threshold slope (SS) of ~82 mV per decade fairly close to the ideal limit of 60 mV per decade. Inset is a schematic of the flexible device. (Adapted, with permission, from ref. 17 (copyright 2013 American Chemical Society.). (**b**) Conductivity as a function of gate voltage for four MoS_2 devices on PMMA surfaces. The peak field-effect mobilities are 30, 68 and 480 $cm^2\,V^{-1}\,s^{-1}$, corresponding to MoS_2 thicknesses of 1.5, 6.5 and 47 nm, respectively. Reproduced, with permission, from ref. 62 (copyright 2013, AIP Publishing LLC). (**c**) Estimated (intrinsic) transit frequency of TMDs based on equation (1) and constant-field channel length scaling. The low- and high-field limits are determined by the low-field mobility ($\mu_o \sim 30\,cm^2\,V^{-1}\,s^{-1}$, $f_T L \sim 0.4$ GHz-μm) and saturation velocity ($v_{sat} \sim 4 \times 10^6\,cm\,s^{-1}$, $f_T L \sim 6$ GHz-μm) respectively. (**d**) Reported carrier mobility (four-terminal, black circles; two-terminal, red circles) and drain current modulation (blue triangles) of phosphorene FETs of varying thicknesses. The dashed lines are derived from modelling. (Adapted from ref. 28.) (**e**) Mechanical studies of flexible MoS_2 FETs. Below 2 mm bending radius, the exponential increase in off current is due to cracks in the gate dielectric shown in the inset. (**f**) Similarly, the on current degrades, but primarily owing to buckling delamination, which is thickness dependent. Inset is an illustration of device buckling. (**e**,**f**) © 2013 IEEE. Reproduced, with permission, from ref. 58.

back-gated devices on SiO_2/Si and concluded that films around 10 nm thickness offered the highest mobility ($\sim 184\,cm^2\,V^{-1}\,s^{-1}$), owing to competing effects of interface screening and interlayer resistance. In contrast, Fuhrer and coworkers[62] evaluated multilayer MoS_2 TFTs with a polymer back-gate dielectric surrounding and found that ~ 47 nm thick film yielded the highest mobility ($\sim 480\,cm^2\,V^{-1}\,s^{-1}$) in their experimental study. Separate work by Javey and coworkers[16] demonstrated that a single layer of WSe_2 in a top-gated device structure can yield higher mobility ($\sim 250\,cm^2\,V^{-1}\,s^{-1}$) than reported for few-layer MoS_2.

Though differences in effective mass is a factor in carrier transport (W-TMDs have a lower effective mass than Mo-TMDs), theoretical studies by Ma and Jena[63] indicate that charged impurities and the effect of the top and bottom dielectric environment are prominent factors in contemporary experimental devices. Indeed, comparing the results of Appenzeller and Fuhrer suggests that is the case with TMD thickness and dielectric environment significantly influencing mobility and charge transport in fabricated TFTs. Intriguingly, the polymer environment on the thick MoS_2 device also afforded almost symmetric ambipolar electron and hole transport (Fig. 4b), a fairly rare occurrence for MoS_2 transistors. The inconclusive nature of experimental findings to date calls for continued investigation of TMD TFTs to further elucidate on the device physics and structures for accessing their maximum electronic performance.

A topic related to 2D materials that has yet to be thoroughly considered for the case of TMDs is the likely tradeoff between carrier mobility and the minimum contact resistance due to their opposite dependence on effective mass. On one hand, low effective mass is desirable for fast transport ($\mu \propto 1/m^*$). However, low effective mass also translates to low density of states, hence increasing the minimum contact resistance ($R_{c,min} \propto 1/\sqrt{m^*}$)[64] due to the reduced availability of states for charge injection. To the extent that this tradeoff holds true in scaled experimental devices (that is, extrinsic factors do not dominate the transport or contacts), then it might not be straightforward to directly determine the most suitable semiconducting TMD simply based on mobility alone. Additional studies are needed to shed light on the conditions for optimizing charge injection and transport.

High-frequency transport in 2D semiconducting crystals is an important performance metric for high-speed digital and RF electronics. Theoretical estimates for the intrinsic f_T can be derived from classical semiconductor physics based on the velocity (v) model, $v = \frac{\mu E_{DS}}{1+\mu E_{DS}/v_{sat}}$, (refs 27,36).

$$f_T = \frac{v}{2\pi L} \approx \frac{1}{2\pi}\left[\left(\frac{\mu E_{DS}}{L}\right)^{-1} + \left(\frac{v_{sat}}{L}\right)^{-1}\right]^{-1} \quad (1)$$

where the former term within the bracket defines the low-field limit and the latter term sets the high-field limit, governed by velocity saturation (v_{sat}). For low-power nanoelectronics, constant-field (E_{DS}) channel length scaling leads to a $f_T \propto 1/L$ dependence in both the low- and high-field limits. It is worthwhile to note that equation (1) depends on two material properties, low-field μ and v_{sat}, and can be universally applied to the portfolio of semiconducting 2D crystals. To gauge the range of intrinsic f_T that can be expected from TMD TFTs, we examine the case of a modest mobility ($\mu \sim 30\,cm^2\,V^{-1}\,s^{-1}$) for the low-end low-field limit, and a theoretically estimated $v_{sat} \sim 4 \times 10^6$ $cm\,s^{-1}$ (ref. 27) for the high-end high-field limit. Under this treatment, the expected f_T performance range is shown in Fig. 4c, essentially reflecting all mobility values above the low-end value and all velocities below the high-end value. It follows that the two limiting cases translate to two important performance values, $f_T L \sim 0.4$ GHz-μm and $f_T L \sim 6$ GHz-μm, for the low-end and high-end frequency performances, respectively. For channel lengths in the 100–250 nm range, the high-field f_T is in the microwave band, which is sufficient to realize high-speed digital and GHz circuits. Phosphorene offers mobilities as high as $1{,}000\,cm^2\,V^{-1}\,s^{-1}$ (Fig. 4d)[28] which will lead to higher intrinsic frequency performance compared to semiconducting TMDs. Indeed, phosphorene might very well be the most promising of the current portfolio of 2D semiconductors owing to its higher mobility while affording a suitable band gap[28,31].

However, to access the full high-frequency capability of 2D semiconductors, the effects of contact resistance, charge impurities and remote phonon scattering are detrimental device parameters that need to be minimized.

Device mechanics. Regarding mechanical flexibility, the limited studies on device mechanics have introduced an additional constraint relating to the question on the optimum thickness for flexible nanoelectronics. Chang *et al.*[17] evaluated the bendability of back-gated MoS_2 TFTs and found that the TFTs were robust down to a few mm bending radius followed by device failure initiated by two distinct thin-film mechanics[58], namely: (i) cracks in the dielectrics were responsible for off current degradation (Fig. 4e) and (ii) buckle delamination resulted in on current degradation as shown in Fig. 4f. The former can be mitigated by patterning the dielectric into islands, as has been demonstrated for graphene TFTs[59] or using ion-gel gate dielectrics[60].

Buckle delamination of MoS_2 shows a quasi-linear dependence of the buckling height on the film thickness[58], which can be attributed to the thickness dependence of the buckling driving force. It follows that a monolayer TFT is preferred from a device mechanics point of view, in contrast to the conclusion from mobility considerations that indicate a few layers are optimum[15], thereby suggesting a tradeoff in the number of layers that afford optimum device physics and device mechanics. This tradeoff might be mitigated by using high-quality h-BN gate dielectric where its atomic smoothness and high phonon energy are expected to enhance monolayer TMD mobilities as is the case for graphene[3,9]. Beyond bending studies, hydrostatic compressive strain of MoS_2 of about 15% has been recently reported to produce a semiconducting to metallic transition, which can enable new flexible or straintronic device or switch concepts[65].

Atomic sandwiches. Heterostructures composed of different atomic layers have been recently recognized as a new playground for material designers where the desired composite properties can be tailored and the whole can potentially be greater than the sum of its parts[1,2,9,66]. Synthesizing or preparing 2D heterostructures is currently a major research activity with increasing worldwide interest because of the seemingly unlimited range of application prospects. 2D heterostructures can enable flexible and transparent electronic, memory, optical, sensor and energy conversion devices. Recent work on soft substrates has focused on graphene-, h-BN- and TMD-layered heterostructures for flexible device applications[18,39,66]. The simplest and perhaps the most obvious heterostructure is a bilayer consisting of a stacked channel and dielectric such as graphene and its ideal dielectric, h-BN. The high phonon energies and thermal conductivity of h-BN can result in mobility enhancement and improved electronic performance[3,9,13]. For this reason, Lee *et al.*[39] realized a flexible device based on a monolayer graphene—multilayer h-BN heterostructure, which resulted in record 2D TFT current densities on plastics (Fig. 5a).

The next evolutionary development is a trilayer heterostructure that can draw from the individual properties of three different

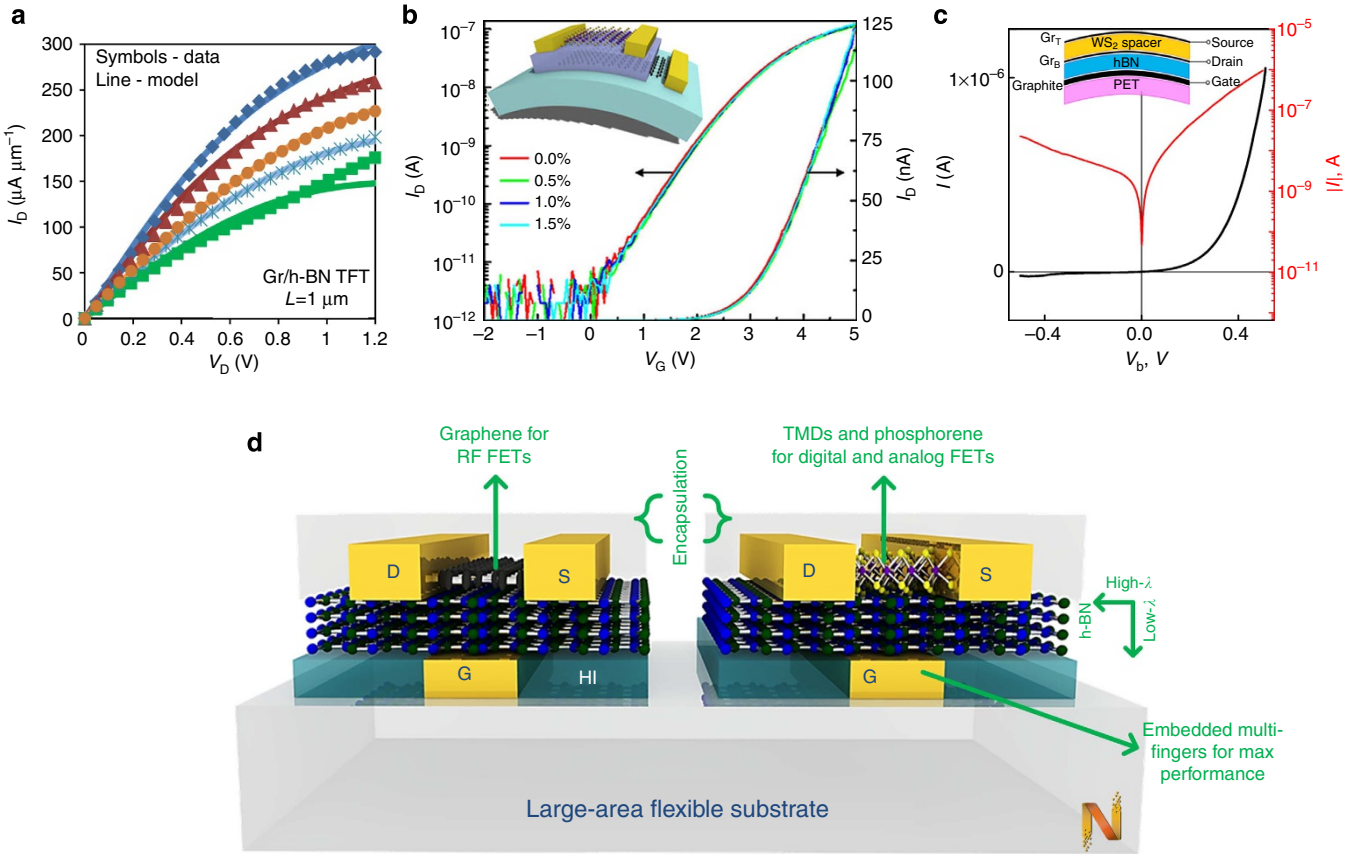

Figure 5 | Flexible 2D heterostructure devices. (**a**) Output characteristics of a TFT consisting of a graphene/h-BN channel/dielectric heterostructure stack on PI substrate showing soft current saturation and high current density. Gr: graphene. (© 2013 IEEE. Reproduced, with permission, from ref. 39.) (**b**) Transfer curves of a transparent trilayer TFT with a MoS_2 channel, h-BN gate dielectric and few-layer graphene gate electrode on PEN substrate featuring robust electronic properties under different bending conditions up to 1.5% strain. The inset shows the schematic diagram of the flexible device. Adapted, with permission, from ref. 18 (copyright 2013 American Chemical Society). (**c**) Room-temperature tunnel current of a five-layer flexible heterostructure vertical tunnel transistor. The data shown are at zero gate voltage and 20 mm bending radius. WS_2 thickness is around 3–10 layers. Schematic of the vertical transistor is shown in the inset. (Adapted from ref. 66.) (**d**) Simplified illustration of the proposed ideal integrated heterogeneous flexible device structure, which employs graphene for RF electronics and semiconducting TMDs or phosphorene for low-power complementary digital and analogue devices. h-BN is ideal as a multifunctional gate dielectric for mobility enhancement, high velocity saturation and thermal management of the channel heat based on its desirable anisotropic thermal conductivity (λ). A hydrophobic coating can preserve device performance. The embedded back-gate process can enable multiple gate fingers, low gate resistance and high current density. HI refers to an heat insulator.

atomic nanomaterials, such as TMD semiconductors, h-BN dielectrics and graphene electrodes. This offers the advantage of an intrinsically transparent transistor that benefits from the low absorption of the individual layers as demonstrated recently on polyethylene naphthalate (PEN) substrates[18] (Fig. 5b). Moreover, the source and drain electrodes that are typically metals can be replaced with single or few-layer graphene as contacts, which not only enables a fully transparent TFT but also improves the overall device flexibility and provides contact tunability of the graphene-channel Schottky barrier resulting in reconfigurable *n*- or *p*-type TFTs[33].

For field-effect tunnelling transistors, more complex 2D heterostructures are needed if one aims to realize the entire stack with layered materials. Mishchenko and co-workers[66] achieved this feat by sequential exfoliation and transfer of five different layers with graphite serving as the gate, h-BN as the dielectric, few-layer WS_2 electron tunnel barrier and monolayer graphene contacts, as illustrated in Fig. 5c. As materials growth advances, integration of layered sheets for heterostructure realization will become more manufacturable and enable comprehensive studies for flexible nanoelectronics.

Bendable challenges

In light of the outstanding potential for 2D atomic sheets for advanced flexible nanoelectronics, it is prudent to balance this perspective with a discussion of the pressing challenges that need to be addressed before Si-like large-scale integration and performance can be realized on soft substrates. Foremost amongst these challenges is the need for research and development of complementary *n*- and *p*-type 2D transistors. Complementary transistor technology has been the foundation of modern low-power integrated electronics for the past five decades. Any practical vision for integrated flexible smart systems will require complementary TFTs for essential circuits, including bias circuitry, data converters, signal processing blocks and microprocessors.

Much of the progress on semiconducting atomic sheets have so far found that intrinsic 2D semiconductors typically exhibit either *n*- or *p*-type device transport[1,2,15,16,67], instead of ambipolar behaviour expected in the absence of intentional doping[68]. A case in point is MoS_2 and $MoSe_2$, which typically afford *n*-type FETs, even when high work function contacts that should theoretically favour hole transport are used[1,12,67]. Likewise, WSe_2

and phosphorene typically afford *p*-type FETs[16,28,31]. For TMDs, this observation has been attributed to a variety of factors including Fermi level pinning at the contacts[15] and material defects such as vacancies or interstitials that can result in *n*- or *p*-type defect levels[69]. Also, one can expect contaminants and adsorbates from the ambient and lithography process to influence the device polarity, in addition to the observed effects of certain dielectric interfaces (for example, polymeric or ion-gel dielectrics), which are not yet well understood[60,62]. Clearly, sustained research is warranted in terms of synthesizing high-purity materials with negligible defects and continued studies in understanding the contact—2D and dielectric—2D interfaces to achieve the desired carrier transport.

It should be noted that conventional substitutional doping of the 2D semiconductor channel is generally not envisioned as a viable technique for controlling carrier type, owing to the high likelihood of crystal damage and mobility reduction. Similar to the case of semiconducting carbon nanotubes, contact engineering is regarded as a suitable method based on low or high work function electrode interfaces to obtain *n*- and *p*-type FETs, respectively[12]. Moreover, the gate electrode can be selected to tune the threshold voltage. Alternatively, self-assembled monolayers can be applied to polymer substrates to effectively dope overlaying graphene layers[70]. Such doping can be spatially controlled by patterning of the self-assembled monolayers.

Facing the heat barrier. Soft substrates cannot tolerate heat compared with bulk semiconductors or ceramics that typically have melting temperatures much higher than practical device operating temperatures. For this reason, thermal management is a more pronounced challenge for flexible electronics, particularly for 2D channel materials in which high current densities needed for the maximum speeds can lead to peak temperatures that are comparable to or can exceed the glass transition temperature of plastic substrates. In the case of graphene, channel hotspots from Joule heating can exceed 300 °C (ref. 71), which results in plastic substrate deformation and irreversible device damage[58] (Fig. 6a). Typical power density limits for bottom-gated GFETs are $\sim$20 kW cm^{-2} (0.2 mW μm^{-2}) and $\sim$45 kW cm^{-2} on PEN and PI substrates, respectively. Overcoming the heat barrier requires use of thermal management materials to prevent the substrate from experiencing temperatures beyond its reliable limit. It is significant to note that the overall RF performance (for example, gain and cutoff frequencies) of flexible graphene TFTs is ultimately limited by thermal constraints of the substrate rather than by electronic characteristics of the device.

Unlike conventional electronics where the substrate is thermally conductive and metallic heat sinks can be used, most flexible substrates are poor thermal conductors, and there is very limited research on strategies for thermal management. Lee *et al.*[58] proposed employing h-BN for thermal management, because its anisotropic thermal properties (Table 1) appear to be ideal for in-plane heat spreading to metal contacts and out-of-plane heat isolation as depicted in Fig. 5d. The main question regards the minimum h-BN thickness required to ensure that the substrate stays within its reliable temperature range during high-field TFT operation. In general, the minimum h-BN thickness will depend on the maximum channel temperature, channel thermal conductivity, channel—h-BN thermal interface resistance, substrate T_g, radiation efficiency to the ambient and channel length, with shorter channels providing increased assistance in heat spreading to the contacts. An alternative material stack that achieves a similar goal of anisotropic thermal management can be constructed from a bilayer film with thermally conductive (for example, BeO) and insulating thin layers facing the hot channel and soft substrate, respectively. Ongoing research on thermal management for flexible nanoelectronics is expected to provide guidance for reliable device design and optimum operation.

Rolling forward

Large-scale nanomanufacturing of 2D thin films and devices on soft substrates is an essential prerequisite for practical flexible nanoelectronics. In this regard, much of the public and technical imagination has focused on nanomanufacturing based on sheet or roll-to-roll (R2R) processing[72,73] for large-area or high-volume nanotechnology that can be as ubiquitous as modern Si very large-scale integration. Either nanomanufacturing method will be rather complex, involving material growth, transfer and lithography in a benign manner to minimize contamination and defects (Fig. 6b). Defects present in 2D semiconductors and dielectrics grown by chemical vapour deposition and subsequently transferred onto process substrates encompass: (i) growth-related crystal imperfections such as vacancies, interstitials, grain boundaries and slip planes in multilayer films and (ii) process related defects such as wrinkles, bubbles, tears and chemical contamination.

For the manufacturing of graphene, large-area growth and R2R processing has experienced substantial progress in the last few years[55,56], as depicted in Fig. 7a,b showing the state-of-the-art in graphene R2R that has enabled 100 m long transparent conductive rolls[73]. Indeed, graphene has recently penetrated the consumer market replacing indium tin oxide as the touch screen panel in some smart phone products in China (Fig. 7c). The current flexible technology maturity of 2D sheets is summarized in Fig. 7e revealing several demonstrated advances of large-area graphene in contrast to the emerging 2D nanomaterials which are

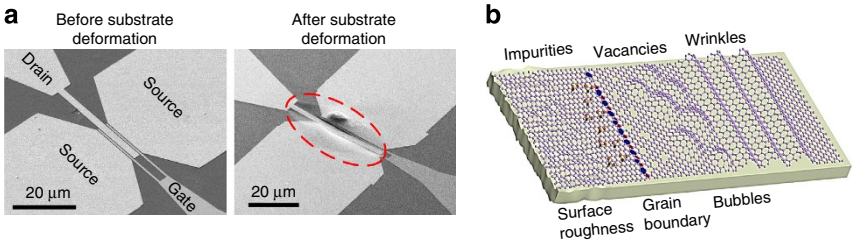

Figure 6 | Device and material challenges. (**a**) Scanning electron microscope images of flexible back-gated graphene FET devices before and after irreversible damage from PEN substrate deformation due to Joule heating at high electric fields. The heat-affected zone in the vicinity of the device channel is highlighted by the dashed region for clarity. Measured power density limit is $\sim$0.2 mW μm^{-2} for a device with 500 nm channel length, source-drain spacing of 900 nm and 6 nm thick high-*k* gate dielectric. (**b**) Examples of material defects commonly found in synthesized and transferred large-area graphene sheets on soft substrates (courtesy of Dr Young Duck Kim). For flexible integrated nanoelectronic systems, minimizing materials defects is essential for yield, cost, performance and reliability.

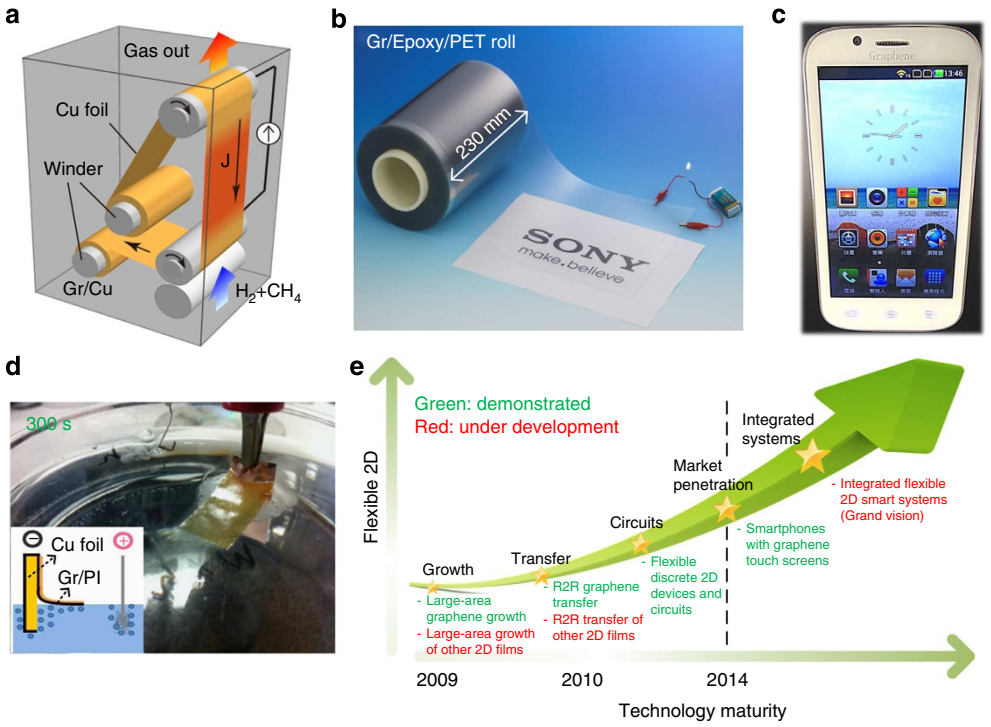

Figure 7 | Large-scale nanomanufacturing. (**a**) A scheme for continuous R2R growth of graphene based on selective Joule heating of copper foil. Gr: graphene. (**b**) The growth is followed by R2R coating and bonding to PET, and finally, the spray etching of the copper substrate to manufacture 100 m long transparent conductive graphene/plastic rolls. (**c**) Large-scale manufacturing of graphene has enabled smart phones with graphene touch screens, which are now sold in China (Image courtesy of 2D Carbon Tech). (**d**) Experimental demonstration of electrochemically delaminated graphene onto PI that affords reuse of Cu foil for a sustainable nanomanufacturing technology. Inset is an illustration of the electrochemical method. Reproduced, with permission, from ref. 74 (© 2013 WILEY-VCH Verlag & Co. KGaA, Weinheim). (**e**) Simplified technology maturity perspective for flexible 2D nanotechnology. Growth, transfer and circuits based on graphene have been demonstrated leading to the 2013–2014 market penetration of graphene as smart phone touch panels. The large-scale advancement of graphene is expected to benefit the progress of other 2D sheets, and graphene's market penetration can be a launch pad for the commercial development of fully integrated flexible smart systems using 2D materials for both passive and active devices. (**a**,**b**) Reproduced with permission from ref. 73. (copyright 2013, AIP Publishing LLC).

still at a nascent stage. We expect that much of the progress in graphene R2R development will benefit the nanomanufacturing of other 2D atomic sheets with substantial advancement needed in terms of: (i) understanding and minimizing crystal grain boundaries, defects and doping[1,2,69] and (ii) development of large-area growth techniques and benign transfer integration onto soft substrates[2]. It is worth noting that current graphene R2R transfer is based on the complete etching of copper foils, a scheme that may be unsustainable for cost, scale, or waste processing reasons. Alternative transfer methods that show strong promise include electrochemical and dry delamination, both of which preserve the foil for reuse[74,75]. Figure 7d demonstrates recent electrochemical delamination of graphene directly onto PI.

Direct growth or integration of assorted layers of 2D semiconductors, dielectrics and conductors is of course the ideal method for realizing high-performance integrated flexible smart systems, which is a grand technology vision for 2D materials as stated in Fig. 7e. We anticipate that flexible smart systems will likely be commercial products over the next 10 years based on the rapid progress so far, which is generally in-line with the time frame of the 10-year EU Graphene-Flagship project (http://graphene-flagship.eu/).

We note that carbon nanotube is another candidate nanomaterial that is under development for flexible nanotechnology. Nanotube smart phone touch panels (produced by Tianjin's CNTouch (http://www.cntouch.com/) in China) have also recently penetrated the consumer market in 2014 and directly competes with graphene as an indium tin oxide replacement. Moreover, flexible integrated systems based on nanotubes have been demonstrated[12,76,77]; however, it is too early to determine how nanotubes will fare with 2D films for commercial flexible systems. At present, graphene has experienced a more rapid large-scale development in transitioning into the touch panel market given that nanotubes have been researched for longer. The challenge facing nanotubes produced by large-scale manufacturing is the need for both high tube density and carrier mobilities while affording sufficiently large on/off ratios for high-performance transistors[12], a long-standing research topic.

We conclude by noting that research on flexible 2D atomic sheets began only a few years ago, with the first papers on flexible graphene, flexible TMD and phosphorene transistors in 2007, 2012 and 2014, respectively. In this time frame, the achieved electronic performance has already substantially exceeded those of organic, amorphous and metal oxide thin-film transistors that have enjoyed decades of research activity. The remarkable high mobility of few-layer phosphorene, which is superior to that of TMDs and silicon TFTs could have a transformational impact in enabling flexible high-performance electronics. The recent graphene penetration of the consumer smart phone market is a major milestone and could be a launch pad for the development of large-scale active electronics. The path to further commercialization is, of course, not exactly predictable. However, sustained research effort that address the major challenges will be indispensable in translating the potential of 2D nanomaterials into a practical high-performance flexible ubiquitous nanotechnology.

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