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Review Article

Integrating MEMS and ICs

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The majority of microelectromechanical system (MEMS) devices must be combined with integrated circuits (ICs) for operation in larger electronic systems. While MEMS transducers sense or control physical, optical or chemical quantities, ICs typically provide functionalities related to the signals of these transducers, such as analog-to-digital conversion, amplification, filtering and information processing as well as communication between the MEMS transducer and the outside world. Thus, the vast majority of commercial MEMS products, such as accelerometers, gyroscopes and micro-mirror arrays, are integrated and packaged together with ICs. There are a variety of possible methods of integrating and packaging MEMS and IC components, and the technology of choice strongly depends on the device, the field of application and the commercial requirements. In this review paper, traditional as well as innovative and emerging approaches to MEMS and IC integration are reviewed. These include approaches based on the hybrid integration of multiple chips (multi-chip solutions) as well as system-on-chip solutions based on wafer-level monolithic integration and heterogeneous integration techniques. These are important technological building blocks for the 'More-Than-Moore' paradigm described in the International Technology Roadmap for Semiconductors. In this paper, the various approaches are categorized in a coherent manner, their merits are discussed, and suitable application areas and implementations are critically investigated. The implications of the different MEMS and IC integration approaches for packaging, testing and final system costs are reviewed.

Keywords: cofabrication platforms; integrated circuits (ICs); microelectromechanical system (MEMS); More-Than-Moore; multi-chip modules (MCMs); system-in-package (SiP); system-on-chip (SoC); three-dimensional (3D) heterogeneous integration

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1 INTRODUCTION

Microelectromechanical system (MEMS) and emerging nanoelectromechanical system (NEMS), henceforth both referred to as 'MEMS', are typically transducer systems that sense or control physical, optical or chemical quantities, such as acceleration, radiation or fluids. A MEMS device typically interacts with a physical, chemical or optical quantity and has an electrical interface to the outside world. For MEMS sensors, the electrical output signal correlates with the physical, optical or chemical input quantity that is sensed. In the case of MEMS actuators, an electrical input signal is used to control one or more physical, optical or chemical quantities. To enable the MEMS transducer to perform useful functions, the electrical interface with the outside world is, in most cases, realized through integrated circuits (ICs) that provide the system with the necessary intelligence. ICs may provide signal conditioning functions such as analog-to-digital conversion, amplification, temperature compensation, storage or filtering as well as system testing and logic and communication functions. The International Technology Roadmap for Semiconductors[1] describes the addition of MEMS functionalities to ICs as an important 'More-Than-Moore' technology.

As illustrated in Figure 1, MEMS and ICs can be integrated using two basic methods: (1) In the general approach referred to here as a multi-chip solution, MEMS and IC components are manufactured on separate substrates using dedicated MEMS and IC processes and are subsequently hybridized in the final system. Two-dimensionally or side-by-side integrated systems are often referred to as multi-chip modules. When chips are vertically stacked in a package in this way, such a system is also referred to as a system-in-package or a vertical multi-chip module[2]. Devices created through vertical stacking of several IC chips are also referred to as three-dimensional integrated circuits (3D ICs)[3]. (2) In the general approach referred to here as a system-on-chip (SoC) solution, MEMS and IC components are manufactured on the same substrate, using consecutive or interlaced processing schemes.

For both multi-chip solutions and SoC solutions, numerous technological schemes have been proposed, and the research community and industry continue to develop new manufacturing and integration schemes at a rapid pace. Each of the two basic methods of combining MEMS and ICs offers distinct advantages and disadvantages, and the preferred solution depends strongly on the device, the field of application and the product requirements. Based on recent MEMS market studies[4,5], we estimate that approximately half of all existing MEMS products (in terms of market value) are currently implemented as multi-chip solutions (including many accelerometers, gyroscopes, microphones, pressure sensors, RF MEMS and microfluidic devices) and that the other half are implemented as SoC solutions (including digital mirror devices, infrared bolometer arrays, inkjet printheads, and certain gyroscopes, accelerometers and pressure sensors). Many of the MEMS products that are implemented as SoC solutions have the common feature that they consist of large transducer arrays in which each transducer is operated individually, and thus, the integration of each MEMS transducer and its associated IC on a single chip is the only practical way to implement these types of systems. However, there are also other products, including certain gyroscopes, accelerometers, microphones and pressure sensors, that are implemented as SoC solutions. The commonality among

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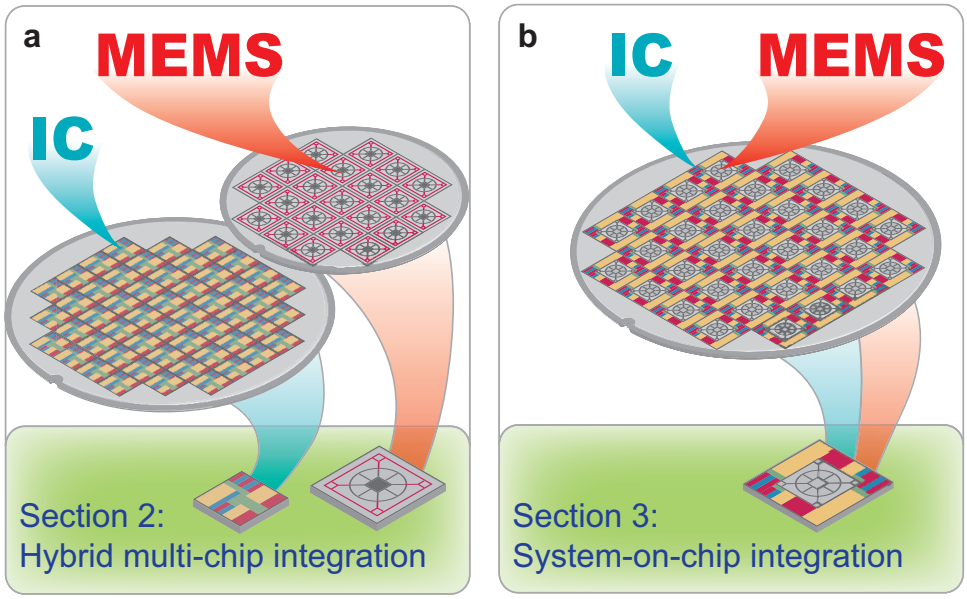

Figure 1 MEMS and IC integration methods are based on either (**a**) hybrid multi-chip solutions (described in Section 2) or (**b**) system-on-chip solutions (described in Section 3).

these products is that they are relatively mature products that are manufactured and sold in very high volumes.

The existing literature contains several reviews of important technologies for the cofabrication of MEMS and electronics on the same substrate (by Fedder *et al*[6], Brand[7] and French *et al*[8]). Several review articles on heterogeneous integration technologies for MEMS have also been published[9–12]. In contrast to previous work, the present paper provides a comprehensive, up-to-date overview and comparison of the available technologies for integrating MEMS and ICs, both for (1) hybrid multi-chip solutions and (2) SoC solutions. Established and emerging technologies for the integration of MEMS and ICs are reviewed, analyzed and categorized in a coherent manner, and their implementation in MEMS products is discussed. MEMS packages must provide either a hermetically sealed environment (e.g., for resonators, inertial sensors and IR imaging sensors) or a physical interface to the ambient environment (e.g., for microphones, pressure sensors and flow sensors). The packaging of MEMS is not the subject of the present review; however, this topic is discussed in a number of review articles[13–16] and in books by Hsu[17], Tummala[18], Lau[19] and Madou[20].

2 HYBRID INTEGRATION OF MEMS AND ICS: MULTI-CHIP SOLUTIONS

In recent decades, hybrid integration of MEMS and IC technology has been dominated by 2D integration approaches. In such an approach, the MEMS and IC wafers are designed, manufactured and tested independently. The wafers are then separated into discrete chips and eventually integrated into multi-chip systems at the board or package level. Historically, MEMS and IC chips have been packaged individually and then integrated as a system onto a printed circuit board (PCB). This led to the development of multi-chip modules in which, as shown in Figure 2, MEMS and IC chips are placed side-by-side in a common package and interconnected at the package level, typically via wire and/or flip-chip bonding. In wire bonding, a highly automated micro-welding process for metal wires is employed to create chip-to-chip and chip-to-package interconnects[21]. In flip-chip bonding, solder balls or stud bumps are placed on pads on the topside of a chip. The chip is then flipped upside down and aligned with and attached to the package substrate or another chip via pick-and-place soldering. Both the wire and flip-chip bonding processes employ temperature, force and/or ultrasonic energy in the joining

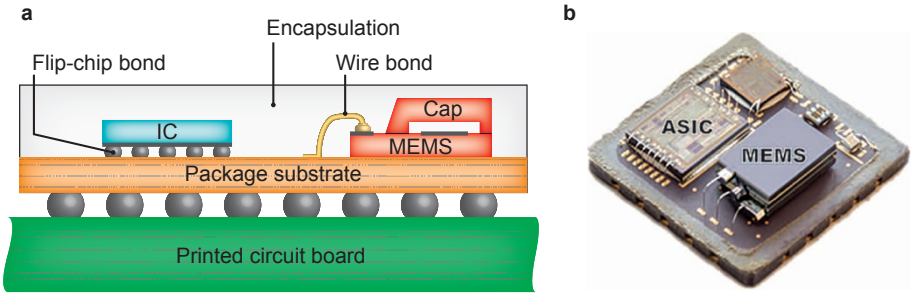

Figure 2 (**a**) 2D side-by-side integration with flip-chip and wire bonded interconnections. (**b**) Photograph of a decapsulated Colyibrys MS9000-series accelerometer (Colibrys Ltd, Yverdon-les-Bains, Switzerland). ASIC and passive chips are placed side-by-side with an encapsulated MEMS chip. All chips have wire bonded interconnections. Package dimensions: 8.9 × 8.9 × 3.2 mm^3.

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process. While wire bonds serve merely as electrical interconnects, flip-chip bonds can double as physical chip attachments and electrical interconnects. Several concepts for MEMS and IC integration through flip-chip bonding are being used in applications such as RF-MEMS[22], micro-opto-electro-mechanical system[23–25] and MEMS sensors[26,27], and a general study investigating various MEMS test structures has been reported[28]. More recent concepts for chip-to-chip and chip-to-package interconnections have been developed based on thin-film interconnects between embedded chips[29–33]. This method has been commercially exploited in fan-out wafer-level packaging concepts, including the wafer-level ball grid arrays developed by Infineon and there distributed chip packages developed by Freescale Semiconductor Inc, Austin, Texas, USA[34]. Other unconventional chip-to-chip interconnection methods include mechanically flexible interconnects[35] and quilt packaging, in which chips with different functionalities are tiled in close proximity on the package substrate and are interconnected by vertical facets protruding from each chip[36].

Multi-chip modules have a significantly reduced signal path length between chips and occupy a lesser area of PCB real estate compared with system-on-board approaches, in which discrete components are integrated on a PCB. Thus, this concept is broadly applied both in research[37–42] and in commercial products[27,39]. In particular, the integration of MEMS chips with commercially available standard application-specific integrated circuits (ASICs) enables the extremely simple, rapid and cost-efficient implementation of hybrid systems[41].

As shown in Figure 3, system-in-packages, also referred to as vertical or stacked multi-chip modules, consist of chips that are attached on top of each other and interconnected via wire and/or flip-chip bonding, either directly[43,44] or through additional re-distribution layers[45]. The main benefits of these 3D-stacked approaches are their higher integration densities, shorter signal path lengths and smaller package footprints/volumes in comparison with multi-chip modules. This method enables chip-to-wafer stacking[43,44,46] and is employed both in research[47–50] and in a large number of commercial products, such as accelerometers and pressure sensors[51–53].

As shown in Figure 4, the chip-scale package and wafer-scale package concepts yield very compact packages with footprints similar to the size of the largest chip involved. An example of this approach is the chip-on-MEMS technology that has been commercialized by Murata Electronics Oy, Finland (formerly VTI Technology Oy, Vantaa, Finland). Here, IC chips are attached to larger, encapsulated MEMS devices at the wafer level via flip-chip bonding (chip-to-wafer bonding). After dicing, the chip-stack is again flip-chip bonded directly to the PCB, as depicted in Figure 4a. Similar approaches have been reported by Premachandran *et al*[55], Tian *et al*[56] and Sugizaki *et al*[57]. Such compact integration concepts require vertical through-substrate vias, known as through-silicon vias or through-glass vias, depending on the substrate used. Through-substrate vias enable even shorter signal path lengths with superior electrical characteristics in terms of lower capacitive, resistive and inductive parasitic effects. Through-substrate vias have already been commercially implemented in a number of products, such as MEMS-microphones[58] and RF-filter and RF-switch devices[59,60].

System-on-package approaches are another alternative that enables highly integrated and miniaturized system technology at the package level. Here, MEMS and IC devices are integrated with a broad spectrum of other basic technologies, ranging from optics and power electronics to wireless components, in a

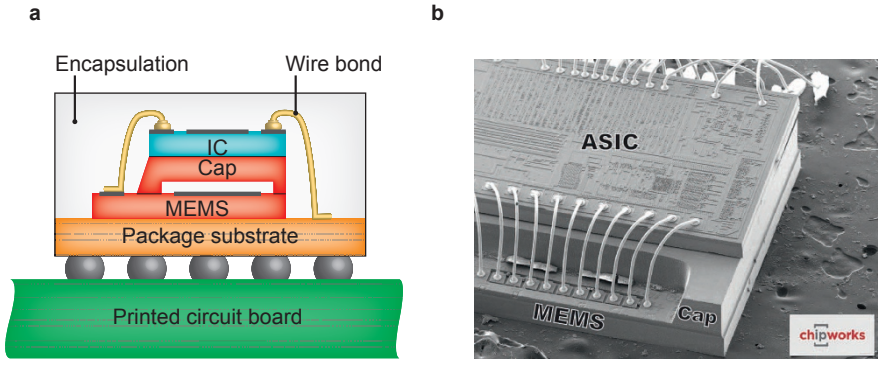

Figure 3 (**a**) System-in-package solution constructed via 3D stacking with wire bonded interconnects. (**b**) SEM image of a decapsulated STMicroelectronics LIS331DLH 3-axis accelerometer (STMicroelectronics, Geneva, Switzerland). An ASIC chip is stacked on an encapsulated MEMS chip and interconnected via wire bonds. Package dimensions: 3 × 3 × 1 mm^3. From Ref 54.

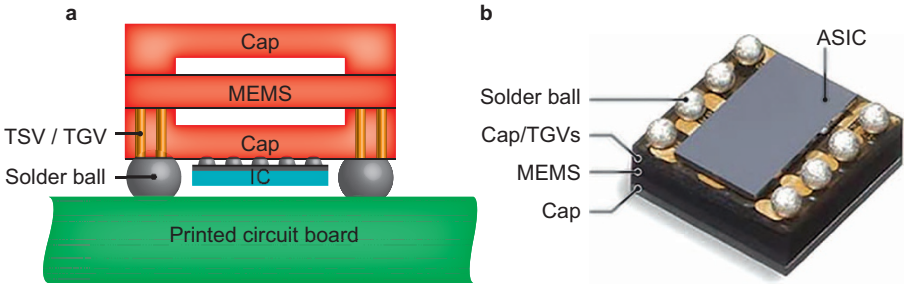

Figure 4 (**a**) Chip-scale package (CSP): the MEMS and IC chips are attached via face-to-face flip-chip bonding. (**b**) Photograph of a 3-axis accelerometer (VTI, CMA 3000) fabricated using chip-on-MEMS technology. Package dimensions: 2 × 2 × 1 mm^3. From Ref 61.

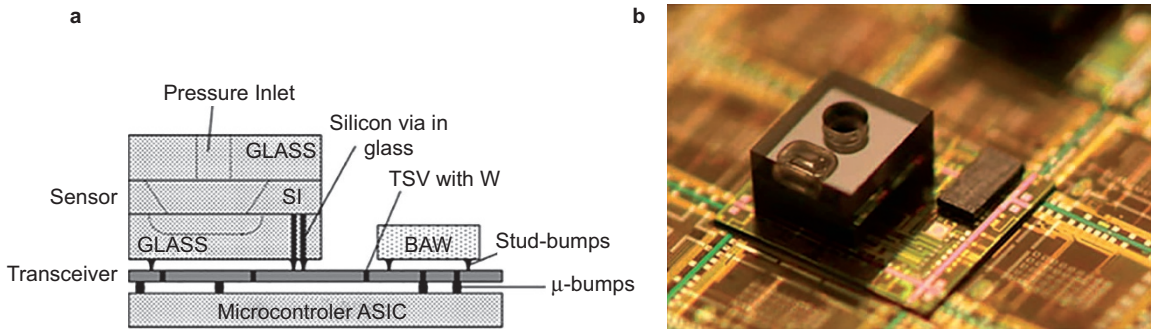

Figure 5 (**a**) Sketch of a 3D sensor node stack fabricated using through-silicon vias. (**b**) Photograph of a 3D sensor node stack fabricated using through-silicon vias at the wafer level. From Ref 62.

common package[2]. As shown in Figure 5, complete sensor nodes comprising chip-level MEMS, ASIC, wireless communication and power management components are 3D integrated at the package level[62,63].

In summary, the key advantages of multi-chip solutions are their modularity, high flexibility and reasonably low fabrication complexity. In these approaches, the MEMS and IC manufacturing processes are completely decoupled, which results in full freedom of the design approaches and technology used for both the MEMS and IC chips. This enables rapid development cycles (short time-to-market) and relatively low development costs. The product specifications can easily be modified because the IC and MEMS chips are interchangeable. For the IC chips, the migration from one CMOS technology node to another, more advanced CMOS technology node can be readily implemented. Furthermore, the combined cost of a MEMS chip and the associated IC chip is not significantly impacted if there is a size difference between the MEMS and IC chips, as they are manufactured on separate wafers such that the maximum number of chips is fabricated on each wafer. Only tested (known-good) MEMS and IC chips are then packaged. Typically, the pre-packaging or sealing of MEMS structures is implemented at the wafer level, thus reducing the complexity of the final system. The manufacturing and testing infrastructure that is available from the semiconductor industry can be readily utilized for multi-chip solutions. Finally, technology, design and packaging standards can be established in a fairly simple manner for multi-chip solutions. The typical disadvantages of multi-chip solutions are their limited integration densities, large system footprints and thicknesses. Long electrical chip-to-chip connections can result in rather large parasitic capacitances and in the reduced robustness of electromagnetic compatibility (EMC), which can be a key disadvantage for certain devices, such as capacitive transducers. In addition, multi-chip solutions contain two or more chips per module, which can be a disadvantage in certain industries, such as the automotive industry, in which quality standards require the tracking of individual chips throughout the lifecycle of a product.

3 WAFER-LEVEL INTEGRATION OF MEMS AND ICS: SOC SOLUTIONS

The cofabrication of MEMS and IC components on a single substrate has been investigated for over three decades. Historically, however, few of those fabrication approaches have found their way into the industry. Only recently have various products implemented as SoC solutions, such as pressure sensors, inertial sensors, and microphones, been successfully commercialized.

SoC solutions are characterized by the fabrication and integration of MEMS and IC components on the same substrate, with chip separation occurring only at or near the end of the fabrication process. In general, SoC solutions can be categorized into two main integration schemes: (1) monolithic MEMS and IC integration techniques, as presented in Section 3.1, in which both the MEMS and IC structures are fabricated entirely on the same substrate and (2) heterogeneous MEMS and IC integration techniques, as presented in Section 3.2, in which the MEMS and IC structures are fully or partially prefabricated on separate substrates and subsequently merged onto a single substrate, typically via wafer bonding or similar transfer techniques.

3.1 SoC solutions using monolithic MEMS and IC integration

SoC solutions based on monolithic MEMS and IC integration can be categorized into four basic approaches: (1) monolithic MEMS and IC integration using MEMS-first processing, (2) monolithic MEMS and IC integration using interleaved MEMS and IC processing, (3) monolithic MEMS and IC integration using MEMS-last processing via the bulk micromachining of the IC substrate (also sometimes referred to as CMOS-MEMS) and (4) monolithic MEMS and IC integration using MEMS-last processing via layer deposition and surface micromachining.

3.1.1 Monolithic MEMS and IC integration using MEMS-first processing

Monolithic MEMS and IC integration using MEMS-first processing is an integration approach in which all required processing steps for a complete MEMS device are performed prior to the CMOS processing, typically including substrate planarization to enable subsequent CMOS integration. This allows for a very high thermal budget of greater than 1100 °C for the processing of the MEMS material, which enables the use of high-temperature processes, to obtain high-performance epitaxial silicon or to release stress in thick layers of deposited poly-crystalline silicon layers, for example. Examples of MEMS-first processing schemes are illustrated in Figure 6 and 7.

Figure 6 illustrates the advanced porous silicon membrane process developed by Robert Bosch GmbH, Stuttgart, Germany, which is an innovative method for manufacturing vacuum cavities sealed with monocrystalline silicon membranes in silicon wafers[64–67]. In this process, localized porous silicon is created via anodic etching in hydrofluoric acid (HF). A subsequent annealing step in a hydrogen atmosphere at 900–1100 °C initiates a sintering process, causing the low-porosity layer near the surface to recrystallize and the high-porosity layer below to dissolve. An epitaxial silicon layer is then grown on top of the wafer, simultaneously creating a monocrystalline membrane and a high-quality silicon surface for CMOS fabrication. At present, Bosch is successfully fabricating pressure sensors for automotive

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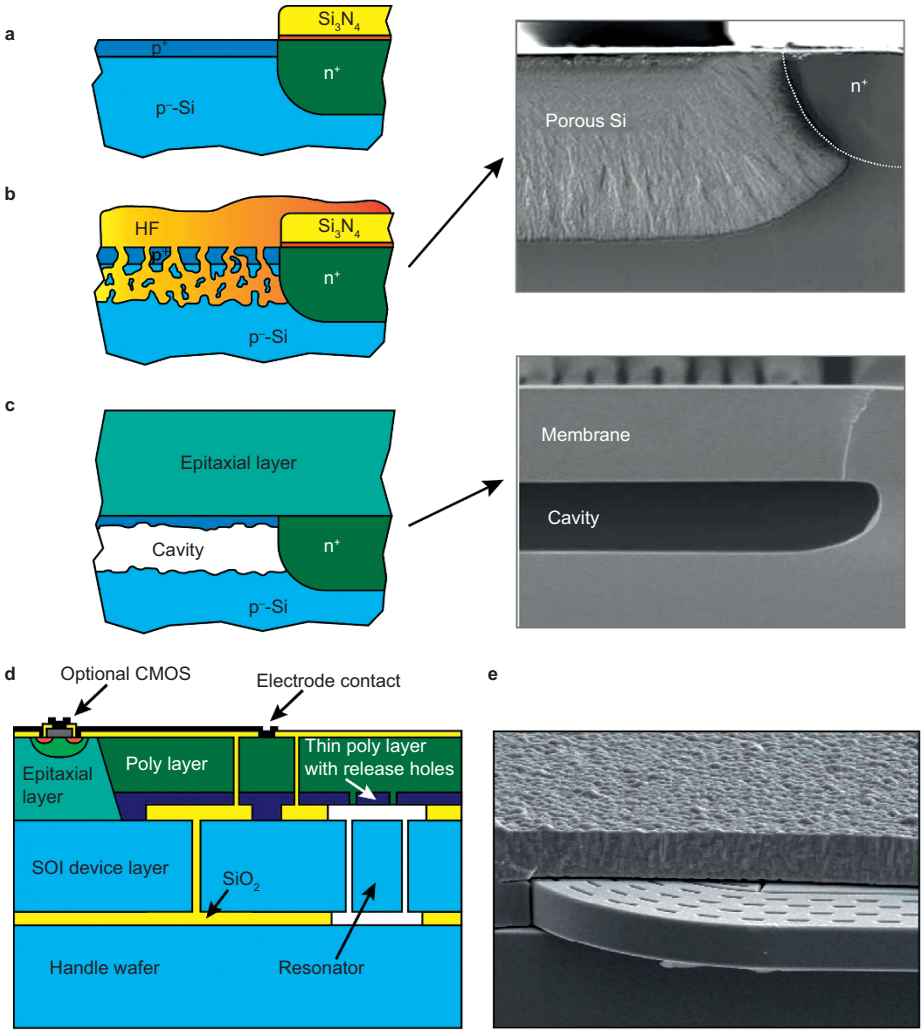

Figure 6 (**a**–**c**) Advanced porous silicon membrane (APSM) process developed by Bosch. (**a**) n^+ and p^+ implantation. (**b**) Anodic HF etching. (**c**) Sintering to form a cavity and a silicon epitaxial layer. Adapted from Ref 65 and Ref 66. (**d**–**e**) Similar MEMS-first platform developed by SiTime (now MegaChips, Japan) and Stanford University. MEMS structures are fabricated in the SOI device layer and released by means of HF vapor etching. The ICs are fabricated in the epitaxially grown silicon top layer. (**d**) Schematic cross-section. (**e**) SEM image of a fabricated resonator[72].

applications using this method. Bosch's advanced porous silicon membrane process has been further developed using SOI substrates manufactured by SiTime Corp., Sunnyvale, CA, USA (now MegaChips, Japan) and Stanford University, CA, USA[68–70]. After the MEMS structures are patterned into the silicon device layer, the structures are encapsulated by an SiO_2 layer and a thin poly-silicon layer, as depicted in the schematic view in Figure 6d. Small vent holes, which allow for the release of the MEMS structures by means of HF vapor etching, are created in the poly-silicon layer. The vent holes are subsequently sealed by an additional epitaxial deposition of silicon. In areas outside the MEMS structures, the epitaxy process creates monocrystalline silicon, providing a high-quality material for CMOS fabrication. Figure 6e shows an SEM picture of a fully fabricated MEMS resonator structure. SiTime has successfully applied this MEMS-first process in high-volume fabrication of MEMS resonators for timing products[71].

Another MEMS-first platform is the 'plug-up' process developed by VTT, which has found commercial application in pressure sensors[73–75]. As shown in Figure 7, this process is based on an SOI substrate in which cavities are formed via HF etching of the buried oxide through small holes in the silicon device layer that are covered by an HF-permeable layer of poly-silicon. The holes are then filled with another layer of poly-silicon, and the surface is planarized via chemical-mechanical planarization (CMP) to expose the monocrystalline surface, onto which the CMOS circuits can then be integrated.

In summary, MEMS-first integration approaches offer favourable conditions for MEMS fabrication, such as a very high thermal budget. This allows for the fabrication of high-performance MEMS structures and hermetically sealed packages of superior quality, which is why this technology is used for products such as high-performance MEMS resonators. However, there are strict requirements on the surface planarity and material exposure of the pre-processed MEMS wafers. Typically, it is not permitted for pre-processed wafers to be brought into standard CMOS fabs, which is why this approach is utilized predominantly by companies that have access to a dedicated CMOS fab. For the same reason, this approach is impractical in fabless business models.

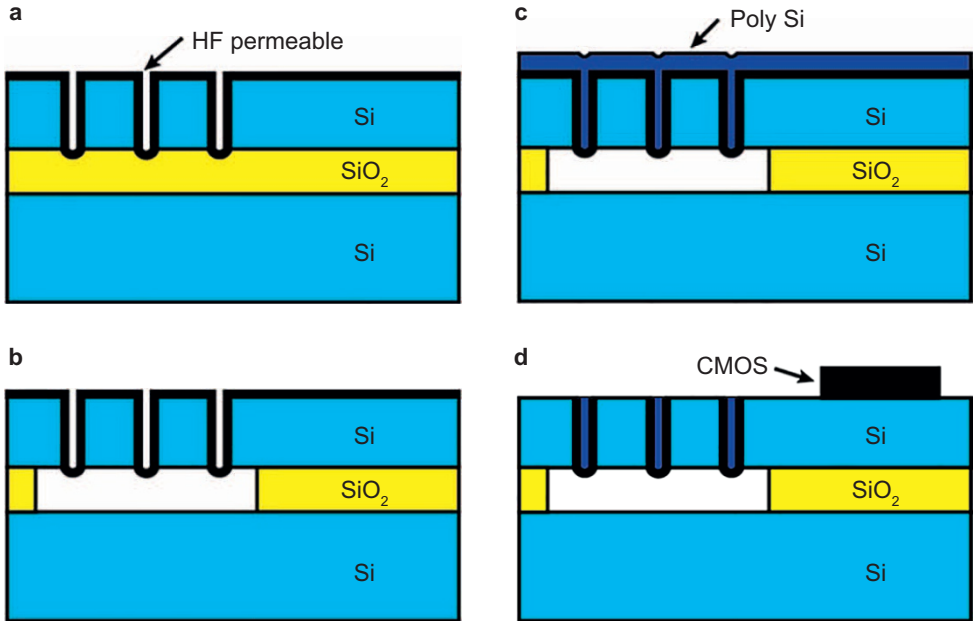

Figure 7 Processing sequence for the 'plug-up' concept. (**a**) Small holes are etched, and a thin HF-permeable poly-silicon layer is deposited. (**b**) The buried oxide is etched with HF. (**c**) The holes are closed via the deposition of poly-silicon. (**d**) CMP followed by CMOS processing. Adapted from Ref 73.

3.1.2 Monolithic MEMS and IC integration using interleaved MEMS and IC processing

Monolithic MEMS and IC integration using interleaved MEMS and IC processing is achieved through a combination of MEMS processing steps performed before, after, or during CMOS fabrication. Examples of interleaved MEMS and IC processing platforms include M^3EMS, Mod-MEMS and various SOI-based integration concepts.

The M^3EMS technology platform[76], developed by Sandia National Laboratories, California, Albuquerque, NM, USA, utilizes shallow trenches in which MEMS structures are fabricated through a series of silicon oxide and poly-silicon deposition steps. A subsequent CMP process is applied to planarize the wafer and expose the monocrystalline silicon surface for IC fabrication. A post-CMOS HF etching step is necessary to release the MEMS structures and to complete device fabrication. In Figure 8, a schematic cross-section of a fully fabricated device is presented.

The Mod-MEMS integration process, developed by Analog Devices Inc., Norwood, MA, USA[77,78] in collaboration with UC Berkeley, uses a different technique to achieve the planarity necessary for CMOS fabrication. As illustrated in Figure 9a, the MEMS structures are manufactured on top of a flat silicon wafer via the deposition and surface micromachining of silicon nitride, silicon oxide and poly-silicon. Monocrystalline silicon is epitaxially grown on the area beside the MEMS structures to level out the surface topography. Finally, the surface is polished via CMP and prepared for subsequent CMOS processing. The fabrication is completed with an HF-based release etch.

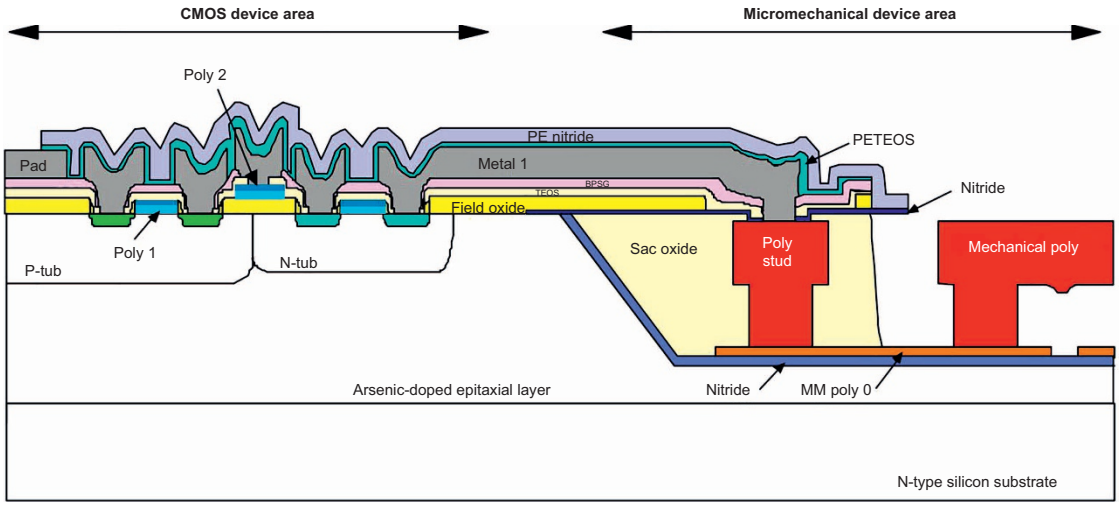

Figure 8 Multilevel MEMS formed within a shallow trench using the Sandia National Laboratories M^3EMS platform. From Ref 76.

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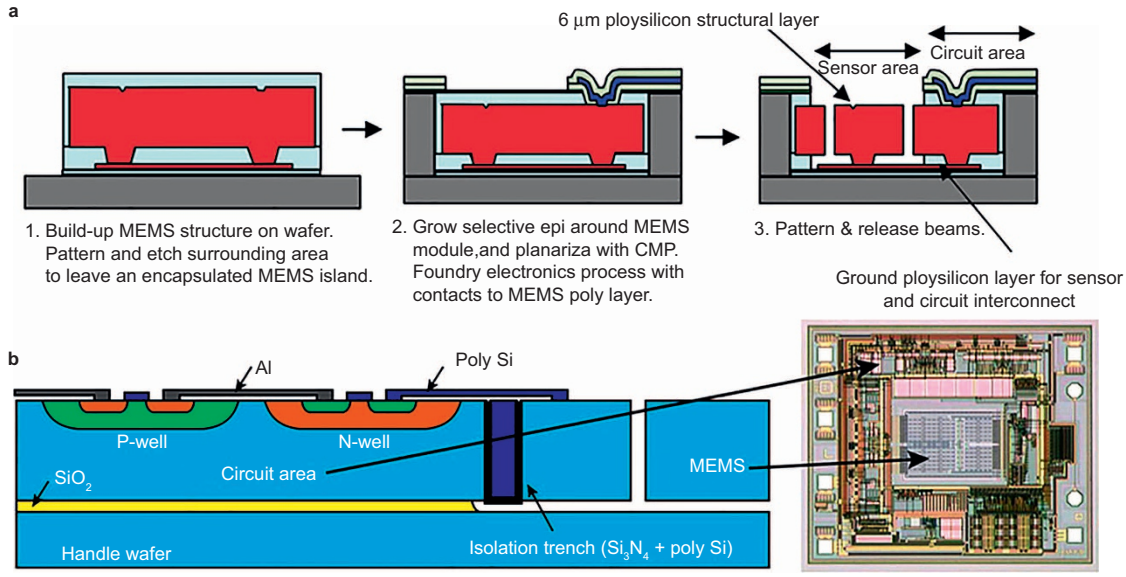

Figure 9 (**a**) Process outline for the Mod-MEMS platform. From Ref 77. (**b**) Schematic cross section and photograph of an SOI-MEMS device, showing the released MEMS structure fabricated from an SOI wafer, the isolation trench, and the IC area. Adapted from Ref 6 and Ref 80.

A related SOI-based integration technology that was also developed by Analog Devices Inc., Norwood, MA, USA[79] in collaboration with UC Berkeley[80–82] is depicted in Figure 9b. This integration platform involves separating the MEMS area from the CMOS area by creating isolation trenches in the silicon device layer of an SOI wafer. After a CMP step, the CMOS is fabricated in the device layer, followed by the definition of the MEMS structure and its release etching.

The CNM Institute of Microelectronics in Barcelona, Spain, has also developed an SOI-based integration platform in which the MEMS structures are fabricated in the device layer, whereas the CMOS circuits are fabricated in the bulk silicon[83]. This optical iMEMS technology platform[84] was developed for the integration of high-quality micro-mirrors with a BiCMOS process. Instead of using standard SOI wafers, the iMEMS process is based on a three-layer silicon stack that is formed through wafer bonding. A similar technology platform has also been developed at MIT[85]. MEMS interleaved processing can also be achieved by introducing additional, custom processing steps into the regular CMOS processing sequence[86]. This approach has found commercial application in the fabrication of pressure sensors by Infineon Technologies AG, Neubiberg, Germany[87] and inertial sensors by Analog Devices Inc., Norwood, MA, USA[88,89]. The University of Michigan has introduced a method based on a p^{++} etch-stop technique. Here, an additional implantation step in the CMOS process defines highly doped regions, and the MEMS structures are subsequently created via the bulk machining of the substrate. A large variety of applications using this technique have been demonstrated, ranging from pressure sensors and infrared sensors to neural probes[90–95].

In summary, monolithic MEMS and IC integration using interleaved MEMS and IC processing offers the possibility of integrating high-performance MEMS materials and devices together with CMOS circuits on the same substrate. In most approaches, the MEMS and CMOS structures are placed side-by-side on the substrate, which limits the achievable integration density to some extent. MEMS interleaved approaches require full access to a dedicated custom CMOS production line, which considerably limits the general utility of the technology, as this requirement is typically not compatible with fabless business models.

3.1.3 Monolithic MEMS and IC integration using MEMS-last processing via the bulk micromachining of the IC substrate

Monolithic MEMS and IC integration using MEMS-last processing by means of bulk micromachining is achieved through integration schemes in which the MEMS structures are manufactured after the entire CMOS fabrication process has been completed. This includes all approaches in which the MEMS components are fabricated in the CMOS substrate and/or in the CMOS thin-film layers; approaches that include subsequent layer deposition are presented in Section 3.1.4. MEMS-last integration via the bulk micromachining of the IC substrate has been under investigation since the late 1970s. Early efforts consisted of backside micromachining to realize piezoresistive pressure sensors[96,97]. Since that time, a variety of different fabrication approaches have been developed, as shown in Figure 10.

Backside etching with timed etch-stop control, as illustrated in Figure 10b, has been commercialized by Freescale for pressure sensor applications[99]. An alternative to timed etch-stop control is the electrochemical etch-stop technique depicted in Figure 10c, which allows for very precise etch stops between p-doped and n^{+}-doped regions[100,101]. Various MEMS structures, such as membranes, cantilevers and suspended islands, can be fabricated using this technique. Another approach is to directly structure the front side of the substrate. The technology platform shown in Figure 10d was developed at Carnegie Mellon University and uses the back-end interconnect metal layers as a hard mask for the patterning of the MEMS structures[102]. This method has found application in the fabrication of a variety of devices, ranging from accelerometers[103] and gyroscopes[104] to infrared imagers[105] and variable capacitors[106]. A similar fabrication approach, which uses photoresist masks for MEMS structuring, is depicted in Figure 10e. This method has been applied for the fabrication of passive, free-etched inductors for RF circuits[107] and, more recently, for microbolometers[108] as well as single-chip scanning microwave microscope and atomic force microscope (AFM) systems[109]. The method presented in Figure 10f is based on the deep-reactive ion etching (DRIE) of both the front and back sides of the substrate. This enables the fabrication of integrated monocrystalline silicon MEMS structures with superior mechanical properties[110]. The fabrication of infrared bolometer arrays using an

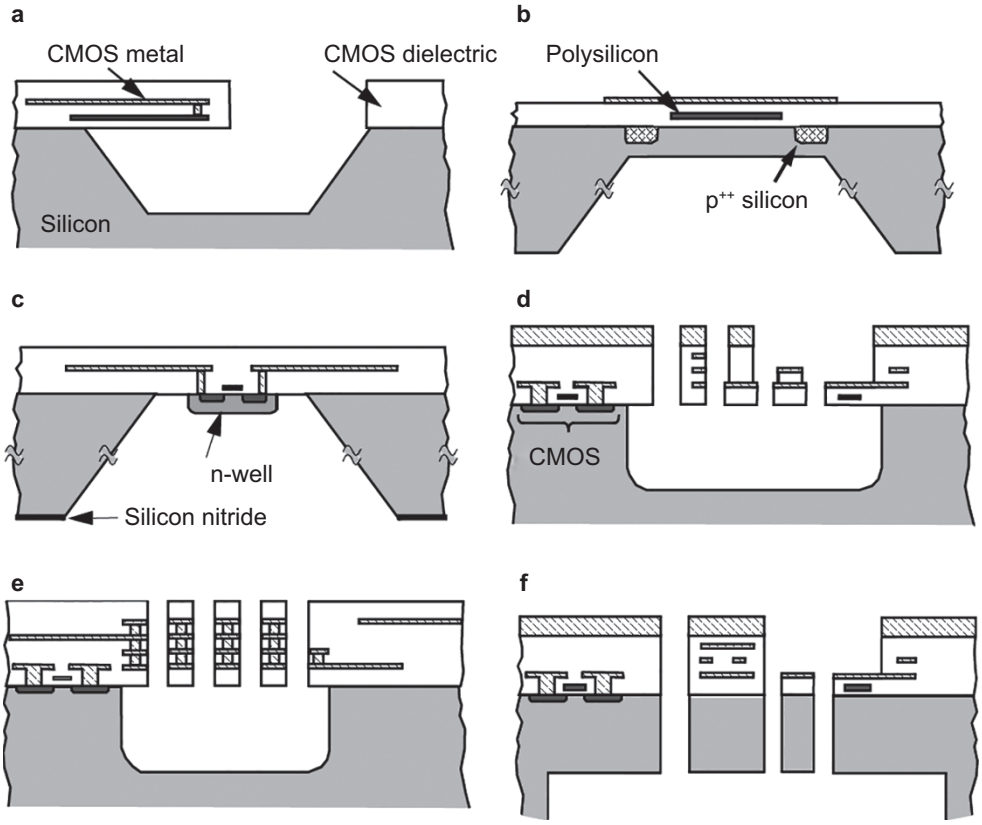

Figure 10 Various approaches to monolithic MEMS and IC integration using MEMS-last processing via the bulk micromachining of the IC substrate: (**a**) Front-side wet etching. (**b**) Backside wet etching. (**c**) Backside wet etching using an electrochemical etch stop. (**d**) Front-side dry etching using a metal hard CMOS mask. (**e**) Front-side dry etching using a photoresist mask. (**f**) Front-and backside anisotropic deep-reactive ion etching (DRIE) of a CMOS wafer. Adapted from Ref 98.

electrochemical etch stop has been developed at the Middle East Technical University, Ankara, Turkey[111], and is being commercialized by MikroSens, Ankara, Turkey[112]. In this process, n-well micro-bolometers are created via a standard CMOS process and connected by dielectric support arms, with the metal interconnect layer providing the electrical connections. A front-side electrochemical etch-stop technique is used to free etch the bolometer pixels without etching away the n-wells.

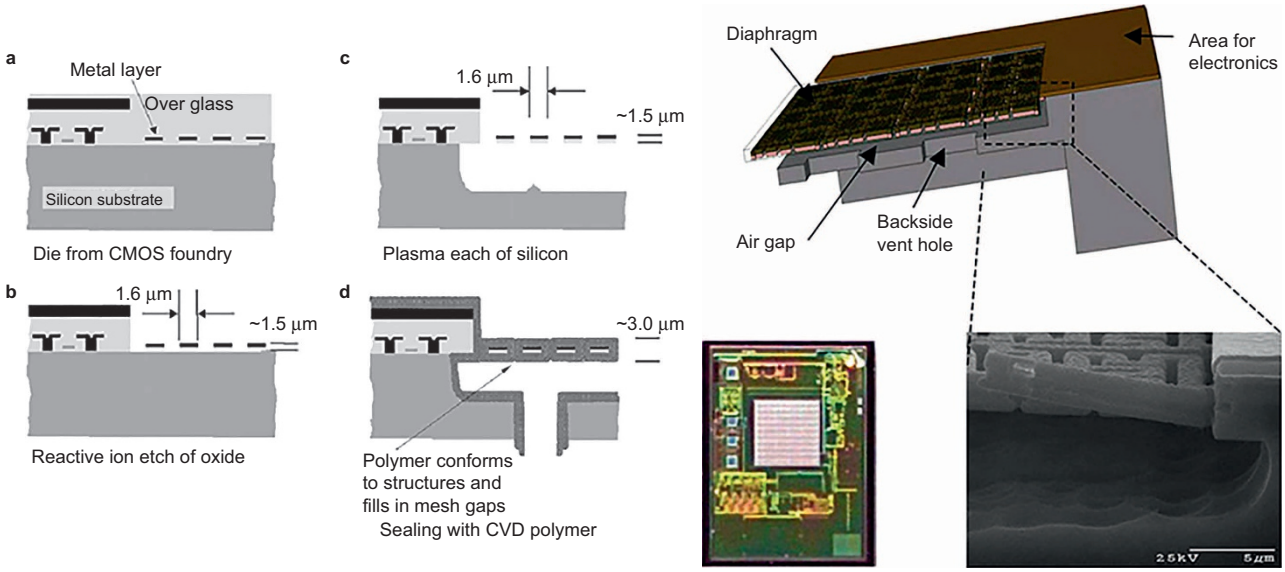

Figure 11 Fabrication process and images of an IC-integrated MEMS microphone. Adapted from Ref 6 and Ref 113.

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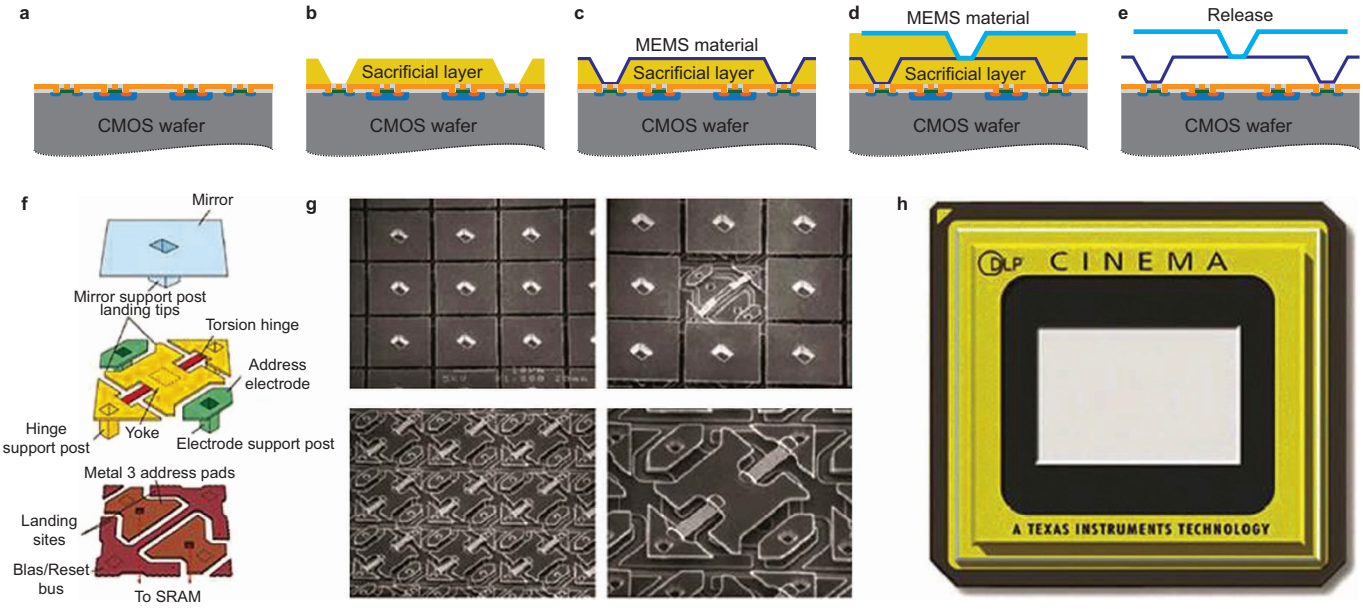

Figure 12 Typical processing scheme for monolithic MEMS-on-IC integration using MEMS-last processing via the deposition and surface micromachining of two layers: (**a**) Manufacturing of the CMOS wafer. (**b**) Deposition and patterning of the sacrificial layer. (**c–d**) Deposition and patterning of the first layer of MEMS material, the second sacrificial layer and the second layer of MEMS material. (**e**) Etching of the sacrificial layer. (**f**) Schematic diagram of a deflected torsional micro-mirror pixel. (**g**) SEM images of micro-mirror pixels with the mirror plate of the center pixel removed to expose the underlying hinge structures. (**h**) Packaged DLP™ chip containing an array of more than two million micro-mirrors, placed in a ceramic package with a glass window[6].

An integration process for MEMS microphones based on a combination of DRIE backside etching and the use of the interconnect metal as a hard mask for front-side etching was developed at Carnegie Mellon University and later commercialized by Akustica, Inc. (now Bosch)[113]. The process utilizes a serpentine mesh pattern in a metal interconnect layer to form a suspended membrane that is sealed by a CVD-deposited polymer. Figure 11 shows a schematic illustration of the fabrication process for the microphone membrane as well as images of a fabricated device.

A variety of different MEMS-last integration approaches based on bulk micromachining have been applied in the fabrication of monolithic inkjet printheads with integrated CMOS circuits[114–116]. Inkjet printheads represent the largest-volume commercial application of monolithic MEMS and CMOS integration in the industry to date.

In summary, monolithic MEMS and IC integration using MEMS-last processing by means of bulk micromachining has the important advantage that it can be implemented using existing IC infrastructure, including access to design tools and IC foundries. The MEMS components are formed in the completed IC wafers using fairly simple and cost-effective processing steps. This approach offers the potential for short development cycles (i.e., short times to market) and the use of extremely low-cost components. The disadvantages of this approach are the limited design freedom for the MEMS devices and the limited selection of materials for the MEMS devices allowed by the CMOS process. The etching processes, such as the passivation step, must be carefully designed not to attack any CMOS structures. In addition, in standard CMOS production lines, the mechanical properties of the materials and layers are typically not very well characterized or controlled. This can result in reliability and repeatability problems in the fabricated MEMS devices.

3.1.4 Monolithic MEMS and IC integration using MEMS-last processing via layer deposition and surface micromachining

In monolithic MEMS and IC integration using MEMS-last processing via layer deposition and surface micromachining, the MEMS structures are fabricated by depositing and micromachining materials on top of completed CMOS wafers. Figure 12 illustrates a characteristic processing scheme for the integration of two-layer MEMS structures on top of a CMOS substrate. First, a sacrificial layer is deposited and patterned on the CMOS substrate, as shown in Figure 12a and b. Then, the MEMS material is deposited and patterned, as shown in Figure 12c. Figure 12d illustrates a second cycle of sacrificial material deposition and patterning followed by MEMS material deposition and patterning to create the second layer of the MEMS structure. Finally, the sacrificial material is removed in a release etching step to yield a suspended MEMS device on top of the CMOS substrate, as depicted in Figure 12e. This approach allows for the realization of rather complex MEMS structures on top of IC substrates[6,117]. In this processing scheme, it is important that the procedures for the deposition of the sacrificial and MEMS materials are compatible with the CMOS substrate. The maximum temperature to which a typical CMOS substrate can be exposed without causing permanent damage to the circuits is approximately 400–450 °C[6]. Some of the most commonly used sacrificial materials are various types of polymers that can be easily deposited and then removed using oxygen plasma dry-etching processes with very high etching selectivity towards the typical materials that are used for MEMS and CMOS structures[6,117,118]. Metals[6], dielectrics[119] and poly-crystalline and amorphous semiconductors[6,120] have also been used as sacrificial layers. The functional MEMS materials that have been deposited on CMOS substrates include various metals[6,118,119,121], silicon nitride, silicon dioxide[6,122], piezoelectric aluminium nitride[6], zinc-oxide[6], poly-crystalline silicon germanium[120,123,124], amorphous

silicon[117,122], vanadium oxide[122,125], structural polymers[6,126] and various combinations of the above materials.

The vast majority of commercially available micro-mirror arrays[118] and uncooled infrared bolometer focal plane arrays[122] are implemented as SoC solutions based on monolithic MEMS and IC integration using MEMS-last processing via layer deposition and surface micromachining. One example are the digital micro-mirror arrays from Texas Instruments that are depicted in Figure 12f–h[6,118].

The application of monolithic MEMS and IC integration using MEMS-last processing via layer deposition and surface micromachining has been proposed for a large number of MEMS devices, including infrared bolometer arrays consisting of VO_x[125], amorphous silicon[117] or metal[121], micro-mirror arrays consisting of poly-crystalline silicon germanium[123] or metal[119], inertial sensors consisting of poly-crystalline silicon germanium[124], biochips consisting of structural polymers[127], bulk acoustic wave resonators consisting of poly-crystalline silicon germanium[128], and many other MEMS devices based on a variety of materials[6].

In summary, the most important advantage of monolithic MEMS and IC integration using MEMS-last processing via layer deposition and surface micromachining is that in this approach, standard CMOS foundries can be utilized to fabricate the CMOS wafers. The MEMS structures are integrated on top of completed CMOS wafers, utilizing, e.g., a specialized MEMS fab. The complexity of the process flow is relatively low, and the same chip area can be simultaneously occupied by both MEMS and CMOS structures. Thus, the available area on the chip is used very efficiently, and the achievable integration densities can be extremely high. The primary disadvantage of this approach is that the deposition temperature for the MEMS materials must lie within the allowed temperature budget for the CMOS wafer, which is typically below 400 or 450 °C. This excludes the use of important high-performance MEMS materials such as monocrystalline and poly-crystalline silicon and makes the technology less attractive for MEMS devices that must be implemented using high-performance MEMS materials, such as inertial sensors and resonators. Such devices typically benefit from the outstanding material properties provided by monocrystalline silicon, including low internal stresses, perfect elastic behaviour and a high quality factor (Q).

3.2 SoC solutions using heterogeneous MEMS and IC integration

Heterogeneous MEMS and IC integration is defined here as the joining of two or more substrates that contain fully or partially fabricated MEMS and IC structures to produce a heterogeneous SoC solution. Heterogeneous MEMS and IC integration can be categorized as either (1) heterogeneous MEMS and IC integration with via formation during layer transfer (e.g., wafer bonding), also referred to as via-first processes, or (2) heterogeneous MEMS and IC integration with via formation after layer transfer (e.g., wafer bonding), also referred to as via-last processes.

3.2.1 Heterogeneous MEMS and IC integration with via formation during layer transfer

An example of a typical heterogeneous MEMS and IC integration process in which the vias that establish the mechanical and electrical contacts between components on the two substrates are formed during the layer transfer process (i.e., wafer bonding) is shown in Figure 13a. This specific integration process is used for the manufacturing of very high-volume multi-axis gyroscope products distributed by InvenSense in the USA (manufactured by TSMC in Taiwan)[9,11,129]. In this process, the monocrystalline silicon MEMS sensors (e.g., gyroscopes), including the cap for the MEMS package, are prepared on an initial wafer that is subsequently bonded to a pre-fabricated CMOS-based IC wafer that contains etched cavities, as indicated in Figure 13a–c. In this example, aluminium/germanium eutectic bonding is used to bond and seal

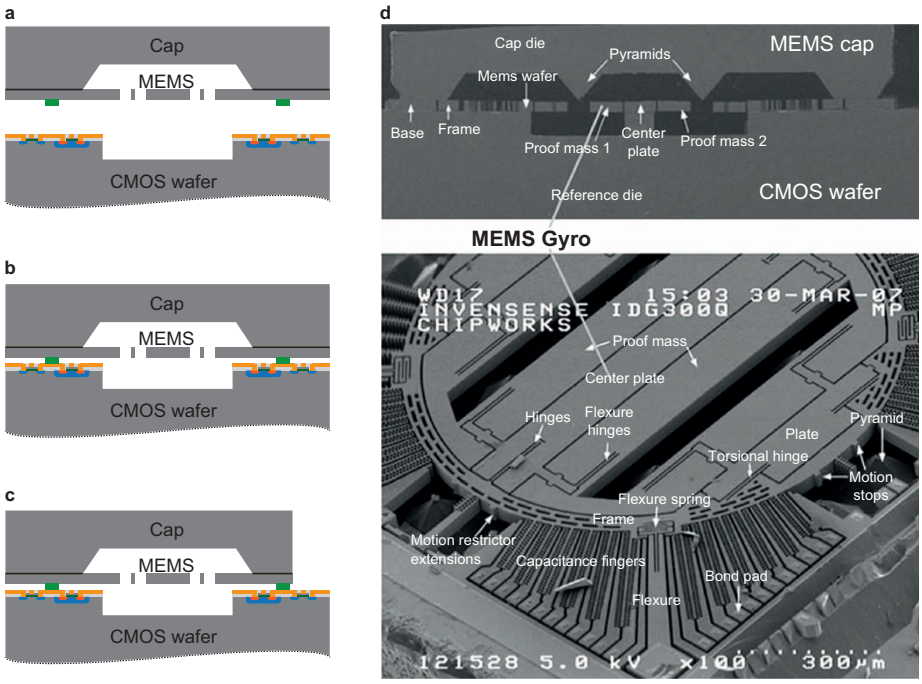

Figure 13 Via-first heterogeneous integration platform from InvenSense Inc., San Jose, CA, USA, which is used for, e.g. the high-volume manufacturing of gyroscope products: (**a**) A pre-fabricated monocrystalline silicon MEMS sensor, including a cap, is (**b**) bonded to a pre-fabricated CMOS-based IC wafer containing etched cavities; then, (**c**) the contact pads on the CMOS wafer are revealed. (**d**) SEM images of a gyroscope integrated with CMOS circuits. From Ref 9.

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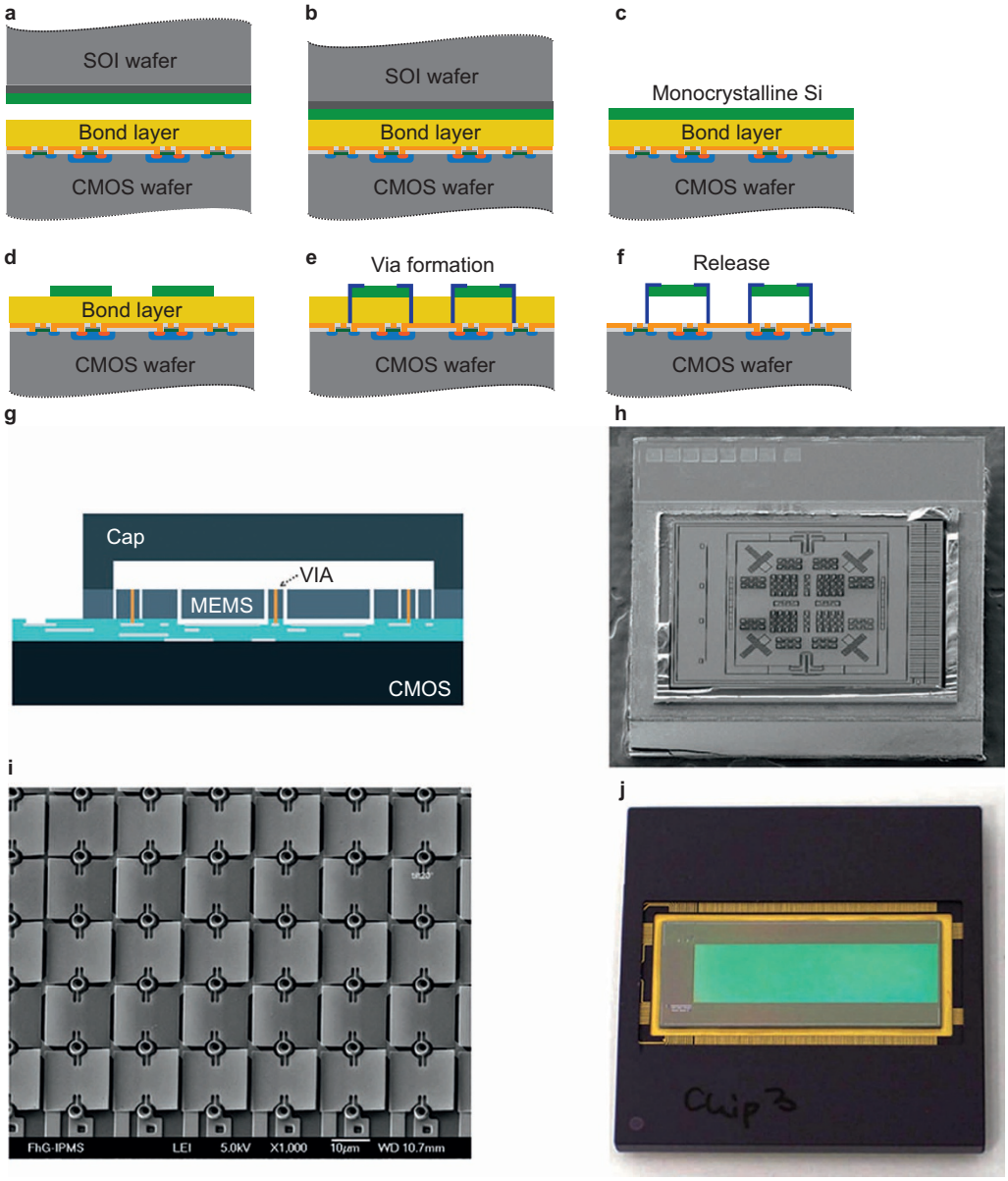

Figure 14 Example of heterogeneous MEMS and IC integration with via formation after bonding: (**a**) Individual fabrication of the IC wafer and the handle wafer, which contains a monocrystalline silicon MEMS device layer (e.g., an SOI wafer). (**b**) Wafer bonding using an intermediate adhesive layer. (**c**) Sacrificial dissolution or release of the handle wafer. (**d**) Patterning of the monocrystalline silicon. (**e**) Via-hole etching and via formation. (**f**) Sacrificial etching of the intermediate adhesive layer. (**g**) Design based on via-last heterogeneous MEMS and IC integration for accelerometers distributed by mCube in the USA (manufactured by TSMC Ltd.) and (**h**) SEM image of an mCube accelerometer. From Ref 142. SEM images of (**i**) a 1-megapixel monocrystalline silicon mirror array on CMOS driving electronics and (**j**) a packaged micro-mirror array. From Ref 143.

the combined gyro and cap wafer against the aluminium metal layer on the CMOS wafer[130]. Figure 13d shows SEM images of a gyroscope that was manufactured using this technology[9].

One of the first reported examples of heterogeneous MEMS and IC integration with via formation during wafer bonding was a monocrystalline silicon mirror array consisting of 32 × 32 mirrors with individual mirror dimensions of 1 mm × 1 mm[131,132]. Another well-developed heterogeneous MEMS and IC integration platform has been used to manufacture large arrays of IC-integrated AFM tips[133] and RF switches[134,135]. In this process, a glass wafer with pre-fabricated monocrystalline silicon AFM tips is aligned with and bonded to a CMOS-based IC wafer using a combination of solder-bump bonding and polyimide adhesive bonding. Next, the transferred AFM tips are released from the glass wafer via laser debonding. The vias of the AFM tips are 15 µm in diameter, the AFM tip array has a pitch of 130 µm × 100 µm, and the monocrystalline silicon AFM cantilevers are 300 nm thick. Other variations of heterogeneous MEMS and IC integration with via formation during device transfer have been proposed[22,25], including the integration of carbon-based NEMS materials[136–138], material integration using self-assembly processes[139], and transfer printing techniques for MEMS[140].

In summary, a key advantage of heterogeneous MEMS and IC integration with via formation during layer transfer is that it allows high-performance MEMS materials such as monocrystalline silicon to be combined with standard CMOS-based IC wafers. The

MEMS components can be pre-fabricated prior to integration with the IC wafer, and the integration and packaging can be performed in a single bonding step, as illustrated in Figure 13. In addition, some of these technologies are supported by the existing foundry infrastructure, thus greatly facilitating fabless business models. The disadvantages of via-first processes are that they often require aligned substrate-to-substrate bonding, which adds process complexity and results in limitations on the achievable post-bonding alignment accuracies[141]. Additionally, reliable electrical interconnections of bonded vias with dimensions of less than 10 μm are challenging to implement.

3.2.2 Heterogeneous MEMS and IC integration with via formation after layer transfer

Heterogeneous integration with via formation after layer transfer (i.e., wafer bonding) is schematically illustrated in Figure 14. In this approach, the vias that establish the mechanical and electrical contacts between components on the different substrates are defined after the layer transfer is performed, as depicted in Figure 14e. In this specific example, the MEMS handle substrate is sacrificially dissolved or released from the MEMS structures prior to via formation[9].

A heterogeneous MEMS and IC integration process with via formation after wafer bonding has been developed by TSMC, Ltd. in Taiwan and is offered as a MEMS foundry platform[11,144]. This process involves bonding a completed CMOS wafer onto a silicon MEMS wafer using an intermediate SiO_2 adhesive layer and subsequently forming vias to electrically interconnect the MEMS devices to the CMOS circuits. This process is utilized for, e.g., the high-volume manufacturing of multi-axis accelerometers by mCube Inc., San Jose, CA, USA [see Figure 14g–h][145].

Different heterogeneous MEMS and IC integration processes with via formation after layer transfer have also been proposed for the realization of infrared bolometer arrays[122,146–152], arrays of tilting and piston-type micro-mirrors[143,153–156], nanoelectromechanical switches for logic circuits[157], micro-Pirani vacuum gauges[158] and RF MEMS devices[159–163]. In most of these integration platforms, an intermediate polymer adhesive layer is used in the wafer bonding process. The advantages of adhesive bonding using an intermediate polymer layer are the high process yield that can thus be achieved and the fact that no demanding surface pre-treatment or surface planarization steps are required for the bonding[164–166]. The first reported MEMS device to be integrated on top of functional CMOS circuits using via-last heterogeneous 3D integration was a 1-megapixel monocrystalline silicon micro-mirror array, depicted in Figure 14i–j[143]. This mirror array has a pixel pitch of 16 μm × 16 μm and contains silicon mirror membranes that are 340 nm thick and are located at an extremely well-defined distance of 700 nm from the corresponding electrodes on the underlying CMOS circuits. The mirror vias have a diameter of 2 μm, and the torsional mirror hinges are 600 nm wide. Heterogeneous MEMS and IC integration with via formation after layer transfer has also been proposed for the integration of carbon-based NEMS materials[167], self-assembly processes[139] and transfer printing techniques[140].

In summary, the key advantage of heterogeneous MEMS and IC integration processes with via formation after layer transfer is the fact that they allow high-performance MEMS materials such as monocrystalline silicon to be combined with standard CMOS-based IC wafers. Therefore, wafer-to-wafer alignment during bonding is not necessarily required, and as a consequence, the achievable placement accuracy of the MEMS components on the IC wafer is defined by the placement accuracy that can be achieved using the lithography tools, which can easily be in the nm-range. The feasible via dimensions can be in the sub-μm-range, and the distance between the MEMS device membranes and the IC substrate surface can be accurately defined by the thickness of the intermediate bonding layer over a large interval of below 100 nm to several tens of μm. Thus, via-last heterogeneous MEMS and IC integration platforms can be employed for the fabrication of IC-integrated MEMS with extremely small dimensions and extremely high integration densities. A disadvantage of this approach is the greater number of processing steps as compared to typical via-first heterogeneous MEMS and IC integration processes.

4 OUTLOOK AND CONCLUSIONS

A wide variety of alternative solutions for combining and integrating MEMS and ICs are available. These methods can be divided into hybrid multi-chip solutions and SoC solutions, both of which have distinct advantages and disadvantages. In general, multi-chip solutions are more flexible and less complex, allow for rapid product development cycles and are cost-effective for all combinations of MEMS and IC chip sizes. However, compared with SoC solutions, multi-chip solutions offer relatively low integration densities, are larger in size and footprint and suffer from lower EMC robustness and high parasitic capacitances in the electrical connections between the MEMS and IC components. SoC solutions, on the other hand, have the disadvantages of higher complexity, lower flexibility and longer development times. For certain classes of MEMS products, such as large arrays of transducers, the high integration density that can be achieved in SoC solutions is a necessary prerequisite for the implementation of these products. High integration densities also endow MEMS products with small system dimensions, including a small footprint and low thickness.

If the fabrication yield of either the IC or the MEMS process is low, then SoC solutions are strongly affected by the aggregated combined yield, whereas in the multi-chip approach, known good dies can be paired to achieve a better overall yield. Another cost-driving factor for SoC solutions arises if the MEMS and IC chips are significantly different in size. This leads to unused wafer area, which, in many cases, is not economically viable.

The potentially lower yield of SoC solutions is offset by their lower costs for testing and packaging. SoC solutions offer the possibility of packaging at the wafer level, which reduces the number of packaging and wire bonding steps that must be performed at the chip level. Testing is also often a significant contribution to the overall system cost. For SoC solutions, this cost can be greatly reduced because only one test on the final assembled device is needed, compared with the several tests of individual modules prior to assembly as well as tests after assembly that are required in the case of multi-chip solutions.

The development of cost-effective through-substrate vias of increasingly smaller pitch and thinner chips has had a profound impact on MEMS and IC integration based on hybrid multi-chip solutions. The 3D stacking of IC and MEMS chips with small through-substrate vias enables the fabrication of relatively thin devices with small footprints and electrical interconnects with small parasitic capacitances, while still maintaining the advantages of hybrid multi-chip solutions. Extensive research efforts by the semiconductor industry in the areas of 3D IC integration and through-substrate vias will facilitate the widespread adoption of these solutions for integrating MEMS and ICs, as well.

Heterogeneous MEMS and IC integration approaches for SoC solutions enable the integration of high-performance MEMS materials and devices on top of standard foundry CMOS wafers. Thus, no compromise must be made in the selection of MEMS materials, and the most suitable CMOS technology can be chosen. The same chip area can be simultaneously occupied by both MEMS and CMOS structures. These advantages, together with the development of stable and CMOS-compatible wafer-level packaging solutions, enable flexible and cost-effective SoC

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solutions. Several products that are based on heterogeneous MEMS and IC integration approaches have already gained significant market shares on the extremely competitive high-volume consumer market[9,11,12]. Some of the factors contributing to this success are the compatibility of such approaches with fabless and fab-light business models, their ability to utilize standard CMOS-based ICs from various foundry sources and the potential they offer to dramatically shrink the overall MEMS device dimensions, thereby enabling the combination of multiple sensors on a single, highly integrated chip.

In summary, future developments in multi-chip and SoC solutions are converging towards higher MEMS and IC integration densities and, thus, smaller and cheaper components. A clear trend that is evident in MEMS sensor components is the integration of several sensing functions (e.g., multi-axis inertial and magnetic field sensing) in a single module, together with specialized processing functions for the sensor signals. These pre-processed and robust (often digital) sensor signals can be interfaced with high-performance processing units for advanced signal processing and the fusion of signals from various sensor elements.

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COMPETING INTERESTS

The authors declare no conflict of interest.

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