Short-Channel Transistors Constructed with Solution-Processed Carbon Nanotubes

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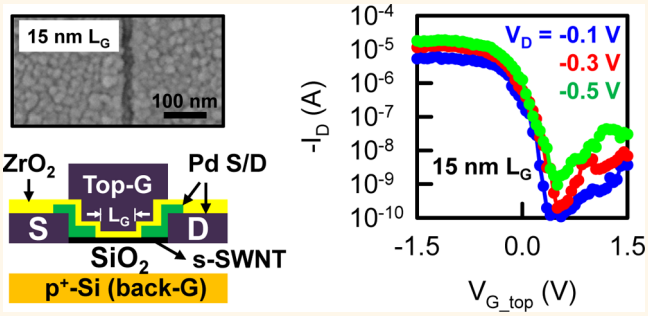
ABSTRACT We develop short-channel transistors using solution-processed single-walled carbon nanotubes (SWNTs) to evaluate the feasibility of those SWNTs for high-performance applications. Our results show that even though the intrinsic field-effect mobility is lower than the mobility of CVD nanotubes, the electrical contact between the nanotube and metal electrodes is not significantly affected. It is this contact resistance which often limits the performance of ultrascaled transistors. Moreover, we found that the contact resistance is lowered by the introduction of oxygen treatment. Therefore, high-performance solution-processed nanotube transistors with a 15 nm channel length were obtained by combining a top-gate structure and gate insulators made of a high-dielectric-constant ZrO_2 film. The combination of these elements yields a performance comparable to that obtained with CVD nanotube transistors, which indicates the potential for using solution-processed SWNTs for future aggressively scaled transistor technology.



KEYWORDS: carbon nanotubes · short channel · transistor · ballistic · solution-processed carbon nanotubes · contact resistance · quantum limit

The exceptional electronic properties of single-walled carbon nanotubes (SWNTs) make them promising building blocks for future nanoelectronic devices primarily because they perfectly combine the following traits: one-dimensional transport, small size, extremely high carrier mobility, large current density, small intrinsic gate delay, and high intrinsic cutoff frequency.[1] Clean and defect-free SWNTs are desirable for fabricating high-quality devices. Therefore, the high-temperature growth of SWNTs directly onto a substrate *via* chemical vapor deposition (CVD) has become the most widely used technique for achieving high-quality SWNT devices.[2−5] Devices formed *via* the CVD method possess excellent field-effect transistor (FET) properties with typical mobilities ranging from 1000 to 10 000 $cm^2/(V\cdot s)$, depending upon the diameter of the nanotubes,[6] and conductances approaching the ballistic limit ($G = 4e^2/h \approx 155\ \mu S$).[3,7] However, the CVD process yields a mixture of metallic (m-SWNTs) and semiconducting (s-SWNTs) nanotubes, and m-SWNTs are an unacceptable contamination for digital electronics applications. Moreover, an effective method for selectively removing m-SWNTs after their growth without affecting neighboring s-SWNTs has not yet been established on a large scale.[8]

Solution-processed SWNTs offer an attractive alternative to separating SWNTs according to their electronic type in solution using techniques such as density gradient ultracentrifugation,[9,10] selective polymer wrapping,[11] and chromatography.[12,13] However, solution-processing techniques can introduce defects that degrade the intrinsic electrical properties of the SWNTs with a reported average effective mobility for s-SWNTs ranging from 20 to 300 $cm^2/(V\cdot s)$,[14−20] which could limit their application in future nanoelectronic devices. Nevertheless, for short-channel nanotube transistors operating in the quasi-ballistic regime, in which electron transport is primarily limited by the contacts, transistors made from

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solution-processed s-SWNTs can be expected to provide high performance if the quality of the metal contact with these nanotubes is comparable to that of the CVD nanotubes.[20] In the current work, we report the integration of 15 nm gate length (L_G) short-channel solution-processed SWNT transistors into a top-gate structure with a high-κ (ZrO_2) gate dielectric layer. The objective of this work is to assess the feasibility of using solution-processed nanotubes in scaled FETs. The results confirm that the performance of the scaled solution-processed nanotube devices approaches the best p-type devices containing CVD nanotube channels.

RESULTS AND DISCUSSION

The devices used in this work were composed of a purified, commercially available 90% semiconducting SWNT solution (0.01 mg/mL, average diameter ranging from 1.2 to 1.7 nm, determined by the commercial provider, Nano Integris Inc.) bridging metal source (S) and drain (D) electrodes on a SiO_2 (55 nm)/p^+-Si substrate. We employed the spin alignment technique to partially align the nanotubes on the substrate.[15] The hydrodynamic flow, which has been shown to efficiently align nanoparticles on a drying surface,[21] appears to be markedly enhanced by the spinning wafer and effectively aligns the nanotubes as the solvent evaporates and thins.[22] The degree of alignment and number of nanotubes can be tuned based on the spin-assembly conditions, such as spin speed and solution volume.[15,23] We first fixed the nanotube deposition conditions at a spin speed of 7000 rpm and varied a nanotube solution volume of 4 μL to obtain a large number of devices with single nanotube channels. For multiple nanotube channels, we simply increased the volume of nanotube solution up to 6 μL.

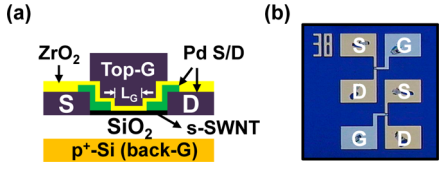

Figure 1. (a) Device schematic for the top-gate solution-processed SWNT transistor. (b) Optical image of such devices fabricated on the chip.

After depositing the solution-processed nanotubes, a two-step source/drain (S/D) metallization (optical and e-beam lithography) of Pd was used to form the bottom-gate transistors. The bottom-gate transistors (Si as the back gate) were first characterized via electrical transport measurements before being subjected to atomic-layer deposition (ALD) of a ZrO_2 film ($\kappa \approx 12$) for a single nanotube channel transistor using a tetrakis (ethylmethylamido) zirconium precursor and water at 130 °C.[24] After that, Pd gate electrodes were patterned for the top-gate structures.

A schematic of the device structure is shown in Figure 1a. Note that our top-gate device differs from self-aligned nanotube transistors[25] in that this device has ungated regions on two sides of the S/D electrodes. However, these ungated regions cannot significantly affect the carrier transport because top-gate can still modulate these areas through the strong fringing field. The minimum L_G value in this study is 15 nm. Figure 1b shows an optical microscope image of the fabricated top-gate transistors.

When packing numerous SWNTs into a device, the predicted on-current (I_{ON}) is often hampered by charge screening.[26] Such screening is part of the reason why transistors from solution-processed nanotubes exhibited lower-than-anticipated on-currents.[14] However, the modest SWNT densities from the spin-aligned deposition used in this work provide an excellent platform for observing direct on-current scaling. Representative transfer characteristics for a bottom-gate FET with $V_D = -0.5$ V are shown in Figure 2a. This device has an L_G of 270 nm (in a bottom-gate device, an L_G is defined by the distance between S/D electrodes) with only a single nanotube (confirmed by AFM tapping mode) with an I_{ON}/I_{OFF} ratio in excess of 10^6. Approximately 50% of the devices contained a single nanotube channel when the spin speed was 7000 rpm and the volume of the nanotube solution was 4 μL (Figure 2b). Figure 2c shows a plot of the I_{ON} *versus* the number of s-SWNTs from different devices. Note that some of the nanotubes for the multichannel device are m-SWNTs and such devices were excluded in this plot. The trend is linear, which represents direct on-scaling similar to previous reports for CVD nanotubes.[27] The deviation of

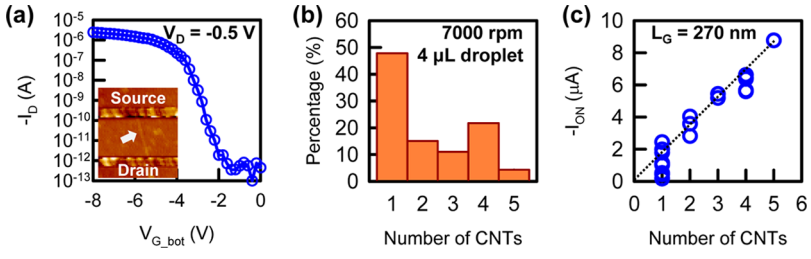

Figure 2. The electrical properties of the bottom-gate solution-processed SWNT transistors with L_G = 270 nm. (a) Transfer characteristics at $V_D = -0.5$ V. (Inset) AFM image of the device. (b) Probability for the number of SWNTs bridging the S/D electrodes at 7000 rpm with a volume of 4 μL of the nanotube solution. (c) I_{ON} *versus* the number of SWNTs from a set of bottom-gate devices under the same bias conditions ($V_G = -8$ V and $V_D = -0.5$ V).

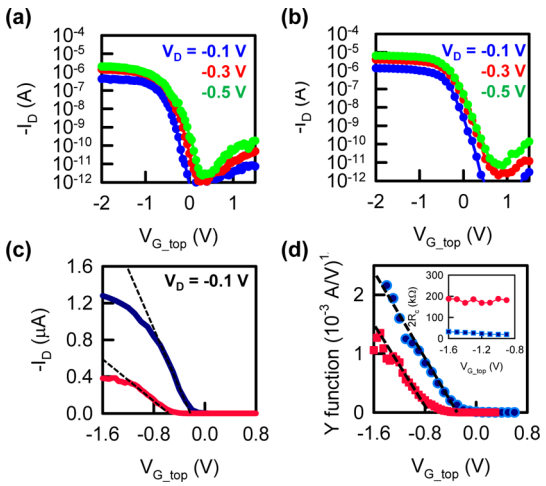

Figure 3. Transfer characteristics for the top-gate device with a single SWNT channel with L_G = 240 nm at different V_D for the as-made device (a) and the device after oxygen treatment (b). The 15 nm ZrO_2 film (EOT ≈ 4.9 nm) was used as a gate dielectric. (c) Linear transfer characteristics for the two devices shown in Figure 3 (red line, as-made device; blue line, device after oxygen treatment) at $V_D = -0.1$ V. The black dotted lines serve as a visual guide. (d) The calculated *Y*-function and $2R_C$ for the two devices made from solution-processed SWNTs with L_G = 240 nm, shown in frame c, as a function of V_G (red symbol, as-made device; blue symbol, device after oxygen treatment). The black dotted lines represent the linear fits.

the data points from this linear relationship is most likely due to the variation in the SWNT diameters, which results in different band gaps and, thus, Schottky-barrier heights. Ideally, further work should tighten the distribution of the nanotube diameters and further increase the s-SWNT density while maintaining even spacing to prevent charge screening.

Next, we conducted systematic electrical transport measurements of the top-gate solution-processed device. Figure 3a shows the representative transfer characteristics for an as-fabricated top-gate device in air at room temperature with no further passivation or annealing treatments. This top-gate device was further processed from the bottom-gate devices with a single nanotube channel. The back-gate bias was floated in all measurements of the top-gate devices. The different L_G values between Figure 2 (270 nm) and Figure 3 (240 nm) arose from the different definition of L_G between bottom- and top-gate structures. For 15 nm thick ZrO_2 gate dielectric layers, an L_G of a top-gate structure is defined by the gate electrode, that is, $L_G = 270 - (2 \times 15) = 240$ nm. Note that both the subthreshold swing and the transconductance drastically improved from the bottom-gate device because of the thinner high-κ gate dielectrics and top-gate structures. However, the current drivability was not significantly enhanced for the device as-made (Figure 3a). We did observe that the electrical performance of the top-gate device were substantially improved (Figure 3b) after oxygen exposure in the chamber at 230 mTorr for 50 min (we called this process "oxygen treatment"). The device after oxygen treatment exhibited a maximum transconductance ($g_m = dI_D/dV_G|_{V_D}$) ≈ 8.6 μS and $I_{ON} \approx -5.8$ μA (defined as $|V_G - V_T| = 1.0$ V and $V_D = -0.5$ V). The g_m and I_{ON} values were improved by 360% and 340%, respectively, after oxygen treatment. The subthreshold swing of the device was ~130 mV/decade, the I_{OFF} in $I_D - V_G$ was relatively bias-independent (for $V_D = -0.1$ V to -0.5 V), and the I_{ON}/I_{OFF} remained constant at ~10^5.

It is interesting to investigate the effect of oxygen treatment on our top-gate devices. The effect of oxygen on the electrical properties of the nanotube devices has been reported previously, and was attributed to an increase in the work-function of metal contacts with the adsorption of oxygen molecules[28] To evaluate the oxygen effect on our top-gate structure, we introduced the *Y*-function method to obtain contact resistance and mobility values with the assumption of ohmic contacts and drift-diffusion as dominant carrier transports in long channel devices.[20,29] The *Y*-function is defined as follows:

$$Y = \frac{I_D}{g_m^{1/2}} = \left(\frac{W}{L} C_{OX} \mu_{FE} V_D\right)^{1/2} (V_G - V_T)$$

$$= \left(\frac{1}{L^2} C_G \mu_{FE} V_D\right)^{1/2} (V_G - V_T) \quad (1)$$

where we extracted the mobility (μ_{FE}) from the slope of the *Y versus* V_G plot, with the intrinsic V_T coming from the *x*-axis intercept. From the known μ_{FE} and V_T, the contact resistance (R_c) of a specific device can be acquired from the following:

$$2R_C = \frac{V_G}{I_D} - R_{ch} = \frac{V_G}{I_D} - \frac{L_G^2}{\mu_{FE} C_G (V_G - V_T)} \quad (2)$$

Linear-scale transfer curves for two top-gate transistors, that is, with and without oxygen treatment, are shown in Figure 3c. These devices yield very different values for g_m, which results in differing slopes for the linear scale. However, the plot of the *Y*-function for these devices reveal that they have nearly identical μ_{FE} values, as indicated by their similar slopes (Figure 3d), which results in a similar extracted μ_{FE} of ~380 $cm^2/(V \cdot s)$. This value is lower than the previously reported average for CVD nanotubes, which is typically in the range of 1500−3000 $cm^2/(V \cdot s)$, extracted from individual nanotube devices with similar submicrometer L_G.[1,5,30,31] These results indicate that relative to CVD nanotubes, solution-processed SWNTs can possess some structural defects induced during the purification and suspension processes, which limit μ_{FE}. However, we observe that the R_c values of the oxygen-treated device were significantly lower than those of the as-made device. The inset of Figure 3d presents the calculated $2R_c$ as a function of the V_G according to eq 2. Note that the lowered contact

resistance values ($2R_c$ = 20 − 34 kΩ) were almost similar to those reported in previous studies of CVD nanotubes. Therefore, the solution-processed nanotubes are expected to perform similarly to CVD nanotubes in the final scaled FETs, in which electron transport is largely limited by the contacts rather than the channel scattering. We speculate that similar but slightly higher $2R_c$ values in this work as compared to those in the best-reported CVD nanotube devices[30,32] are possibly due to remaining surfactants on the nanotube surface.

The lower R_c after oxygen treatment can be explained as follows. It has been reported that exposure of the device to oxygen could increase the work-function of the metal surface.[28] An increased work-function modifies the barrier at the metal-semiconducting nanotube interface and allows for efficient carrier transport. Oxygen molecules can desorb from the nanotube contacts during our ALD process for the ZrO_2 gate dielectrics due to the high process temperature (130 °C) and ambient vacuum. Although the devices are capped with the ZrO_2 gate dielectric layers, these layers are permeable enough to allow oxygen molecules to escape from and penetrate into the nanotube contacts to some extent. However, exposure to oxygen molecules in air is insufficient to produce high-performance devices, as shown in Figure 3a. Furthermore, to improve the electrical properties, long-time exposure in air should be required, but it is inefficient. Therefore, a reproducible improvement in the transistor performance is obtained for our top-gate structures through our oxygen treatment. Therefore, we conclude that oxygen treatment can effectively improve the performance of the device by reducing the contact resistance associated with the S/D electrodes.

To observe the scaling behavior of the solution-processed nanotube devices, we first scaled the L_G to 15 nm for a single nanotube channel. In this case, reduced ZrO_2 film thickness of 10 nm was used for the gate dielectric (equivalent oxide thickness, EOT ≈ 3.2 nm). We also used oxygen treatment to enhance the electrical properties, such as g_m and I_{ON} values. Top-view SEM images of 15 and 45 nm L_G devices are shown in Figure 4a. Our representative miniaturized 15 nm L_G top-gate device with a single solution-processed SWNT exhibited a high peak transconductance of 32 μS per tube, $I_{ON}/I_{OFF} > 10^4$ at $V_D = -0.5$ V, and a subthreshold swing of ~130 mV/dec (Figure 4b,c). The notable properties of the device were that its saturation current reached as high as ~17 μA at $|V_G - V_T| = 1.0$ V. As shown in Figure 4d, the saturation current was significantly improved when the channel was scaled down to 15 nm. The improvement from the L_G scaling primarily relates to the suppression of scattering within the channel, and the nanotube device nearly reached the ballistic transport limit.[25]

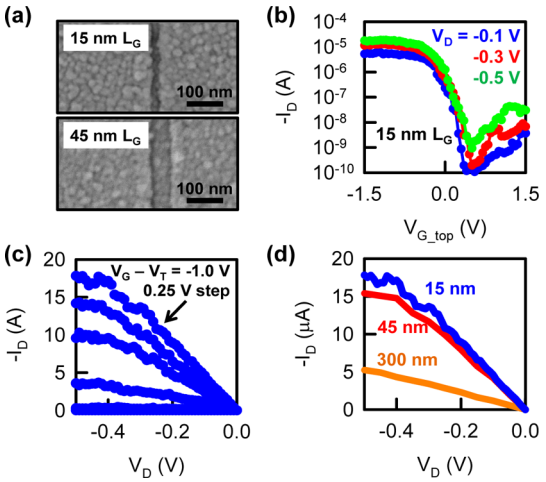

Figure 4. Short-channel device with a single solution-processed SWNT. The 10 nm ZrO_2 film (EOT ≈ 3.2 nm) was used as a gate dielectric. (a) Top-view SEM images of the devices (L_G = 15 and 45 nm). (b) Transfer characteristic for a device with L_G = 15 nm at $V_D = -0.1$ V, −0.3 V, and −0.5 V. (c) Output characteristics of the same device. The gate overdrive voltage was changed from 1.0 V in −0.25 V steps. (d) Output characteristics at the same gate overdrive voltage ($|V_G - V_T| = 1.0$ V) for the devices with different L_G.

These results are significantly improved over those from the best solution-processed nanotube transistors reported to date.[16,17,19,20,33] Furthermore, Figure 4d shows how L_G scaling affects the low-field slope and saturation current. Note how similar the curves are for 15 and 45 nm L_G devices, indicating that at low fields, scattering in the channel plays a minor role in device performance. This is evidence of reaching ballistic channel transport (negligible channel resistance) and is consistent with previous reports on CVD nanotubes.[25,30,32] However, relatively higher subthreshold slope, lower saturation current, and lower transconductance values in our device, compared to the CVD nanotube devices,[25,30,32] can be attributed to the thicker EOT. Therefore, we anticipate an improved switching behavior will be obtained for the current device when using thinner high-κ gate dielectrics.

We further developed highly scaled devices with multiple solution-processed nanotube channels. Those transistors were fabricated in different batches. The volume of the nanotube solution for the spin alignment technique increased from 4 to 6 μL to obtain a large amount of multiple nanotube channels. The average number of nanotubes inside the channel with 2 μm width is estimated as 3−4 from the test structure (inset of Figure 5a). The thickness of ZrO_2 film for gate dielectrics was 10 nm. Oxygen treatment was also employed for the device fabrication.

Figure 5 panels a, b, and c show the transfer characteristics of 15, 45, and 65 nm L_G devices with multiple nanotube channels, respectively. The I_{ON}/I_{OFF} ratio for the 15 nm L_G device is larger than 10^4 at $V_D = -0.1$ V and larger than 10^3 at $V_D = -0.5$ V. Moreover, the

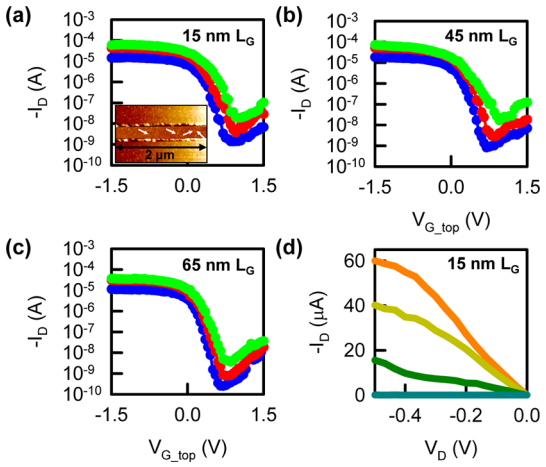

Figure 5. Representative transfer characteristics of the devices with multiple SWNT channels at different V_D (−0.1 V, −0.3 V, and −0.5 V) for (a) 15 nm, (b) 45 nm, and (c) 65 nm devices. Inset in frame a: AFM of a test structure (*z*-scale is 30 nm) to extract the number of nanotubes inside the channel. The estimated number of nanotubes inside the channel is 3−4. (d) Output characteristics of the 15 nm L_G device. The gate overdrive voltage was increased from 0 to 1.5 V in 0.5 V step.

transconductance of the 15 nm L_G device is up to 73 μS. These large I_{ON}/I_{OFF} ratio and excellent transconductance suggest that the devices with multiple solution-processed nanotube channels are also effectively controlled by the combination of a top-gate structure and high-κ gate insulators. The 15 nm L_G device also shows current saturation around $V_D = -0.35$ V at $|V_G - V_T| =$ 1.5 V in the on-state (Figure 5d). However, there is a slight increase in the minimum current as L_G decreases, primarily a result of back-injection of carriers into the conduction band from the drain. In addition, the slightly increased subthreshold values and V_T roll-up for decreasing L_G, indicating mild short-channel effects, are attributed to the somewhat thick gate dielectric layer and may be addressed by using thinner EOT. Note that the I_{ON} levels for the two set of devices that have $L_G \leq 45$ nm are almost consistent ($\langle I_{ON} \rangle =$ 60 μA for 15 nm L_G devices, $\langle I_{ON} \rangle = 61$ μA for 45 nm L_G devices, and $\langle I_{ON} \rangle = 36$ μA for 65 nm L_G devices at $|V_G - V_T| = 1.5$ V) in the same manner as the results of single nanotube channel devices.

SUMMARY

We evaluated the performance of short-channel, top-gate, solution-processed carbon nanotube devices with high-κ gate dielectrics. Electrical characterization of the device indicates that the structural defects in the solution-processed nanotubes, which might result from the purification or suspension processes and can act as localized electron-scattering centers, limit the electron transport characteristics; however, they do not significantly affect the quality of the contact between the nanotubes and metal electrodes. Moreover, we found that the oxygen treatment can effectively decrease the contact resistances. Therefore, measurements of the 15 nm L_G devices with a single solution-processed nanotube showed a transconductance of 32 μS and a high I_{ON}/I_{OFF}. These values are comparable to those previously reported for CVD nanotubes and demonstrate the potential of solution-processed nanotubes for future nanoelectronics. Moreover, the further aggressive scaling down to 15 nm L_G for the multiple nanotube channel devices reaches a transconductance of 73 μS with a reasonable I_{ON}/I_{OFF} ratio. Further progress will follow improvement in the purity and placement of the solution-processed nanotubes and the optimization of the transistor structure and integration.

Conflict of Interest: The authors declare no competing financial interest.

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