

Gate tunable WSe₂/SnSe₂ backward diode with ultra-high reverse rectification ratio

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ABSTRACT: Backward diodes conduct more efficiently in the reverse bias than in the forward bias, providing superior high frequency response, temperature stability, radiation hardness, and 1/f noise performance than a conventional diode conducting in the forward direction. Here we demonstrate a van der Waals material based backward diode by exploiting the giant staggered band offsets of WSe₂/SnSe₂ vertical heterojunction. The diode exhibits an ultra-high reverse rectification ratio (R) of $\sim 2.1 \times 10^4$ and the same is maintained up to an unusually large bias of 1.5 V – outperforming existing backward diode reports using conventional bulk semiconductors as well as one- and two-dimensional materials by more than an order of magnitude, while maintaining an impressive curvature coefficient (γ) of $\sim 37 \text{ V}^{-1}$. The transport mechanism in the diode is shown to be efficiently tunable by external gate and drain bias, as well as by the thickness of the WSe₂ layer and the type of metal contacts used. These results pave the way for practical electronic circuit applications using two-dimensional materials and their heterojunctions.

KEYWORDS: WSe₂, SnSe₂, van der Waals heterostructure, backward diode, reverse rectification ratio, curvature coefficient, charge transport.

Introduction:

Heterostructures formed by incorporating different semiconductor materials play a vital role in the modern semiconductor world as they offer unique properties employing complementary features of each material. The distinctive electronic and optoelectronic characteristics of heterojunctions have been deployed in a wide variety of solid-state devices¹. However, lattice matching across the interface is critical in achieving desired performance as any epitaxial distortion induces detrimental interface defect states. Van der Waals force across layered two-dimensional (2D) materials eases the heterostructure fabrication from this aspect². Vertical stacking of these 2D materials opens the possibility of assembling different layers arbitrarily without any deliberation over the precision of lattice matching unlike their bulk counterparts³⁻⁵. Recent developments in vapor phase growth techniques facilitate the direct synthesis methods of 2D/2D vertical heterojunctions⁶⁻⁸. These 2D heterostructures have been recently investigated for different device applications such as transistors⁹⁻¹², photodetectors^{13,14}, photovoltaics^{15,16} and LEDs^{17,18}.

Backward diode^{1,19-21} is a special type of diode that conducts more efficiently in the reverse direction than in the forward direction, typically due to strong Zener tunneling under reverse bias. These diodes do not suffer from minority carrier storage induced capacitance as in a diffusion controlled forward biased conventional diode operation. Consequently, backward diodes find widespread applications in high frequency switches, microwave detectors and mixers²²⁻²⁵. The low threshold conduction in the reverse bias is also useful for small peak to peak signal rectification

applications. Backward diodes typically provide superior temperature stability, radiation hardness, and $1/f$ noise performance compared to conventional diodes^{26,27}.

SnSe₂, a tin based transition metal dichalcogenide, exhibits a large electron affinity²⁸ with degenerate n-type doping. On the other hand, WSe₂ shows ambipolar behavior²⁹ where the characteristics can be modulated by gate voltage and contact metal. The band offset between SnSe₂ and WSe₂ forces a highly staggered type II band alignment³⁰⁻³². In this work, we exploit this property of the WSe₂/SnSe₂ heterojunction to demonstrate a backward diode with a large curvature coefficient of $\sim 37 \text{ V}^{-1}$, coupled with an extremely high reverse rectification ratio of $\sim 2.1 \times 10^4$, outperforming previously reported numbers^{19,20,33-43}. We also demonstrate an efficient modulation of the rectification ratio by tuning the applied gate voltage, contact metals, and thickness of the WSe₂ layer. Finally, we show that the effective current transfer length at the heterointerface of these vertical heterojunctions can be very large encompassing the entire overlap area of WSe₂ and SnSe₂, avoiding current crowding, which is in sharp contrast to typical metal-2D semiconductor contact interfaces, with small transfer length^{44,45}.

Results and Discussions:

We first study the degree of charge transfer across WSe₂/SnSe₂ heterojunction owing to the highly staggered type II band alignment (Figure 1a)^{46,47}. We employ photoluminescence (PL) spectroscopy to obtain first-hand information about charge transport processes across the interface⁴⁴. To have an easy optical access to the photoactive WSe₂ layer, for the PL experiment, we make a WSe₂-top/SnSe₂-bottom heterostructure (see **Experimental Section**) on a Si wafer coated with 285 nm SiO₂, as schematically depicted in Figure 1b. An optical image of the structure is shown in the top panel of Figure 1c. Atomic Force Microscopy (AFM) along the white dashed line in Figure 1c suggests that the thickness of WSe₂ and SnSe₂ flakes are 4.7 nm and 22.6 nm,

respectively (Figure 1d). The Raman spectra of different portions of the flakes, as characterized with a 532-nm laser illumination, are shown in Figure 1e. The isolated WSe₂ portion exhibits strong A_{1g} and 2LA(M) peaks at 251 cm⁻¹ and 258 cm⁻¹ respectively⁴⁸, which are suppressed at the junction area. On the other hand, the junction clearly shows the E_g and A_{1g} peaks of SnSe₂ at 110 cm⁻¹ and 184.5 cm⁻¹ respectively.

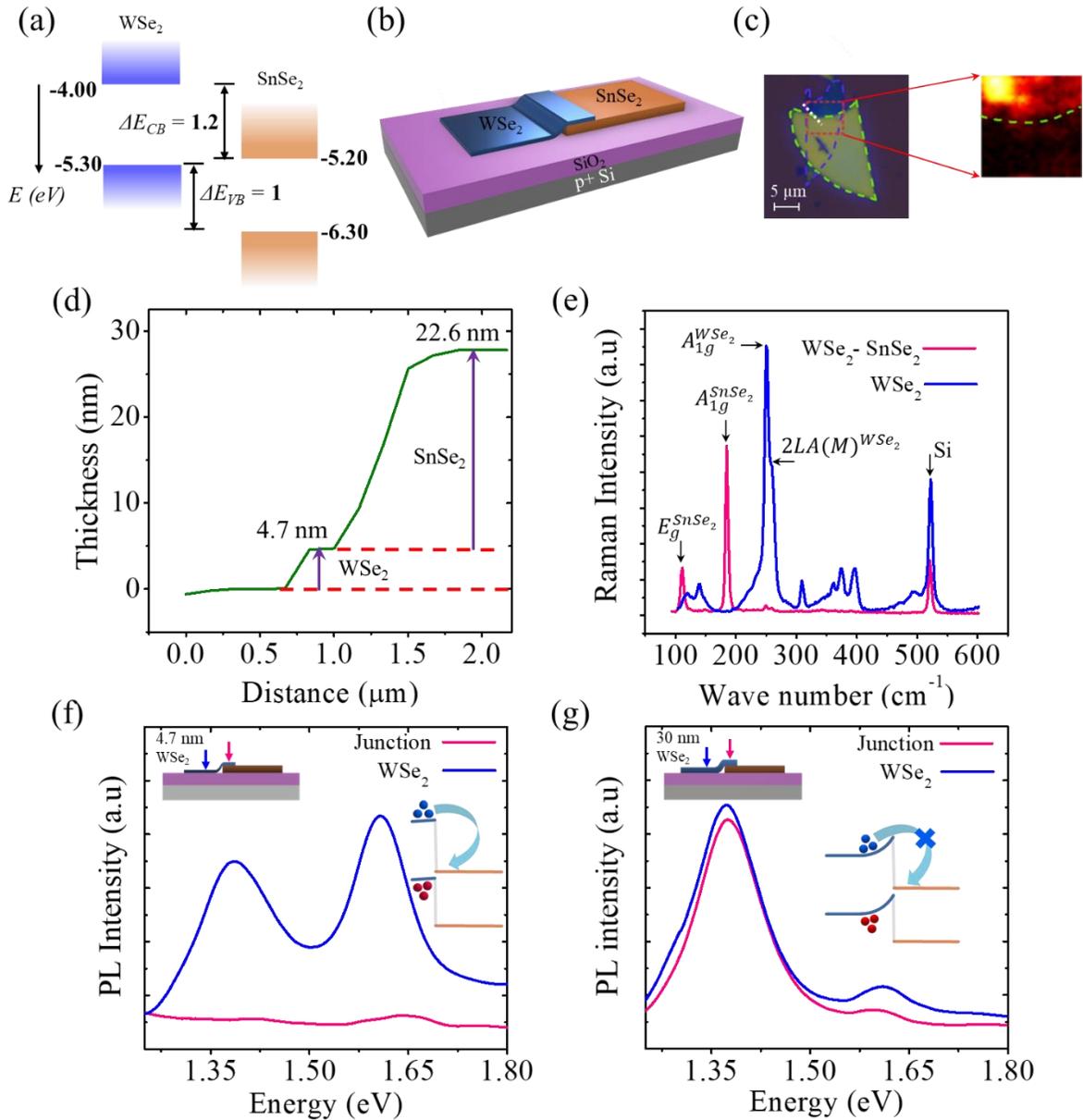


Figure 1: (a) Band alignments of bulk WSe₂ and SnSe₂. (b) Schematic of WSe₂-top/SnSe₂-bottom heterojunction used for PL mapping. (c) Optical image of the heterojunction used for the PL experiment and the corresponding PL map of the region surrounded by red dashed lines. The dark portion from the junction suggest strong PL quenching. (d) Thickness characterization from AFM depicting thickness profiles of WSe₂ (4.7 nm) and SnSe₂ (22.6 nm) regions along the white dotted line in (c). (e) Raman spectra (using 532 nm laser) measured on isolated WSe₂ portion and on WSe₂/SnSe₂ junction. (f-g) PL spectra of (f) thin (~4.7 nm) and (g) thick (~30 nm) WSe₂ flake, in isolated (blue) and in junction (pink) area. Top Inset, Schematic of the cross section of the structure. Right inset, Band diagram illustrating charge transfer. Band bending in SnSe₂ is negligible owing to its degenerate doping.

In Figure 1c, we show the WSe₂ indirect peak PL intensity mapping of the area surrounded by the red dashed lines. We observe almost complete quenching of PL intensity at the junction, compared with the isolated WSe₂ portion. Figure 1f shows the corresponding PL spectra of the characterized junction and isolated WSe₂ portion. The large conduction band offset of ~1.2 eV at the WSe₂/SnSe₂ junction as described in Figure 1a suggests efficient transfer of the photo-excited electrons from WSe₂ to SnSe₂, supporting the WSe₂ PL quenching. Interestingly, the PL quenching is not significant when the thickness of the WSe₂ flake is increased. For example, the PL spectra for a 30-nm thick WSe₂ flake on SnSe₂ is shown in Figure 1g. Such thickness dependent PL quenching can be explained from the band bending on the WSe₂ side in both the investigated structures. Under equilibrium, to maintain the band offsets at the WSe₂/SnSe₂ interface and zero field at the top WSe₂/air interface, the bands of WSe₂ in the depletion region are forced to bend concave downward from WSe₂/SnSe₂ interface, which is supported by the moderate p-doping in WSe₂. When WSe₂ flake is too thin, bands cannot bend steeply in the constrained physical space to reach equilibrium positions as illustrated in the inset of Figure 1f. Here, the photo-excited electrons in WSe₂ get transferred to SnSe₂ side because the minimal band bending in WSe₂ does not form any barrier. But in the case of thick WSe₂ as in the inset of Figure 1g, bands can bend sufficiently, which forms a barrier for the electrons inhibiting their transfer to SnSe₂.

Before discussing the electrical transport properties of WSe₂/SnSe₂ junction, we discuss the individual behaviour of SnSe₂ and WSe₂ channels using back gated structures, as summarized in Figure 2. SnSe₂ is a degenerately n-doped semiconductor with Fermi-level lying about 0.2-0.3 eV above the conduction band⁴⁹. We obtained similar values using KPFM measurements⁵⁰. This results in ohmic and highly conductive I_{ds} - V_{ds} response from SnSe₂ channel with Ni/Au contacts, as shown in Figure 2a. The degenerate doping results in negligible modulation of current by the back gate voltage (V_g).

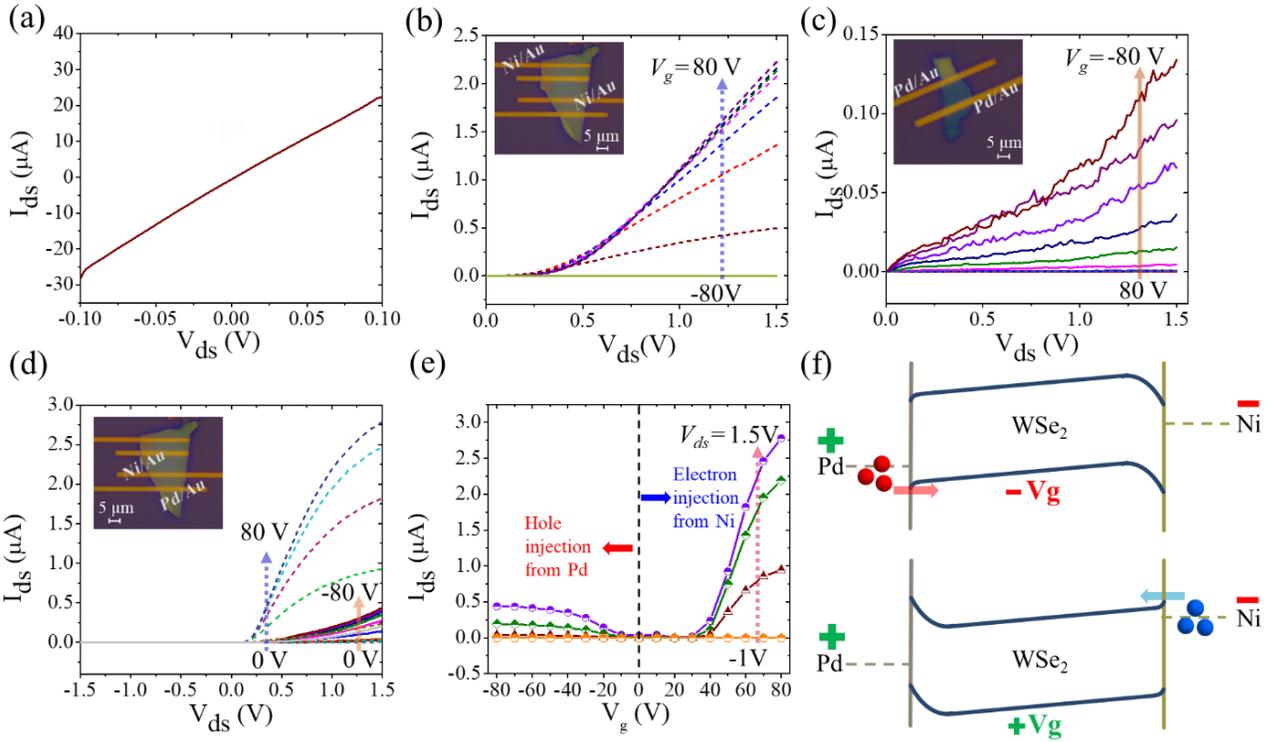


Figure 2: (a) I_{ds} - V_{ds} characteristics across the two Ni/Au contacts on SnSe₂. (b-c) I_{ds} - V_{ds} characteristics of back gated WSe₂ channel with (b) two Ni/Au contacts and (c) two Pd/Au contacts. V_g varies from -80 V to 80 V in steps of 10 V. Inset, an optical image of the fabricated device. (d-e) I_{ds} - V_{ds} and I_{ds} - V_g characteristics of back gated asymmetric WSe₂ channel with Pd/Au and Ni/Au contacts. Ni/Au is grounded while bias is applied to Pd/Au. Inset of (d), an optical image of the fabricated device. (f) Band diagrams of (d) and (e), under forward bias, with negative (top panel) and positive (bottom panel) gating. Under negative V_g , Pd efficiently injects holes (red

spheres) into the WSe₂ channel, while under positive V_g , Ni injects efficiently electrons (blue spheres).

On the other hand, as explained in Figures 2b-c, Ni contacted WSe₂ behaves as an nFET with an increasing current for $V_g > 0$, while Pd contacted WSe₂ channel behaves like a pFET with an increasing current for $V_g < 0$. These observations suggest that Ni (Pd) can efficiently inject electrons (holes) into the WSe₂ channel. Consequently, the asymmetric device with Ni/Au and Pd/Au as two different contacts to WSe₂ channel exhibits a perfectly rectifying, but ambipolar behavior, as shown in Figures 2d-e. Figure 2f explains the forward bias current mechanism under both gating conditions. At positive gate voltage, under forward bias (Ni side grounded, Pd side biased), Ni efficiently injects electrons, providing large current. However, under reverse bias condition, Pd being poor injector of electrons into WSe₂, the current is suppressed. On application of negative gate voltage, under forward bias condition, Pd efficiently injects holes. However, poor hole injection by Ni under reverse bias condition suppresses the current.

We next fabricate a back-gated heterojunction diode D1 using the WSe₂/SnSe₂ stack as illustrated in Figure 3a with Ni/Au contact on SnSe₂ and Pd/Au contact on WSe₂ (see **Experimental Section**). The thickness of the WSe₂ and the SnSe₂ flakes are 8 nm and 122 nm, respectively, as suggested by AFM characterization in Figure 3b. Contrary to the PL experiment structure, we now use WSe₂-bottom/SnSe₂-top heterostructure to efficiently modulate ambipolar WSe₂ by the back gate. The V_g dependent current-voltage characteristics, as summarized in Figure 3c-d, show three important features. First, the magnitude of the current increases with both negative and positive V_g , retaining the ambipolar behavior of WSe₂. Second, both the forward ($I_{forward}$) and reverse ($I_{reverse}$) bias currents can be efficiently controlled by 6 orders of magnitude by tuning V_g . Third, the diode conducts heavily in the reverse bias regime than in the forward bias, particularly for $V_g > 0$, and

hence can be used as a backward diode. In the inset of Figure 3d, we show the turn on behavior of the diode in the linear scale under reverse bias, with suppressed conduction in the forward bias.

The reverse rectification ratio ($R = \frac{I_{reverse}}{I_{forward}}$) is plotted as a function of V_g and $|V_{ds}|$ in Figure 3e.

Here $I_{reverse}$ and $I_{forward}$ are measured at $-V_{ds}$ and $+V_{ds}$, respectively. R is found to reach an impressive value of ~ 220 for small positive V_g and large $|V_{ds}|$.

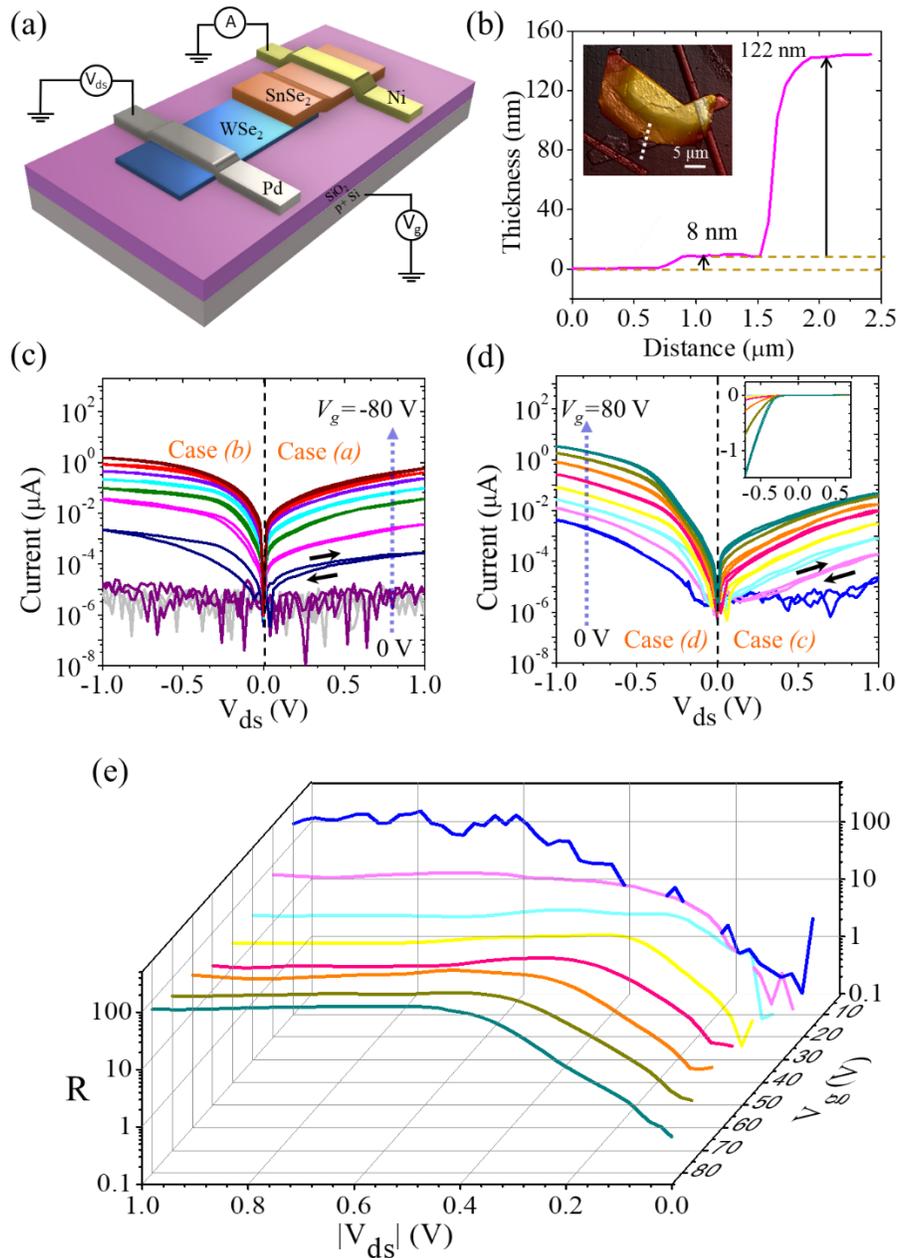


Figure 3: (a) Schematic of back gated WSe₂-bottom/SnSe₂-top device (D1) fabricated for electrical measurement. (b) Thickness profile of flakes along the white dashed line on AFM image of the device in the inset. (c) Log scale I_{ds} - V_{ds} characteristics of the device under negative gating, starting from 0 V to -80 V in steps of 10 V. The black arrows indicate the forward and reverse sweep, with negligible hysteresis. (d) Log scale I_{ds} - V_{ds} characteristics of the device under negative gating, starting from 10 V to 80 V in steps of 10 V. Inset, Linear scale plot of I_{ds} - V_{ds} . (e) Reverse rectification ratio ($R = \frac{I_{reverse}}{I_{forward}}$) of D1 as a function of drain bias and positive gate voltage. $I_{reverse}$ and $I_{forward}$ are measured at $-V_{ds}$ and $+V_{ds}$, respectively.

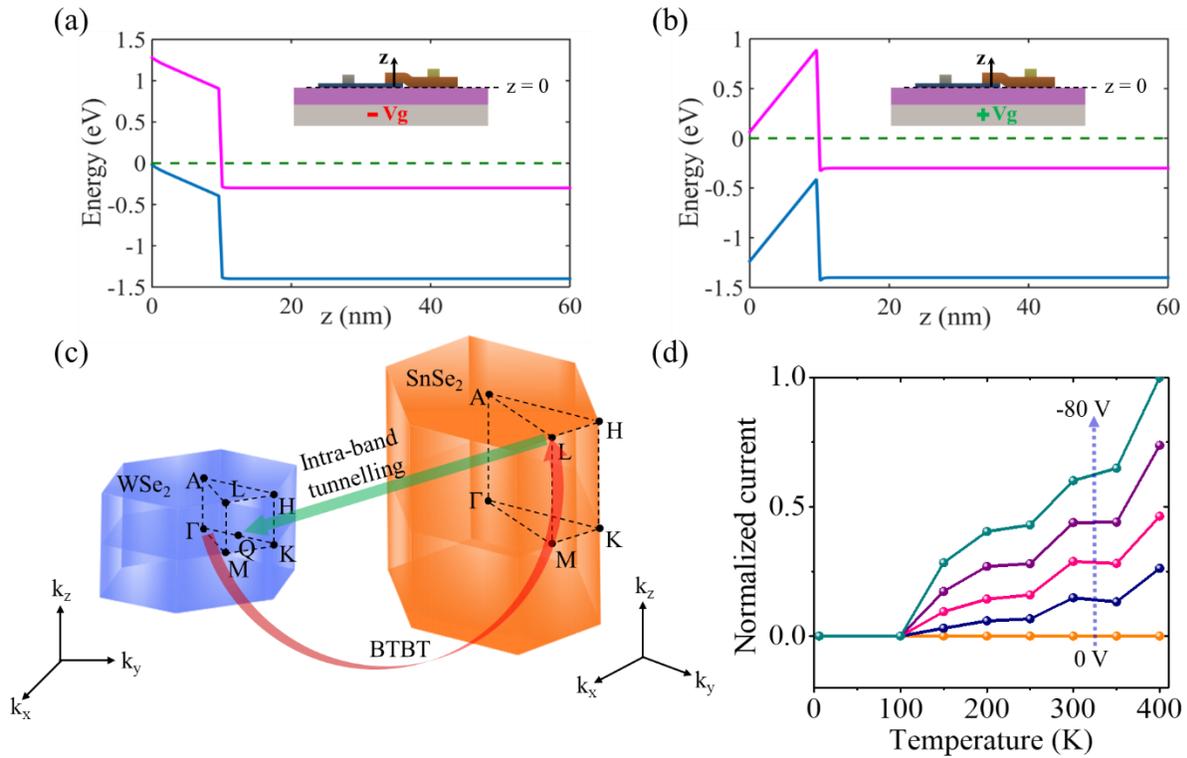


Figure 4: (a)-(b) Simulated 1D equilibrium band diagrams across the vertical cross-section of the heterojunction under (a) negative and (b) positive gating. The green dashed line indicates the chemical potential. (c) First Brillouin zones of bulk WSe₂ (blue) and bulk SnSe₂ (orange). Band to Band tunnelling (BTBT) across VB of WSe₂ and CB of SnSe₂ is shown by red arrow while green arrow depicts the intra-band electron tunnelling from CB of SnSe₂ to CB of WSe₂. (d) Normalized current across WSe₂/SnSe₂ device at $V_{ds} = -0.5$ V, as a function of temperature at gate voltages varying from 0 V to -80 V in steps of 10 V.

To understand the large magnitude of reverse current from the nature of the WSe₂/SnSe₂ vertical heterojunction, we self-consistently solve 1D Poisson equation in conjunction with semi-classical charge density to obtain the band bending along the vertical z direction, with the WSe₂/oxide interface being taken as $z = 0$. The resulting band diagrams in equilibrium are shown in Figure 4a-b for negative and positive V_g . The band diagrams clearly indicate that the thickness of the WSe₂ film and the magnitude of V_g play a key role in determining the vertical field in WSe₂, while the SnSe₂ bands remain nearly flat owing to its degenerate doping. From Figure 4a, it is clear that under negative gate voltage, reverse bias would favour strong band-to-band-tunneling (BTBT) of electrons in the vertical direction from valence band of WSe₂ to conduction band of SnSe₂. As shown in Figure 4c, the conduction band minimum (CBM) of SnSe₂ is located at the L point⁵¹ of the Brillouin zone whereas the valence band maximum (VBM) of WSe₂ occurs at the zone center (Γ point)⁵². This difference in crystal momentum results in an indirect BTBT of carriers at the heterojunction interface, indicated by the red arrow in Figure 4c. Temperature dependent current measurements at V_{ds} of -0.5 V in Figure 4d shows a strong suppression of the reverse bias tunneling current with reduced temperature, depicting the indirect nature of tunneling.

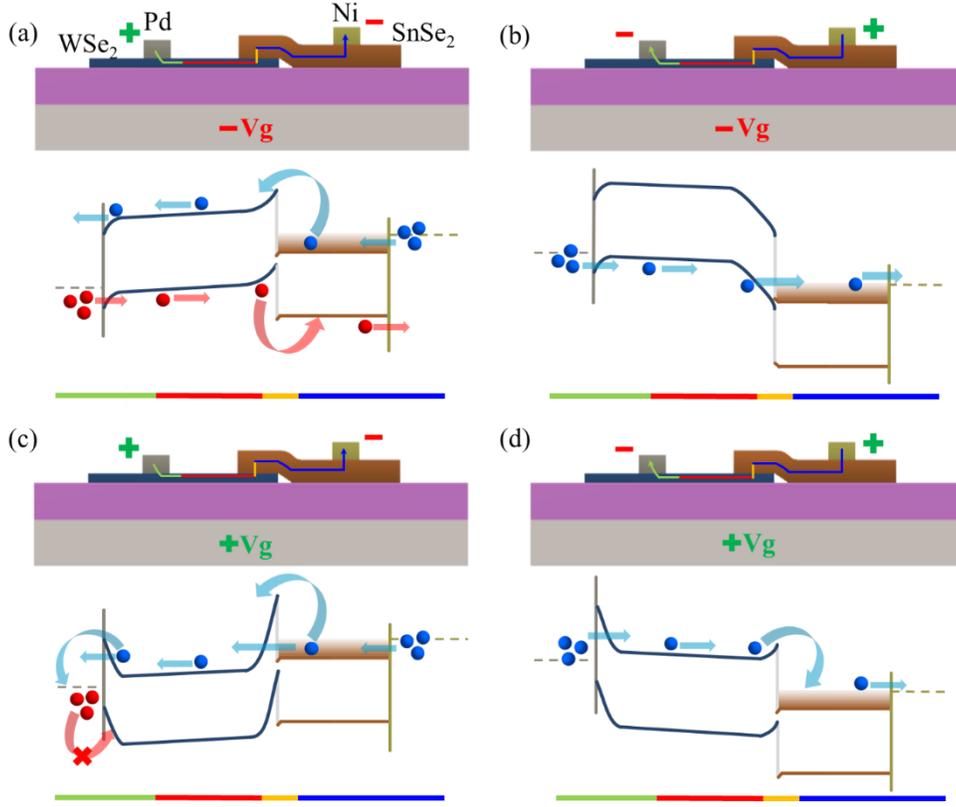


Figure 5: (a)-(d) The band diagrams and the corresponding device schematics of diode D1 for the four cases discussed in the text, namely (a) $V_g < 0, V_{ds} > 0$, (b) $V_g < 0, V_{ds} < 0$, (c) $V_g > 0, V_{ds} > 0$, and (d) $V_g > 0, V_{ds} < 0$. Color bar below each band diagram and multi-colored arrow in the respective device cross-section map the relevant regions along which transport is considered.

With the above discussion in background, we next discuss the carrier transport mechanism of Figure 3c-d in four different biasing conditions, namely (a) $V_g < 0, V_{ds} > 0$, (b) $V_g < 0, V_{ds} < 0$, (c) $V_g > 0, V_{ds} > 0$, and (d) $V_g > 0, V_{ds} < 0$. The corresponding band diagrams are shown in Figure 5a-d, respectively. The band diagrams are drawn along the arrows, as indicated in the corresponding schematic in each figure, and the different regions are represented by different color coding. In case (a), i.e. negative gate voltage and forward bias, Pd contact efficiently injects holes (shown by red spheres) in WSe₂, which overcome the WSe₂/SnSe₂ thermionic hole barrier under forward bias, and eventually get collected at the Ni contact of SnSe₂. For a given V_{ds} , the hole

injection from Pd contact to WSe₂ is a strong function of V_g , while electron injection from Ni contact to SnSe₂ is almost independent of V_g . However, the electrons (shown by blue spheres), being injected from Ni contact of SnSe₂ have to overcome the SnSe₂/WSe₂ electron barrier - relatively larger than the hole barrier and get collected by the Pd contact of WSe₂. Thus, the holes contribute to a major component of the forward current in case (a). For positive V_g and forward bias [case (c)], the hole injection from Pd is cut off, suppressing the hole current. On the other hand, positive V_g (Figure 5c) enhances the electron current, as the electrons from the conduction band of SnSe₂ can tunnel through to the conduction band of WSe₂ through the thin triangular barrier, the width of which is primarily determined by the thickness of the WSe₂ film and the magnitude of V_g . We note that such intra-band tunneling in the conduction band, also requires a change in crystal momentum, and hence inelastic in nature, as indicated by the green arrow in Figure 4c.

Under reverse bias, with negative V_g [case (b)], the current is primarily governed by the indirect BTBT at the WSe₂/SnSe₂ interface, as discussed earlier. This situation is depicted in Figure 5b, and results in large reverse current. However, under positive V_g [case (d)], the mechanism for strong reverse bias current cannot be explained by BTBT, as indicated by Figure 5d. Since the WSe₂ film used in the device is ultra-thin (~8 nm), under positive V_g , electrons can be injected from the Pd contact to the WSe₂ channel by tunneling induced field emission through the Schottky barrier, which eventually are drifted to the Ni contact, with almost zero barrier at larger V_{ds} . The WSe₂/SnSe₂ heterojunction device thus represents an excellent platform where the carrier transport mechanism can be controlled by the external biasing conditions, type of contacts used, and the thickness of the WSe₂ film.

To further improve the reverse rectification ratio, we note from Figure 3c-d that the diode works better as a backward diode under positive V_g . From the above discussion, $I_{forward}$ under positive V_g is controlled by the intra-band electron tunneling (Figure 5c) through the triangular barrier at the $\text{WSe}_2/\text{SnSe}_2$ interface. Figure 4b suggests that this tunneling barrier is controlled by the thickness of WSe_2 , and hence one can suppress $I_{forward}$ further by increasing the thickness of WSe_2 film. On the other hand, under reverse bias, with positive V_g , Ni contact on WSe_2 would be a better electron injector than Pd, as explained earlier in Figure 2, owing to Fermi level pinning closer to conduction band edge. Consequently, we next fabricate a $\text{WSe}_2/\text{SnSe}_2$ heterojunction diode D2, as shown in the bottom left inset of Figure 6a, with (i) relatively thick (~ 30 nm) WSe_2 , (ii) deposit Ni contact both on WSe_2 and SnSe_2 , and (iii) operate the same under positive V_g . Figure 6a shows the $I_{ds}-V_{ds}$ characteristics in the log scale, suggesting excellent suppression of $I_{forward}$, while $I_{reverse}$ is very strong. The linear scale plot is shown in the top right inset of Figure 6a, indicating near abrupt turn on with low backward threshold voltage (~ -0.1 V). The corresponding R is plotted in Figure 6b as a function of V_g and $|V_{ds}|$. We achieve an ultra-high $R \approx 2.1 \times 10^4$ at $V_g = 0$, which outnumbers the reverse rectification ratio of conventional Si, Ge backward diodes by two orders^{24,53}. The characteristics of another device from a different run are shown in Supporting Information S1, showing similar R value. The transport mechanism at forward and reverse bias is explained using the band diagrams in Figure 6c-d. Note that, even though the reverse current in D2 under positive gating is not governed by BTBT, the fact that it is a majority carrier drift driven process, facilitates fast device operation, by avoiding diffusion capacitance.

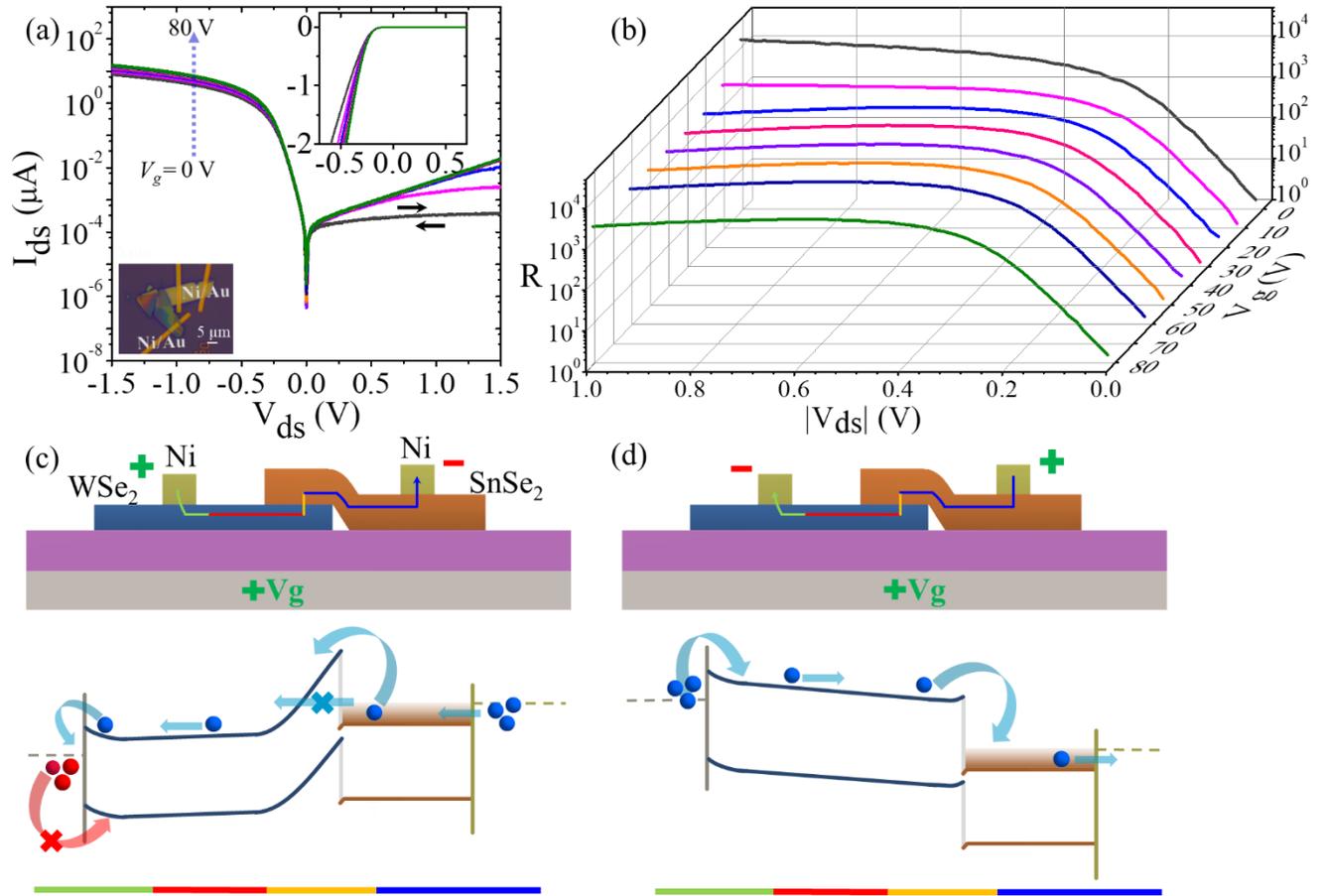


Figure 6: (a) I_{ds} - V_{ds} curves of device D2 in logarithmic scale at different positive gate voltages from 0 to 80 V varying in steps of 10 V. This device has both of the contacts as Ni/Au. The black arrows indicate the forward and reverse sweep, with negligible hysteresis. Inset, Linear scale plot of I_{ds} - V_{ds} showing excellent backward rectification. (b) Reverse rectification ratio (R) of D2 as a function of positive gate voltage and drain bias. (c)-(d) Band diagrams under positive gating, with (c) forward and (d) reverse bias, along with schematics of device cross section. The Color bar below each band diagram and multi-colored arrow in the respective device cross-section map the relevant regions along which transport is considered.

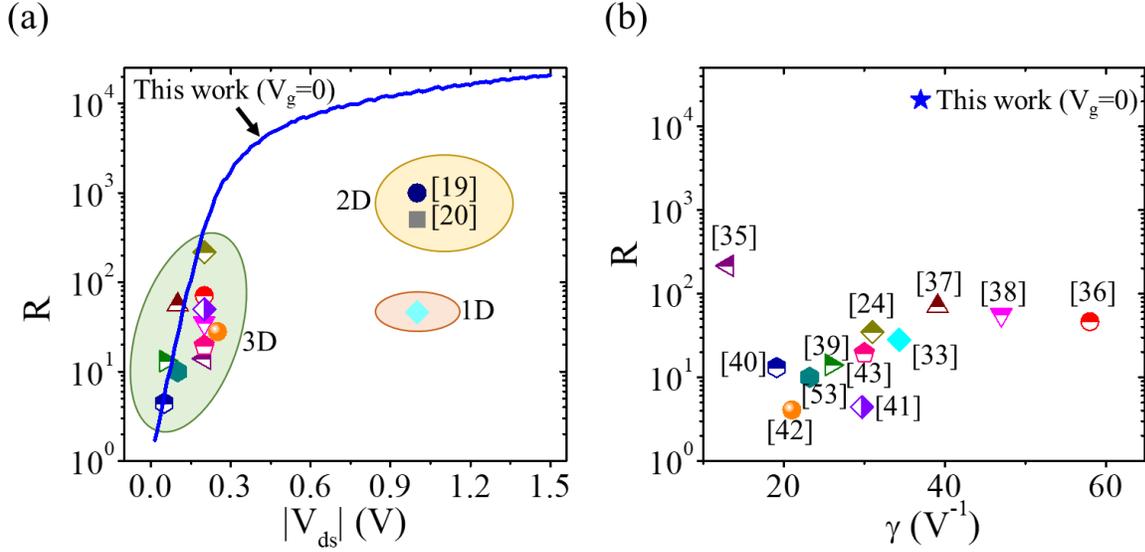


Figure 7: (a) Reverse rectification ratio (R) of different backward diodes reported in literature plotted (using symbols) as function of applied bias. The data from diodes based on 3D (Si, Ge, III-V), 2D (vdW materials) and 1D (nanotube) materials are clustered separately. The corresponding references for 3D and 1D systems are shown in (b). The solid blue line indicate R from device D2 reported in this work. (b) R versus γ benchmarking plot for different reports in literature. The blue star indicates data from device D2.

In Figure 7a, we benchmark the obtained R with backward diode data from literature, by plotting R as a function of applied bias. Our device exhibits more than an order of magnitude higher R compared with the best reported numbers, encompassing backward diodes based on 1D (nanotube), 2D (vdW materials) and 3D (Si, Ge, III-V) systems. Another unique feature of the reported device is that such a large R is maintained even at a very large bias of 1.5 V by suppressing the forward current efficiently, thanks to the large band offset between WSe₂ and SnSe₂. Curvature coefficient (γ) is another important figure of merit which determines the non-linearity and current sensitivity of a backward diode for detector applications^{34,54}, and is expressed as

$$\gamma = \left. \frac{d^2 I_{ds} / dV_{ds}^2}{dI_{ds} / dV_{ds}} \right|_{V_{ds}=0}$$

We achieve an impressive value of γ as 37 V^{-1} for diode D2, which is very close to the theoretical limit of 38.6 V^{-1} at 300 K for transport mechanism controlled by thermionic barrier. In Figure 7b, we benchmark our device with literature data in a R versus γ chart.

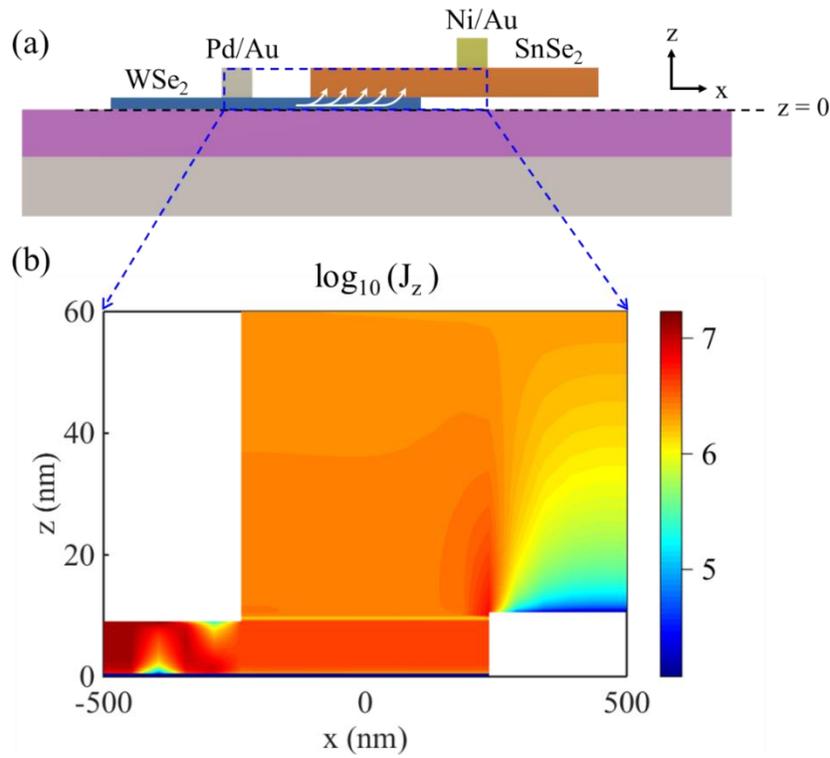


Figure 8: (a) Representation of device geometry (highlighted with blue dashed lines in the schematic) used in the simulation of current density distribution. The white arrows highlight the uniform transfer of current in the z direction across the entire interface. (b) Simulated distribution of z component of current density in log scale, suggesting uniform current transfer along the interface.

Finally, we comment on the transfer efficiency of the current from one layer to another in the WSe₂/SnSe₂ vertical heterojunction. Such a transfer depends on the relative values of the in-plane

and out-of-plane conductivity of each material at the interface⁵⁵. We model the current distribution across the entire structure in Figure 8a using the solution of current continuity equation⁵⁶. Conductivity values at different points along the z -direction are obtained from the corresponding carrier densities of solved poisson equation. The 2D current density distribution, $J_z(x, z)$, is plotted in Figure 8b, depicting how the current flows across the interface. The current density plot indicates that the transfer of current happens almost uniformly across the entire overlap region of WSe₂/SnSe₂. This is in stark contrast with a typical metal-2D semiconductor interface, where the effective contact area is limited by so called “*transfer length*”^{44,57}, and is only about ~100 nm for metal/TMDs interface⁴⁵. This is understood from the fact that the effective overlap length across which the current is transferred from one material to the other depends on the ratio of the in-plane and the out-of-plane resistivity. Each layer of van der Waals materials offers a resistance to the current flow in its plane which is lower than the resistance offered by the out-of-plane vertical interface across the layers. Consequently, current crowding at such heterointerface is avoided. The entire overlap area is thus important for carrier collection and can be used as a device design parameter to control the total current through the diode.

Conclusion:

In conclusion, we demonstrate the highly conducting nature of a gate tunable WSe₂/SnSe₂ heterojunction under reverse bias which is appealing for high performance backward diode applications. Drift driven reverse current conduction enables high speed diode operation. By efficiently manipulating the current transport mechanism using gating and device parameter optimization, we achieve a superior backward diode with small reverse threshold (~ -0.1 V), sharp reverse turn on, large reverse rectification ratio (2.1×10^4), almost completely suppressed forward current up to a large bias of 1.5 V, and a high curvature coefficient (37 V^{-1}). This opens

up interesting avenues for high frequency, low noise, radiation hard electronic circuit applications based on vdW backward diode. Further, it is shown that the vertical current transfer efficiency from one layer to the other at the heterojunction interface has a large transfer length, encompassing the entire physical overlap area of the two vdW materials – a result that would be useful for a wide variety of vdW based vertical heterojunctions.

Experimental Section:

Fabrication and characterization of heterojunction: For PL experiment, we first mechanically exfoliate SnSe₂ flake of desired thickness on top of Si/SiO₂ substrate. We then exfoliate WSe₂ on PDMS sheet and transfer this to a glass slide. Using a micromanipulator, we maneuver the WSe₂ flake of interest on PDMS sheet over the SnSe₂ flake that is on Si/SiO₂ substrate. Then the glass slide with PDMS and substrate are brought close to each other adjusting microscope stage movement in a very slow manner till we observe air release at their interface. At this point, we retract the stage gently to identify a successful formation of SnSe₂-bottom/WSe₂-top structure. For measuring the electrical characteristics of the back gated heterojunction diode, we swap the WSe₂ and SnSe₂ layers making a WSe₂-bottom/SnSe₂-top structure for efficient back gating. Pd/Au (20 nm/50 nm) and Ni/Au (10 nm/50 nm) contacts are patterned by e-beam lithography and deposited with e-beam evaporation technique. All electrical measurements are done using an Agilent B1500 device analyzer keeping the sample chamber pressure less than 10⁻⁵ Torr.

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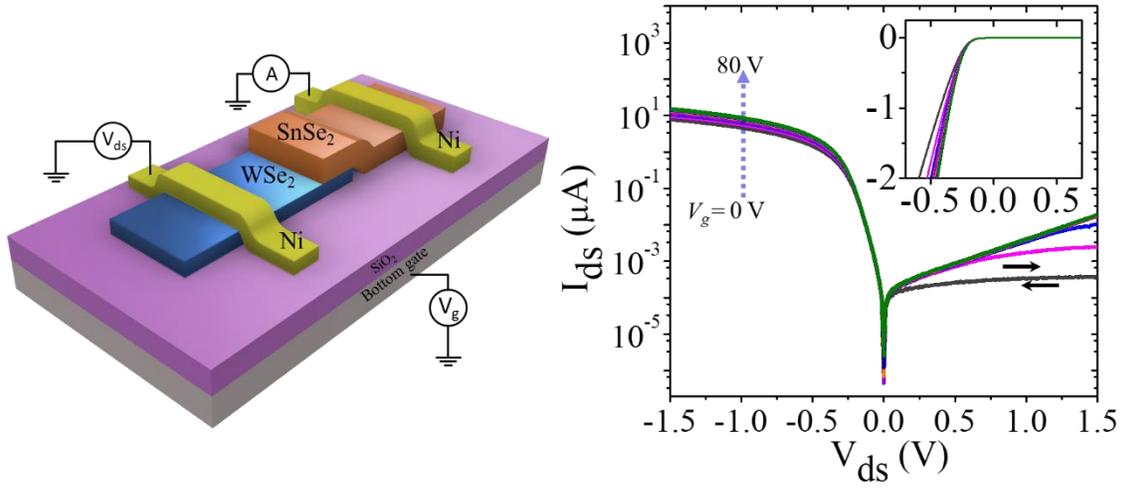
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Supporting Information S1

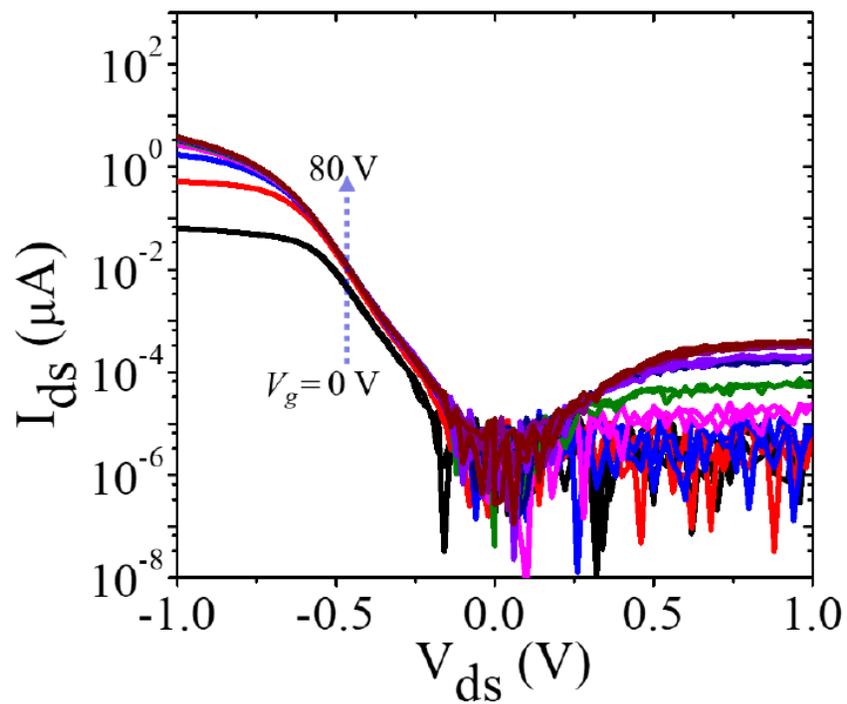


Figure S1: Characteristics of a Ni contacted $\text{WSe}_2/\text{SnSe}_2$ backward diode, obtained from a different run, showing large reverse current and suppressed forward current, giving rise to large reverse rectification ratio.