High-K materials and Metal Gates for CMOS applications

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Abstract

The scaling of complementary metal oxide semiconductor (CMOS) transistors has led to the silicon dioxide layer used as a gate dielectric becoming so thin that the gate leakage current becomes too large. This led to the replacement of SiO_2 by a physically thicker layer of a higher dielectric constant or 'high-K' oxide such as hafnium oxide. Intensive research was carried out to develop these oxides into high quality electronic materials. In addition, the incorporation of Ge in the CMOS transistor structure has been employed to enable higher carrier mobility and performance. This review covers both scientific and technological issues related to the high-K gate stack - the choice of oxides, their deposition, their structural and metallurgical behaviour, atomic diffusion, interface structure, their electronic structure, band offsets, electronic defects, charge trapping and conduction mechanisms, reliability, mobility degradation and oxygen scavenging to achieve the thinnest oxide thicknesses. The high K oxides were implemented in conjunction with a replacement of polcryslliane Si gate electrodes with metal gates. The strong metallurgical interactions between the gate electrodes and the HfO_2 which resulted an unstable gate threshold voltage resulted in the use of the lower temperature 'gate last' process flow, in addition to the standard 'gate first' approach. Work function control by metal gate electrodes and by oxide dipole layers is discussed. The problems associated with high K oxides on Ge channels are also discussed.

Glossary

ALD atomic layer deposition
CB conduction band
CBO conduction band offset
CMOS complimentary metal oxide semiconductor
CNL charge neutrality level
CV capacitance voltage
CVD chemical vapour deposition
DB dangling bond
DOS density of states
EA electron affinity
ECT equivalent capacitance thickness
EOT equivalent oxide thickness
ESR electron spin resosnance
EWF effective work function
FET field effect transistor
GGA generalised gradient approximation
LDA local density approximation
MEIS medium energy ion scattering
MIGS metal induced gap states
MOCVD metla organic chemical vapour deposition
MOS metal oxide semiconductor
MOSFET metal oxide semiconductor field effect transistor
MO_x arbitrary metal oxide
NMOS n-type MOS
PMOS p-type MOS
RCS remote Coulombic scattering
RPS remote phonon scattering
SBH Schottky barrier height
TAT trap assisted tunnelling
T_{inv} inversion thickness
Vt threshold voltage (of FET)
Vfb flat band voltage
VB valence band
VBO valence band offset
WF work function

1 Introduction

The incorporation of high-K dielectrics with metal gates into a manufacturable, high volume transistor process is the result of tremendous ingenuity and effort by many scientists and engineers [1]. We review that progress in this article, with an emphasis on the key developments in the high-K/metal gate stack process. We also summarize recent results on incorporation of Ge in the transistor, which appears to provide a viable route to higher performance technology.

It is more than a decade since high-K gate dielectric research for Si-based transistor technology was first reviewed [2,3]. We begin this review with a brief summary of the scaling issues that drove the incorporation of high-K dielectrics and metal gate technologies. We then discuss the materials chemistry of the high-K dielectrics employed in transistor fabrication. This is followed by a review of the current understanding of the high-K/semiconductor interfacial bonding. Defects, which play an important role in high-K dielectrics, are then discussed. Of course, the electrical performance of the transistor is paramount, and we review the recent developments, including work function control for the transistor gate stack.

1.1 Scaling and gate capacitance

The complementary metal oxide semiconductor (CMOS) field effect transistor (FET) made from silicon is the most important electronic device. This has arisen because of its low power consumption and its continuing performance improvement over forty years following Moore's Law of scaling. This "law" notes that the number of devices on an integrated circuit increases exponentially, doubling every 2-3 years. The minimum feature size in a transistor decreases exponentially each year (Fig. 1).

Until recently the materials and elements used in CMOS technology were very few – Si, O, P, Al, B, H and N. Now the situation has reversed. New materials are being introduced in many areas, from Cu instead of Al for interconnects, low dielectric constant materials such as SiOCH for inter-metal dielectrics, silicides as contact metals, and diffusion barrier materials such as TiN.

The SiO_2 layer used as the gate dielectric is now so thin (~1.2 nm) that the gate leakage current due to direct tunnelling of electrons through the SiO_2 becomes too high, exceeding 1 A/cm^2 at 1 V (Fig. 2). This means that the static power dissipation would be unacceptable [2-13]. In addition it becomes increasingly difficult to make such thin films, and they become increasingly unreliable. Thus, SiO_2 had to be replaced.

An FET is a capacitance-operated device, where the FET source-drain current depends on the gate capacitance, which is most simply expressed as

$$C = \frac{\varepsilon_0 K A}{t} \tag{1}$$

where ε_0 is the permittivity of free space, K is the relative dielectric constant, A is the area and t is the oxide thickness. Tunnelling currents decrease exponentially with increasing distance. Hence, the solution to the tunnelling problem is to replace SiO_2 with a physically thicker layer of new material of higher K, as shown in transmission electron microscope images Fig 3. This will keep the same capacitance, but decrease the tunnelling current. These new gate oxides are called 'high K oxides'.

For a device designer, as the precise material does not matter, it is convenient to define an electrical thickness of a new oxide in terms of its equivalent silicon dioxide thickness or 'equivalent oxide thickness' (EOT)

$$t_{ox} = \text{EOT} = (3.9/K)\, t_{HiK} \tag{2}$$

Here, 3.9 is the static dielectric constant of SiO_2. The objective is to develop high K oxides to allow scaling to continue to very low EOT values.

The gate leakage problem has been apparent since the late 1990's [14], but the criteria for choosing the oxide were unclear. In about 2001, the choice of oxide had narrowed to HfO_2, but the problems of making HfO_2 into a successful electronic material were great. Nevertheless, the increasing importance the low-power electronics in cell-phones, lap-tops, and portable electronics mean that the problem had to be solved. Low standby power CMOS requires a leakage current of below $1.5x10^{-2}$ A/cm^2 rather than just 1 A/cm^2. There were many difficulties in manufacturing high K oxides /metal-gate stacks but these were gradually overcome. Intel now manufactures the chips with second generation of high K/metal K stacks [1,15] and have now implemented high K for FINFET structures as well.

The second critical issue was the realisation that metallurgical problems would limit the introduction of the high K/metal gate stack in an exact replica of the SiO_2 gate process (gate first) [16], and that instead a 'replacement gate', 'dummy gate', or 'gate last' process [15] would need to be used, to limit the exposure of high K/ metal gate interface to high temperatures.

In a key early paper, Gusev et al [17] identified four key problems for successful introduction of high K oxides -

(1) be able to continue scaling to lower EOTs,
(2) stop the gate threshold instabilities caused by the high defect densities,
(3) limit the loss of carrier mobility in the Si channel when using high K oxides,
(4) control the gate threshold voltage, which resulted in the need for metal gates.

1.2 Metal gates and Effective Capacitance Thickness (ECT)

Viewing the Si – gate stack band diagram of a MOSFET (Fig. 4), the gate capacitance is the series combination of three terms, the oxide capacitance, the depletion capacitance of the gate electrode, and the capacitance of the Si channel carriers. These three capacitances add as (Fig 5)

$$1/C = 1/C_{ox} + 1/C_D + 1/C_{Si} \quad (3)$$

As C varies as 1/t, capacitors in series combine as a sum of effective distances. Thus we can define an 'effective capacitance thickness' ECT of the whole gate stack as

$$ECT = t_{inv} = EOT + t_{gate} + t_{Si} \quad (4)$$

ECT is also known as the inversion thickness t_{inv}.

The channel capacitance C_{Si} arises because the 2-dimensional electron gas of carriers in the channel cannot lie infinitely close to its surface, but delocalises a few Angstroms into the Si. This capacitance contribution is intrinsic and cannot easily be changed. High-k dielectric materials are often first evaluated using a MOS capacitor structure, and sunsequently utilizing a transistor structure measuring the substrate (depletion) and source/drain (inversion) capacitance ("Split CV") independently [18,19].

Previously, the gate electrode was made out of degenerately doped polycrystalline silicon (poly-Si). This is stable at high temperatures and compatible with SiO_2. Poly-Si is a reasonable metal, but it is not a good enough metal as its relatively low carrier density gives a depletion depth of a few Å. In contrast, a good metal has a much higher carrier density and a depletion depth of only 0.5 Å. This depletion effect is removed by replacing poly-Si with a normal metal. The effect on ECT of the replacement of SiO_2 by a high K oxide and poly-Si gate electrode by a metal is shown schematically in Fig. 5. As noted below, the work function of the metal is a critical property to enable proper NMOS or PMOS FET operation.

The ECT is the only thickness that can be measured directly, by capacitance-voltage (CV) methods. On the other hand, EOT can only be estimated by, for example, electron microscopy measurements of oxide thickness, or by back calculating from ECT. EOT is useful, but is not a direct electrical parameter.

A metal gate material must also be carefully chosen. It is chosen primarily for its work function and its thermal robustness, as discussed in detail in section 6.

2 Choice of High K oxide

Silicon dioxide is the main reason that microelectronics uses Si technology and not another semiconductor. As a semiconductor, Si has average performance, but in most respects SiO_2 is an excellent insulator. SiO_2 has the key advantage that it can be made from Si simply by thermal oxidation, whereas every other semiconductor (Ge, GaAs, GaN, SiC…) has a poor native oxide or poor interface with its oxide. SiO_2 is amorphous, has very few electronic defects and forms an excellent, abrupt interface with Si. (The abruptness of the interface is seen by the absence of intermediate valence states in the Si photoemission core spectra.) SiO_2 can be etched and patterned to a nanometer scale. Its only problem is that it is possible to tunnel across it when very thin. Hence, we must loose these advantages of SiO_2 and start to use a new high K oxide. We can in principle choose it from a large part of the Periodic Table.

The requirements of a new oxide are six-fold [2,5,9];

1. Its K value must be high enough to use economically for a reasonable number of scaling nodes.
2. The oxide is in very close contact to the Si channel, so it must be thermodynamically stable with it.
3. It must act as an insulator, by having band offsets with Si of over 1 eV to minimise carrier injection into its bands [20]
4. It must be kinetically stable, and able to be processed at 1000^0C for 5 seconds (in gate first flow).
5. It must form a good electrical interface with Si.
6. It must have few electrically active defects.

Interestingly, once SiO_2 is replaced as the dielectric, a key performance advantage of Si is lost, so other semiconductors such as Ge or III-Vs can now be considered for use as the channel. Silicon continues to provide very useful mechanical properties however, and such properties must be considered in the course of fabrication with automatic-loading tools. Other semiconductors are less abundant and have poor (brittle) mechanical properties. Moreover, as the industry is tooled for large area Si wafers with diameters expected to be at least 450mm in the next decade, it will remain a dominant material for integrated circuit manufacturing in all aspects until the end of the technology roadmap.

2.1 K value

The first key requirement is that the oxide's K value should be over 12, preferably 25-35. There is a trade-off between K value and the band-offset condition, which requires a reasonably large band gap. Table 1 and Fig. 6 shows that an oxide's K value tends to vary inversely with its band gap, so we must accept a relatively low K value [20]. There are numerous oxides with very large K, such as Ta_2O_5 or $SrTiO_3$, which were candidates for DRAM capacitor dielectrics, but their band gaps are too small.

The static dielectric constant is the sum of the electronic and lattice contributions, $\kappa = \kappa_e + \kappa_{lattice}$. The electronic component κ_e is also the optical dielectric constant ε_∞ and it equals the square of the refractive index, n - $\kappa_e = \varepsilon_\infty = n^2$. ε_∞ values are typically in the range 4-5 for the wide gap oxides of interest. Thus they are *not* the main source of the high K. The large static dielectric constant arises from the lattice contribution,

$$\kappa - n^2 = \sum \frac{Ne^2 Z^{*2}_T}{m\omega_{TO}^2} \tag{5}$$

Here, N is the number of ions per unit volume, e is the electronic charge, Z_T* is the ion's transverse effective charge, m is the reduced ion mass, ω_{TO} is the frequency of the transverse optical phonon

and the sum is over the ions. Large values of κ_l occur when Z* is large and/or the frequency of a polar optical mode ω_{TO} is small. It often arises in materials that are incipient ferroelectrics.

2.2 Thermodynamic Stability

The second requirement arises from the condition that the oxide must not react with Si to form either SiO_2 or a silicide by the reactions,

$$MO_2 + Si = M + SiO_2 \quad (6)$$

$$MO_2 + 2\ Si = MSi + SiO_2 \quad (7)$$

This is because any SiO_2 layer increases the EOT and negates the effect of the new oxide, while silicides formed by (7) are metallic and would short circuit the channel.

This condition requires that the oxide have a higher heat of formation (per O atom) than SiO_2 itself as noted by Hubbard and Schlom [21] and Schlom and Haeni [22] found that this restricts choices to very few oxides, from columns II, III and IV of the Periodic Table. These oxides are SrO, CaO, BaO, Al_2O_3, ZrO_2, HfO_2, Y_2O_3, La_2O_3 and the lanthanides. It excludes some otherwise useful oxides such as Ta_2O_5, TiO_2 and the titanates $SrTiO_3$ and $BaTiO_3$. The group II oxides SrO etc are less useful as they have rather low K values. Hence this leaves us with Al_2O_3, ZrO_2, HfO_2, Y_2O_3, La_2O_3, Sc_2O_3 and some lanthanides such as Pr_2O_3, Gd_2O_3 and Lu_2O_3.

Zr and Hf are both from column IV and are generally believed to be two very similar elements. However, it was subsequently found that ZrO_2 is slightly more reactive with Si [23,24] and can form the silicide, $ZrSi_2$. An example is shown in Fig. 7. For this reason, HfO_2 was preferred over ZrO_2, particulary for the higher thermal budget gate-last case.

Of the other binaries, La_2O_3 has a slightly higher K than HfO_2, but is hygroscopic. Al_2O_3 has a rather low K value and high defect density. Y_2O_3 and Lu_2O_3 have a lower K than La_2O_3. The other lanthanides Pr_2O_3, Gd_2O_3 etc are comparable to La [25-28] but have no particular advantage.

The interface between HfO_2 and the Si substrate has undergone considerable scrutiny in the last decade. Thermodynamically, one anticipates HfO_2 to be stable on direct contact with Si, but kinetic effects can alter the interface, potentially resulting in a compositionally graded interface somewhat representative of a silicate [2,29]. The composition of such an interface has spawned some controversy over the years, with some workers indicating that the interface after HfO_2 deposition is purely SiO_2, [30-34] while others indicating the presence of significant amounts of Hf near at the interface [35-38], depending upon the deposition and thermal treatment details.

2.3 Band offsets

The high K oxide must act as an insulator. This requires that the potential barrier at each band must be over 1 eV in order to inhibit conduction by the Schottky emission of electrons or holes into the oxide bands [20,39], as shown in Fig 8. SiO_2 has a wide gap of 9 eV, so it has large barriers for both electrons and holes. However, for oxides with a narrower band gap like $SrTiO_3$ (3.3 eV), their bands must be aligned almost symmetrically with respect to those of Si for both barriers to be over 1 eV. In practice, the conduction band offset is smaller than the valence band offset. This limits the choice of oxide to those with band gaps over 5 eV. The oxides that satisfy this criterion are Al_2O_3, ZrO_2, HfO_2, Y_2O_3 La_2O_3 and various lanthanides, and their silicates and aluminates [20]. It is interesting that these are the *same* oxides that pass the thermal stability criterion. This is because a high heat of formation correlates with a wide band gap. On the other hand, the conduction band offset of $SrTiO_3$ is essentially zero [20,40], so this oxide is unsuitable.

The early leakage current data for various high K oxides are plotted as a function of EOT in Fig. 8 for typical high K oxides, HfO_2 from [17], for ZrO_2 from Gusev et al [41], for Al_2O_3 of Gusev [17] and Guha [42,43], for La_2O_3 from Iwai [26] and data for HfO_2 films with poly-Si electrodes and HfO_2 with TiN electrodes, from Tsai [44].

Device scaling will require the use of ever-smaller EOTs. Yeo [45] defined a Figure of Merit, *k*, for direct tunnelling, which combines the barrier height ϕ, tunnelling mass m* and dielectric constant K,

$$J = J_0 \exp(-2k.t)$$

$$k = (2m^*\phi)^{1/2} (K/3.9) \qquad (8)$$

where *t* is the EOT. Lanthanides have the lowest leakage in Fig 9 and the highest figure of merit because they have the largest conduction band (CB) offset. Hf alloys are presently preferred because lanthanides are hygroscopic and because they give low gate threshold voltages for both FET polarities, nFET and pFET.

2.4 Kinetic Stability

The fourth condition is kinetic stability, that in a gate-first process the oxide must withstand the dopant activation anneal for 5 secs at 1000^0C. We must choose to use a crystalline or amorphous oxide. If an amorphous oxide is desired, this is a strenuous condition as most high K oxides are not good glass formers, unlike SiO_2. In particular, HfO_2 and ZrO_2 crystallise at lower temperatures (400C) and, would be nano-crystalline in use.

The crystallisation problem can be circumvented by alloying the oxide with a glass former – SiO_2 or Al_2O_3 – giving either a silicate or an aluminate [29,46]. This retains a stability against crystallisation up to nearly 1000^0C. However, silicates have significantly smaller K values. The addition of nitrogen is beneficial as it further lowers diffusion rates and raises crystallisation temperatures, so that Hf silicates can then pass this criterion [47].

The arguments against poly-crystalline oxides are that its grain boundaries might cause higher leakage currents, act as dopant diffusion paths, and lead to fluctuating K values from grain to grain. On the other hand, Lee [48] and Kim [49] found that leakage currents of amorphous and nanocrystalline HfO_2 are similar, so there was no specific conduction along grain boundaries.

There have been extensive measurements of the atomic diffusion rates of Hf, O, B and P in HfO_2 and Hf silicate by secondary ion mass spectroscopy (SIMS), Medium Energy Ion Scattering (MEIS) and nuclear reaction profiling [50-55]. The addiotn of nitrgoen to HfO_2 or Hf silicate is also very effective in reducing diffusion rates and also increasing crystallisation temperatures. Nitrogen has other benefits on the electrical properties that are covered in section 5.3.

2.4 Interface Quality and Defects

The high electrical quality of the $Si:SiO_2$ interface was the key advantage of Si as a semiconductor. The interface is essentially atomically abrupt with few sites with intermediate valence; the Si atoms are either in Si or in SiO_2 as seen by XPS core level spectra [56,57]. The interface roughness consists of atomic steps spaced apart by 20 nm in the highest quality oxide.

The electrical quality of the Si : high K interface must be of the highest quality in terms of roughness and absence of defects in order to avoid scattering cariers. Electrically active defects are defined as atomic configurations which give rise to electronic states in the oxide band gap which can trap carriers. Typically, these are sites of excess or deficit of oxygen or impurities. They can be at the interface or in the oxide layer.

Defects are undesirable for four reasons. Firstly, charges trapped in defects shift the gate threshold voltage of the transistor, V_T, the voltage at which it turns on. Secondly, the trapped charge changes with

time so V_T shifts with time, leading to instability of operating characteristics. Thirdly, trapped charge scatters carriers in the channel and lowers the carrier mobility. Fourthly, defects cause unreliability; they are the starting point for electrical failure and oxide breakdown.

SiO_2 is an almost ideal insulating oxide, having a low concentration of defects which give rise to states in the gap. This is fundamentally because of its low coordination number, so that its bonding can relax and re-bond any broken bonds at possible defect sites. Most of the remaining defects are readily passivated by hydrogen, as seen in electron spin resonance [58-61].

The high K oxides differ from SiO_2 in that they are not intrinsically low defect density materials. Whereas SiO_2 has a random network which can relax to heal defect sites, HfO_2 and ZrO_2 come from a family of fast ion conductors, with potentially large O vacancy concentrations. Hence, much of present-day engineering consists of pragmatic strategies to reduce oxide defect densities by process control and annealing.

On the other hand, the interface between Si and the high K oxide always has an SiO_2-rich interfacial layer, it is not an abrupt interface. This allows lower interfacial defect densities to exist in practice. However, after 6 years of further scaling, EOT is reaching values below 0.7 nm, and near-abrupt interfaces are close to being used.

2.5 Metal gate vs poly-silicon gate

While the effective capacitance thickness (eqn 4) indicated that scaling would eventually require the replacement of SiO_2 by a high K oxide, and of the poly-Si gate by a metal gate, it was expected that the two technological changes could occur separately. However, it became clear that there was a reaction between Si and high K oxide. It was found that the reducing ambient during the CVD deposition poly-Si from silane causes a gross reduction of the ZrO_2 or HfO_2, leading to silicide formation [23,62,63], as in Fig 7. It was realised that high K gate oxides and metal gates must be introduced simultaneously.

The second factor was 'Fermi level pinning' which will be described later, and was initially attributed to the formation of Hf-Si bonds at the HfO_2 /poly-Si gate interface [64-66]. Thus, it was decided to introduce high K oxies and metal gate simultaneously [1].

2.6 Gate First/Gate Last Process

The interface between the gate electrode and the gate oxide is at least as critical to the FET performance as that between channel and the oxide. This interface sets the gate threshold voltage V_t, the turn-on voltage of the FET. Whereas the poly-Si gate electrode is refractory and compatible with SiO_2, the atoms in HfO_2 diffuse much more easily and reactions with metal gates occur at lower temperatures. The details are covered later, but the realisation that such reactions will make the V_t very difficult to control led to the decision to develop a 'gate last' process.

The gate first process (Fig 10a) follows the same process flow as with a SiO_2 gate oxide [62]. In gate first, we sequentially deposit a gate oxide layer, gate work function tuning layer, and gate metal. The source and drain doping implants are carried out, and the dopant activation anneal to 1000C is carried out. This annealling temperature is too high for many gate stacks.

In the gate last process, (Fig 10b), the gate oxide is deposited followed by a poly-Si dummy gate [15,67]. The source drain dopant implants are carried out, followed by the dopant activation anneal. An interlayer dielectric is deposited for mechanical stability. This is then planarised by chemical mechanical polishing (CMP) down to the level of the top of the dummy gate. The dummy gate is then etched out, and the metal gate layers are then deposited into this hole, followed by an Al fill. An anneal to 500C is applied. In this way, the gate metal is not exposed to the 1000C temperature anneal.

Variant 2 of the gate-last process etches off both the dummy gate and a 'dummy gate oxide', and replaces both with new gate oxide and gate metal.

3 Materials Chemistry of high K oxides

3.1 Atomic Layer Deposition

The great advantage of SiO_2 was that it can be grown by high temnperature thermal oxidation of the Si substrate. In contrast, high K oxides must be deposited. Previously, deposited oxides were never as good as SiO_2 thermal oxides, but they now have sufficient reliability to be used in transistor technology.

Several deposition methods have been employed in researching high-k dielectrics [68-70]. Sputtering is a physical vapour deposition (PVD) method. Its advantage is that it is broadly available and can produce pure oxides. A disadvantage is that oxides are insulators, so that sputtered oxides will have plasma-induced damage. Also, PVD is line of sight, so it does not give good conformal coverage. A first metal layer can be used to limit the interfacial layer formation and stop over-oxidation. Sputtered films are often used to initially examine dielectric properties prior to further work using CVD or ALD techniques as specialized precurosors are not required.

Another method to produce high purity thin oxides is to deposit metal by electron beam evaporation, which is controllable to small thickness, and then oxidise the metal by ozone or UV assisted oxidation. The advantage is that this produces less damage than oxide sputtering. Ideally, the oxygen partial pressure should be controlled to oxidise just the metal, but not the Si [71,72].

The preferred methods are chemical vapour deposition (CVD) and atomic layer deposition (ALD). CVD uses a volatile metal compound as a precursor, which is introduced into the chamber and oxidised during deposition onto the substrate. The advantages of CVD are that it is already widely used in the electronics industry for insulator deposition, it gives conformal coverage over complex shapes, and the growth rate is controllable. The conformality property is particularly valuable, as it allows deposition even on complex geometries such as the FinFET.

The most preferred deposition method is ALD. It is a method of cyclic deposition and oxidation [73-76]. It was first developed to produce conformal, pin-hole free insulating films for electro-luminescent displays. Fig 11 shows the chemical reactions schematically for the precursor $ZrCl_4$. The surface is exposed to the precursor $ZrCl_4$, which is absorbed as a saturated monolayer. The excess precursor is then purged from the chamber by an Ar or nitrogen pulse. A pulse of oxidant such as H_2O, H_2O_2 or ozone is then introduced which fully oxidises the adsorbed precursor layer into MO_2 and a volatile by-product such as HCl. The excess oxidant is then purged by another Ar pulse, and the cycle is repeated.

The effective chemical reactions are

$$ZrCl_4 + 2\ OH_{surface} = ZrCl_2O_2 + 2\ HCl \quad (9)$$

$$ZrCl_2O_2 + 2\ H_2O = ZrO_2(OH)_{2\ surface} + 2\ HCl \quad (10)$$

The existing ZrO_2 surface is assumed to be terminated by OH groups at about 300^0C. The $ZrCl_4$ chemisorbs exothermically onto the OH sites by the exothermic elimination of HCl to form $ZrCl_2O_2$. In the second stage, water reacts with $ZrCl_2O_2$ so that Cl atoms are eliminated via formation of HCl, leaving a layer of ZrO_2 on the surface. It is noted that such precursors are C-free, which may improve insulator properties and reliability.

Each cycle of ALD adds a layer of oxide, which is usually much less than an atomic layer thick, despite its name. The precursor absorption saturates at less than one monolayer because of steric hindrance. This is not a significant disadvantage, it just takes more cycles to grow a certain thickness.

The precursor is designed so that both steps of absorption and oxidation are exothermic. The precursor must undergo self-limiting adsorption, be volatile, high purity, non-toxic, have no gas phase reactions, no self-decomposition, and no etching of the existing oxide. The first precursors for ZrO_2 and HfO_2 were their chlorides. However, these have a low volatility and tended to clog. They are preferred by industry as they avoid carbon impurities, and industry can handle the corrosive exhaust gases.

A wide range of organic ALD precursors has now been developed to allow high volatility and less corrosive exhausts [73-76]

The main advantage of ALD is that it can grow the thinnest films of any method, and the most conformal films for step coverage or into deep trenches (Fig 12), but the growth rate is very low. Furthermore, a disadvantage of ALD and MOCVD is that they can introduce impurities such as C, H or Cl into the oxides, depending on the precursor. Post-deposition annealing is needed to densify ALD oxides and remove the impurities.

An early problem with ALD was nucleation. The most inert surface of Si is the H-terminated surface formed by HF-last cleaning. It was found that ALD using $HfCl_4$ or many organic precursors did not nucleate properly on HF-last Si surfaces [77,78]. This meant that oxide films even 3 ML thick were not fully 'closed' but islanded. Nucleation occurred more readily on a slightly pre-oxidised Si surface. Thus, ALD was carried out on a 'chemical oxide' (SiO_2) surface formed by ozone or oxidative cleaning of Si. The nucleation problems on Si-H terminated surfaces were removed by using more sophisticated precursors [79,80].

The various types of ALD precursor are listed in Table 2. The precursors are designed to have the desired volatility, reactivity and stability [73-76,81-84]. The molecules are formed by adding organic ligands. The ligands create the volatility. Volatility is aided by using monomer ligands, which do not pack so easily in the solid state. The metal valence is satisfied by polar bonds from N or O atoms. These bonds define the stability and reactivity.

The alkoxides and diketonates are commercially available oxygen containing precursors, of reasonable reactivity. The nitrogen-based ligands are becoming more favoured. It turns out that amido compounds have the desired reactivity to give ALD on oxide surfacers and also to nucleate on Si-H terminated surfaces. Beta-diketonates are useful for lanthanide oxides. ALD can also produce metal nitrides for electrodes or diffusion barriers [83].

Ho et al [35] followed the progress of the ALD deposition of HfO_2 films over a number of ALD cycles by FTIR, see Fig 13. The film was grown from tetrakis ethyl- methyl amino hafnium (TEMAH) or $Hf(N(CH_3).(C_2H_5))_4$ at 100C with water as oxidant on an H terminated Si surface. First, the infra-red spectrum showed that there is an abrupt interface during growth, with Hf-O-Si bonds gradually replacing Si-H bonds. The HfO_2 growth progress can be seen from the Hf-O modes. The continuing presence of Si-H shows that there is still some island growth even after growing 3 ML of oxide. A separate broadened and red-shifted Si-H mode occurs as the Si-H group becomes surrounded by HfO_2. The reaction of the precursor, not the oxidant, is thus crucial.

The film was then subjected to thermal annealing. The film had O-D modes (D=deuterium) from the D_2O oxidant. The post-deposition anneal is used to densify the film and remove contaminants such as organics, water, etc. It is found that at 400-500C, the O-H modes disappear and Si-O modes appear. An interfacial SiO_2 layer 0.9 nm thick has grown. It turns out that ALD leaves an oxygen-rich film. When the oxidant is water, the film contains –OH groups. Annealing should evolve these as H_2O molecules. However, as the film densifies, H_2O molecules are too large to escape. It is only possible for H to diffuse either as H^+ ions or H_2 molecules, desorbing as H_2. Further annealing to higher temperatures expels the excess oxygen, and this creates the interfacial SiO_2 layer by oxidising the underlying Si. There is no interfacial layer *during* growth itself.

Recent advances in ALD have been the ability to deposit $LaAlO_3$ using tris(N,N0-diisopropylformamidinate)–lanthanum and trimethyl aluminium and the epitaxial growth of oxides on Ge and III-Vs [84].

3.2 Alloy Crystallisation

Silicate and aluminate alloys of Zr, Hf and La oxides are often used instead of the pure metal oxides due to their higher resistance to crystallisation [29,53,85]. For Zr silicate, crystallisation directly to the crystalline $ZrSiO_4$ is inhibited by kinetics. Instead, crystallisation occurs by a phase separation into ZrO_2

and SiO_2 phases, followed by a crystallisation of the ZrO_2 component [86]. This can be seen for HfO_2-SiO_2 alloys in the high-resolution transmission electron microscope images in Fig 14 for two different compositions from Stemmer [87].

The phase diagram of the ZrO_2-SiO_2 system is reasonably well known [88], Fig 15(a). That of HfO_2-SiO_2 is similar. The key factor is that ZrO_2 and SiO_2 liquids are immiscible over a range of composition due to the large ionic charge of Zr. This 'miscibility gap' can be extrapolated to lower temperatures to define a solid phase miscibility gap. It also defines a spinodal region in which the alloy will spontaneously phase separate to lower its free energy [88]. The glass transition temperature is also marked in Fig 15(a). Thus, Zr silicates crystallise by two mechanisms. For 20-60mol% Zr, silicates crystallise by spinodal decomposition followed by crystallisation. This leads to small grain sizes. Silicates with over 60% Zr crystallise by the kinetically limited nucleation and growth of crystalline ZrO_2. This was confirmed by extensive TEM and x-ray scattering on Hf silicates by Stemmer [89].

The La silicate phase diagram in Fig 15b) [86,90] is somewhat similar to that of $ZrSiO_4$ except that the two-phase region is further towards SiO_2. The main difference is that La_2O_3 forms a much more stable silicate, whereas Hf or Zr silicates prefer to phase separate into the parent oxides.

3.4 The interfacial layer

An interfacial layer of SiO_2 or silicate usually exists between the Si channel and the high K oxide layer. Fig. 16 shows a cross-sectional of an example [91]. There are advantages and disadvantages to this interfacial layer, as long as its presence and thickness can be controlled. The overall EOT of a layer 1 of SiO_2 and a layer 2 of high K oxide is given by the series capacitance formula,

$$1/C = 1/C_1 + 1/C_2 \tag{11}$$

which becomes

$$EOT = t_{SiO2} + EOT_{hiK} \tag{12}$$

Thus, an extra SiO_2 layer is undesirable as it increases the total EOT. In fact, the K of SiO_2 (3.9) is so small that an SiO_2 layer will rapidly use up the EOT allocation. It is a severe limitation to scaling of EOT below 1.0 nm.

The SiO_2 layer does not arise from the direct reaction of HfO_2 with Si. It arises from the diffusion of O through the HfO_2 layer to oxidise the Si underneath. The SiO_2 layer usually grows during the post-deposition annealing stage, not during growth [92]. It can arise for ALD oxide, because the oxide is initially O-rich and it looses oxygen to oxidise the underlying Si [35]. It can also occur due to oxygen permeation through the top electrode, if the gate material is porous to oxygen.

There was great advantage in retaining the SiO_2 intelayer in the early development of high K gate stacks, because then the Si interface is still between Si and SiO_2, and it retains the low defect density and relatively high reliability of this interface [88].

The second reason a SiO_2 layer exists is intentional, for beneficial reasons. For example, a 'chemical oxide' acts as a nucleation layer for ALD growth of HfO_2 [79,80]. The SiO_2 layer is also introduced to improve the overall electrical quality of the Si-oxide interface, see section 7. The Si-SiO_2 interface is well understood and can be processed to be high quality. In principle, it can be made with a very low defect concentration, by annealing. A SiO_2 layer spaces the Si channel from the high K oxide, which can lessen mobility degradation due remote scattering.

3.5 Metal Inserted Poly-Silicon gates

A number of metals used as gate metals such as W contain oxygen or allow O diffusion. To stop the metal being a source of oxygen, the gate-first process uses a 'metal inserted poly-Si' (MIPS) gate

electrode, which is a thin layer of the metal underneath the poly-Si capping layer, in which the Si acts as a diffusion barrier to oxygen [10].

3.6 Oxygen Scavenging

The continued scaling of EOT below 1.0 nm and towards 0.5 nm requires us to either reduce the thickness of the interfacial layer, or increase the K values. In 2006-2010 there was considerable work towards developing 'higher K' oxides than HfO_2, as described in section 4.3. However, Ando et al [93] pointed out that the contribution of the SiO_2 based interlayer to EOT is so large than higher K would have little effect. Ando et al [93-97] then tried the idea of increasing the K of the interlayer, for example by alloying it with lanthanides. However, there are disadvantages to adding La, as it affects the gate threshold voltage.

It was decided to reduce the interfacial SiO_2 layer thickness. The SiO_2 can be thinned down by an 'oxide scavenging' process, by placing an oxygen scavenging metal layer such as Ti or Hf above the HfO_2 to 'suck' out the O through the HfO_2 by annealing [98-102]. The scavenger metal should have an oxide heat of formation per O atom than is greater than that of SiO_2 (Fig 11). Ando [95] and Frank et al [96] have carried out extensive work on this process. This is described in more detail in section 7.3.

4 Bonding and electronic structure

4.1 Nature of Bonding in high K oxides

The high K oxides of interest, except for Al_2O_3, are closed shell transition metal oxides [103,104]. Al_2O_3 is an s,p bonded oxide. Fig 17(a,b) show the density of states (DOS) anmd screened exchange band structure of corundum Al_2O_3 the most stable crystalline phase. The top of the valence band lies at 0 eV and the band gap lies from 0 to 8.8 eV [105]. The bonding in Al_2O_3 is more ionic than in SiO_2, and its atoms have ionic coordinations of 6 for Al and 4 for O. However, its electronic DOS does resemble that of SiO_2. Its valence band consists mainly of O p states and a conduction band of mainly Al s,p states.

The actual phase of Al_2O_3 used in gate stacks is amorphous, with lower mass density and a lower coordination of ~4.5 for Al and 3 for O [106,107]. This reduces the band gap of the Al_2O_3 to about 6.2 – 6.6 eV [108]. It is possible to model the amorphous phase with one of the lower density, lower symmetry phases such as θ- Al_2O_3 whose band structure is shown in Fig 17(c) [109].

The other high K oxides are closed shell (fully ionised) transition metal oxides. While many transition metal oxides are notable for their mixed valence, here we only deal with fully ionised metal ions. This means the oxides are wide band gap, and do not suffer from the correlation effects.

The most important high K oxide is HfO_2. HfO_2, like ZrO_2, has three phases, cubic, tetragonal and monoclinic [110,111]. The different metal coordinations of these phases are shown in Fig. 18. For large grain sizes, monoclinic is the most stable phase, and cubic the least stable phase. Fig. 19 shows the band structure of cubic HfO_2 and the partial density of states (PDOS) [103]. This phase has an indirect band gap with a maximum at X formed from O p states. The conduction band minimum is a Γ_{12} state of Hf 5d orbitals. The valence band is 6 eV wide. The conduction band PDOS is split by the crystal field field into a lower band of e states and an upper band of t_2 states 5 eV higher.

The electronic structure of the ZrO_2 phases is very similar to that of HfO_2 except that the crystal splitting of the Zr 4d states in the conduction band is smaller than in ZrO_2 (Fig 20) [103].

TiO_2 is another group IV oxide which has various structures including rutile. Its gap is much narrower than that of HfO_2 or ZrO_2 at about 3.3 eV [112].

Crystalline La_2O_3, has a hexagonal structure in which La is 7-fold coordinated, with 4 short bonds and 3 longer bonds. The DOS of La_2O_3 in Fig. 21 shows that the valence band is strongly localised on the O p states and the conduction band is on La d states with some La s,p states starting at 8 eV [103]. The band gap is indirect and 6 eV. The valence band is now only 3.5 eV wide, narrower than for ZrO_2. The ionicity is higher than in ZrO_2.

Of the other group IIIA metal oxides, Y_2O_3 has the cubic bixbyite (defect spinel) structure. This has a large 56 atom unit cell in which there are two types of Y sites, both 7-fold coordinated. This structure occurs because Y has a smaller ionic radius than La. The band gap of Y_2O_3 is direct and is about 6 eV. The valence band is again only 3 eV wide. The partial DOS shows the valence band is largely O p states. The conduction band minimum has mixed Y d,s character. The other lanthanides adopt either the La_2O_3 or bixbyite structure.

In all these transition metal oxides, the conduction band minimum at Γ lies at the metal d energy, while the top of the valence band are non-bonding O 2p states lying at the O 2p energy. Thus the band gap is a pure ionic gap between O 2p and metal d states. The band gap is proportional to the metal atomic d orbital energy [1113].

$ZrSiO_4$ is typical of the transition metal silicates. Crystalline $ZrSiO_4$ (zircon) has the body-centred tetragonal structure. Each Zr atom has eight O neighbours. Each Si has four O neighbours in a tetrahedral arrangement, and each O has three neighbours, two Hf and one Si. These coordinations may carry over to the amorphous phases and amorphous alloys. Its partial DOS is shown in Fig 22. The band gap is about 6.5 eV [103]. The valence band is about 7 eV wide [114-116]. The conduction bands form two blocks. The lower conduction band is due to Zr d states and lies between 6.5 eV and 8 eV, and a second conduction band due to Si-O antibonding states lie above 9 eV.

The extended x-ray fine structure spectrum [117] suggest that the coordinations in Zr silicate alloys do not follow the zircon structure, but are locally more like in pure ZrO_2 or pure SiO_2. This implies local phase separation as noted by Pignedoli [118].

It is an important general rule that the conduction band of Zr silicates forms two non-mixing ZrO_2-like and SiO_2-like bands. The states do not mix because the Si s,p states and metal d states have different local symmetry. Thus, the CB minimum of the silicates has a Zr d character as long as Zr is present, and the band gap increases only slowly, with very strong bowing below the virtual crystal model. Experiments by Kato [119] confirm this.

Another large class of possible gate oxides are the perovskites like $SrTiO_3$. In the ABO_3 structure, the smaller transition metal ion occupies the B site which is octahedrally coordinated by six oxygens. The oxygens are bound to two B ions, while the A ion is surrounded by twelve oxygen ions. The band gap of $SrTiO_3$ is direct and 3.3 eV wide. Due to this small gap, $SrTiO_3$ itself is not useful as a gate oxide.

There has recently been considerable work on other perovskites with larger band gap. $LaAlO_3$ was the first. It is important because it has a large dielectric constant, and a close lattice match to Si. It is unusual in that the transition metal La occupies the A site and Al occupies the octahedral B site. The partial DOS of $LaAlO_3$ is shown in Fig. 23 [120]. The band gap is 5.6eV from the spectroscopic ellipsometry of Lim [121]. However, the problem with $LaAlO_3$ is that it looses some of its high K property when it becomes amorphous.

Following this, numerous combinations of rare earths at A and B sites were tried, such as $DyScO_3$ and $LaLuO_3$. They all have band gaps of about 5.6 eV, and have quite high dielectric constants, usually above 25 [122]. Fig. 24 shows the PDOS of $LaLuO_3$ which includes the filled Lu 4f states in the valence band.

The other type of perovskite is $SrHfO_3$. This retains the simple 2-4 valence of $SrTiO_3$, but is more useful because it has a band gap of 6.0 eV due to the Hf [123].

These various band structures above have been calculated using the local density approximation (LDA) in the generalised gradient approximation (GGA). The LDA under-estimates the band gap of semiconductors and insulators. Many calculations have since used more advanced methods such as hybrid functionals (HSE or screened exchange) [124-127], or by the GW approximation [128,129]. These give calculated band gaps close to the experimental values.

The high K oxides all have a very large heat of formation, they are very exothermic oxides. This is seen if we plot theoxide's heat of formation against the work function of the parent metal, as in Fig 25. The oxide heat of formation is equivalent to the Ellingham diagram at 0^0K. The metal work function is related to the Pauling electronegativity of the metal. It is interesting that there is a rough linear correlation of the heat of formation with the work function, until the heat of formation tends to saturate at large work functions.

4.2 Dielectric constants

As noted in section 2.1, the high value of dielectric constant arises from the lattice contribution to K, whereas the electronic contribution to K is relatively minor. Thus high K oxides are incipent ferroelectrics. Any desire to increase K must target the lattice contribution.

The dielectric constants have been calculated in the LDA for the various phases of HfO_2 and ZrO_2 [130,131]. This allows us to understand the differences and the anisotropies. Rignanese [131] found that the tetragonal phase has the largest and most anisotropic K, but not by as much as found by Zhao and Vanderbilt [130]. These calculations were extended to lanthanides such as Lu_2O_3 [126].

4.3 Higher K and Phase control

The continued scaling of MOSFETs contains high k oxides would appear to require the development of higher K oxides [133,122,145-153]. High K oxides are incipient ferroelectrics. Nevertheless, amorphousness is incompatible with ferroelectricity, as this requires ordered ionic displacements. Thus, huge K values are unlikely.

On the other hand, Shannon [134] observed that ionic polarisabilities were additive, not just the electronic part which might be expected from bonding arguments, but even the ionic part. Thus the K value varies with the ionic density of the oxides, and the component ions.

Amorphous HfO_2 has a lower K value than cubic HfO_2, as has monoclinic HfO_2, as both have a lower density than cubic HfO_2. On the other hand tetragonal HfO_2 has a higher K value than cubic HfO_2, because of its lower frequency polar lattice modes. There has recently been interest in stabilising these higher K phases.

The first method is to use the ability of Zr itself to stabilise its tetragonal phase, and when alloyed with HfO_2, as seen by [135-137]. The second method is to dope the oxide with a smaller diameter group IV element such as Si or Ge [138,139]. The key point is that group IV dopants stabilise the tetragonal phase over the monoclinic or cubic phase, while the group III elements like Y stabilise the cubic phase, as used in ceramics and jewelry [140-144]. A doping content of 2-7% is needed.

Many higher K oxides were synthesied by adding rare earths to the perovskites [145-154]. The important aspect of these oxides is that they combine a higher K value with a large conduction band offset, so their overall figure of merit (eqn 7) is high. $LaLuO_3$ is unusual because it maintains its high K value even in its amorphous phase [122,147,149], unlike $LaAlO_3$. These metals are from opposite ends of the lanthanide series and have quite different ionic radii, La is large, Lu is smaller. Fig. 21 shows its density of states [147]. Because of the different ionic radii, $LaLuO_3$ remains amorphous up to about 900C. This makes it one of the most interesting higher K oxides [147,148]. However, as noted in section 3.6, ultimately the higher K route to scaling is unsuccessful, reducing the interlayer thickenss by scavenging is recognised to be the most promising method.

This brings us to the last aspect of phase control. In the same way that the tetragonal phase has the highest K of the HfO_2 phases, the hexagonal phase of trivalent oxides like La_2O_3 has a much higher K than its bixbyite (cubic) phase [155,156].

4.4 Band Offsets

The band offset between the oxide and Si defines the barrier for injection of electrons or holes into the oxide bands, Fig 26. The conduction band (CB) offset tends to be the smaller of the two. The CB offset is one of the key criteria in the selection of a gate oxide. It must be over 1 eV to give adequately low leakage current [20]. The band offset is measured by methods such as photoemission.

This band alignment at an interface is controlled by any dipole formed by charge transfer across the bonds at the interface. For two non-interacting surfaces, there is no charge transfer, no dipole, and the conduction band line up is given by the difference between the two electron affinities (the energy of the

conduction band edge below the vacuum level) (Fig 26) [20]. This is called the Schottky limit. If the surfaces interact, charge transfer occurs across the interface, and the resulting interface dipole modifies this offset. The charge transfer acts to align a reference energy level in each surface. In the limit of strong coupling, known as the Bardeen limit, these levels are fully aligned. The band offset is then given by the difference of this reference energy level below the two conduction bands, and is independent of the vacuum levels.

The band line up at an interface is controlled by a dipole formed by charge transfer across the interface bonds [157-159]. The dipole consists of two components, a component intrinsic to the bulk oxide and a component that depends on the interface chemical bonding. The intrinsic component is of interest because the specific bonding at the interface is usually not known.

We first consider the intrinsic band offset. First, the oxide-semiconductor interface is just a variant of the interface between two semiconductors, with the oxie treated as a wide bandgap semiconductor. Second, a semiconductor-semiconductor interfaces is treated as a special case of a semiconductor-metal interface (which is known as a Schottky barrier). A particular model of dipoles at a metal-semiconductor interface is the metal induced gap states (MIGS) model [160-162,20]. This model says that in the energy range of the semiconductor band gap, the travelling wave states of a metal decay into the semiconductor as evanescent states called MIGS, Fig 27(a). These states are filled up to some cutoff energy called the charge neutrality level (CNL). In general, the work function of the metal does not equal the CNL energy of the semiconductor, so that when the two systems come into contact, there is a charge transfer between the two which creates an interface dipole. This dipole now tries to align the semiconductor's CNL with the metal Fermi level. The Schottky barrier height, the energy of the semiconductor conduction band above the metal Fermi level, is then given by

$$\phi_n = S(\Phi_M - \Phi_S) + (\Phi_S - \chi_s) \tag{13}$$

where Φ_M is the metal work function, Φ_S is the charge neutrality level of the semiconductor measured from the vacuum level, and χ_S is the electron affinity (EA) of the semiconductor. S is a dimensionless pinning factor given by $S=d\phi_n/d\Phi_M$ which defines how strongly the MIGS can force this alignment. S is given in the linear approximation by [163]

$$S = \frac{1}{1 + \frac{e^2 N\delta}{\varepsilon\,\varepsilon_0}} \tag{14}$$

where e is the electronic charge, ε_0 is the permittivity of free space, N is the density of the interface states per unit area and δ is their extent into the semiconductor. Strong alignment or pinning corresponds to S=0, while no pinning corresponds to S=0. Large values of N and δ give strong pinning.

Monch [160] found empirically that S in (14) varied with the electronic dielectric constant ε_∞ of the semiconductor as

$$S = \frac{1}{1 + 0.1(\varepsilon_\infty - 1)^2} \tag{15}$$

This is an empirical rule, in addition to the basic MIGS model.

The MIGS model is then extended to describe the band offsets between two semiconductors A and B, or an oxide and a semiconductor. Charge transfer tends to align the CNL of the bulk oxide and the CNL of Si. The CB offset is then [20],

$$\phi_n = (\chi_a - \Phi_{S,a}) - (\chi_b - \Phi_{S,b}) + S(\Phi_{S,a} - \Phi_{S,b}) \tag{16}$$

Here, χ_a is the electron affinity (EA) of the oxide, χ_b is the electron affinity of the semiconductor, and $\Phi_{S,a}$ and $\Phi_{S,b}$ are the CNLs of the oxide and semiconductor respectively. All the energies in eqn (15) are measured from the vacuum level, except ϕ_n which is measured from the conduction band edge. S is again the Schottky barrier pinning factor. Note that for two semiconductors, the MIGS only exist where there are band states on one side of the interface, but not where there is a gap on both sides [164], Fig 27(b).

This CNL model is a zeroth-order, but fully parameterised model of band offsets, in which the CNLs are determined by the bulk electronic structure of oxide and Si. The local bonding at the interface does not enter in this model. The CNL acts like the mean electronegativity of the semiconductor [19].

The CNL is an intrinsic property of the bulk semiconductor. It is not a function of the surface chemistry or reconstruction. It is only a function of the bulk band structure [162,20].

The predicted CB offsets in this model [20,103,165] are given in Fig. 28 for the various oxides. Table 3 compares these to the experimental values measured by photoemission, internal photoemission or barrier tunneling [166-186]. Photoemission measures the VB offset, and this is converted into the CB offset by subtracting the oxide and Si band gaps. Internal photoemission measures the energy from the Si valence band to the oxide's conduction band, or the Si conduction band to the oxide's valence band, depending on the Si doping and of the polarity of the applied voltage.

It is seen that the predicted and experimental offsets generally agree well. Those for HfO_2 and ZrO_2 from photoemission agree well [161,184]. $SrTiO_3$ indeed has a small CB offset [166]. Data by Hattori [178] for La_2O_3 that agrees well with the prediction of 2.3 eV. La_2O_3 and $LaAlO_3$ have a particularly large CB offsets [178,182]. The experimental and calculated vales for Lu_2O_3 and Gd_2O_3 are also in reasonable agreement [180]. There is good agreement for Al_2O_3 made by oxidation [167,168]. For ALD Al_2O_3 it is important to use the correct phase [108,170].

It is seen that only Zr, Hf, Al, Y, and La oxides have CB offsets over 1 eV, which is the minimum needed to limit electron injection. The CB offsets decrease in the order of group III, IV, to IV metal oxides. This is because the CNL of the oxide rises in the gap along the sequence group III to V.

The MIGS model predictions have been extended to oxides on Ge and on GaAs [185]. The predictions generally agree fairly well with the experimental values, found by either photoemission or internal photoemission.

4.5 Bonding at HfO_2-Si Interfaces

The simple MIGS model of oxide interfaces is surprisingly successful. Nevertheless, it is useful to have a detailed bonding model for direct Si-oxide interfaces. Firstly, the band offset can depend on the interface bonding. Secondly, imperfect interfaces will have defects which can create gap states which trap charge. Third, the control of work functions in the case of metal gates requires this understanding of interface chemistry.

It is necessary to use epitaxial models in order to understand the bonding at these interfaces [187-196] . The Si:HfO_2 system was used as a model, with reasonably a well lattice-matched interface to cubic HfO_2. The lattice constants of Si and HfO_2 are 5.43Å and 5.12Å respectively. Thus HfO_2 could be grown epitaxially on the Si(100) cube face (as ZrO_2 was [192]), with the HfO_2 cube face lying directly on top of the Si cube face. This is expressed as HfO_2(100)//Si(100), and with the [001] directions of Si and oxide parallel, that is HfO_2[001]//Si[001].

The ideal (100) surfaces of HfO_2 are polar, being oxygen terminated. However, we can construct bulk non-polar units of HfO_2 as $O^{2-}Hf^{4+}O^{2-}$ (or 'OHfO') units by assigning O's alternately up or down to give non-polar faces [189,190].

The interface should be insulating, with no gap states, otherwise an FET will not work. We can determine which interface configurations are insulating by an electron counting rule. For the ideal Si(100) face (Fig 29b), each Si atom would have two dangling bonds (DBs) [189]. These create states in the gap. If we place a non-polar OHfO unit on this (100)Si face, there will be no reaction, and this will still leave Si DB states in the Si gap. These gap states will create a metallic interface.

If instead we first put an oxygen across the two Si DBs, this forms a Si-O-Si bridge which ties up the DBs and removes their gap states. We can then add non-polar OHfO units on top. A complete HfO_2 lattice can be built up on top of this interface by adding additional non-polar OHfO layers. This interface will have no gap states, and is insulating.

This also works for Hf-termination, Fig 29(c). In this case, the first layer is a HfO unit which is formally $Hf^{2+}O^{2-}$ and the Hf has two unsatisfied valences. These can make two Hf-Si bonds to the Si DBs. This also gives an insulating interface with all valences satisfied. The two examples show that we can obtain insulating interfaces, if *polar faces* of HfO_2 are used. The three cases of O-rich, non-polar O and Hf terminated interfaces are shown in Fig 29.

Detailed calculations confirm the simplified bonding analysis [190]. Some lower symmetry configurations were also studied. Fig. 30(a) shows the ideal Si:OOHfO interface, with a double oxygen layer at the interface. Here the interfacial oxygens are initially 6-fold coordinated, bonded to two Si's and four Zr's. These interfacial oxygens relax to form the structure shown from two directions in Fig 30(b). Those oxygens lying in the Si-O-Si bridges relax towards the silicon layer. The other two oxygens relax up towards the HfO_2 layer. This interface is denoted the O_4. Overall, these interfaces have the same number of oxygen atoms at the interface. Another interface denoted O_3 interface is a slightly more stable structure. Finally, an interface shown in Fig 30(c) would be formed by a literal ALD process, but this is less dense and less stable.

The non-polar interface of Fig 29b would be metallic, in a high symmetry configuration. In a doubled unit cell, the interface reconstructs to break symmetry and create a band gap.

For Hf-terminated interfaces, the simplest has 6-fold coordinated Hf_6 sites, as in Fig. 31(a). This structure relaxes so that the interfacial Hf-Si bond becomes longer. This interface is insulating in the full calculation. Fig 31(b) shows another interface in which Hf is 10-fold coordinated,. This bonding is similar to that in $ZrSi_2$. This Hf_{10} interface is the more stable than the Hf_6 interface by 0.3 eV per interface Si [190].

In summary, the O_4, O_3 and Hf_6 interfaces are insulating. They have no states in the Si band gap. The Hf_{10} interface is metallic, despite formally satisfying the electron counting rule, because it is over-coordinated. Thus, only O-terminated interfaces are useful for devices.

The valence band offsets for the various Si:HfO_2 interface structures can be from the partial density of states of Si and oxide. The conduction band offsets are not given well by the LDA calculations, due to the LDA band gap error. The CB offset is found from the VB offset by adding the experimental band gap. The VB offset for the various O-terminated interfaces of ZrO_2 are found to be similar to the VB offset from from the CNL method. In contrast, the VB offset for Hf-terminated interfaces has a large variation of 0.9 eV between Hf_{10} and Hf_6, being much larger for Hf_6. This is due to a large change in the interface dipole. Summarising, the interface-specific dipole is quite small for the O-terminated interfaces, but large for the Hf-terminated interfaces. These results emphasise how much the interface dipole can depend on termination, and go beyond the MIGS model.

Realistic models of the HfO_2:Si(100) interface, including interfacial SiO_2 layers, have been created by Gavartin [197], Broqvist [198], and Alkauskas et al [126]. The presence of the SiO_2 does affect the previous band offset values. The Si termination is similar to that expected from ALD reactions.

5 Electronic structure of Defects

5.1 HfO_2

A problem with high K oxides [199] is that they can contain a much higher concentration of defects than in SiO_2. The two defects in HfO_2 with the lowest formation energy are the oxygen vacancy and the oxygen interstitial, fig 32(a,b), according to Foster et al [200,201]. Metal site defects cost more, because of their higher coordinations.

First, consider the oxygen vacancy in HfO_2. Recall that the valence band of HfO_2 consists mainly of O p states and the conduction band consists mainly of Hf d states. The electronic structure of the oxygen

vacancy and oxygen interstitial in HfO_2 have been calculated by various groups [200-214, 124,127]. Many used LDA methods. The LDA produces good total energies and structures, but LDA under-estimates band gaps, by 30% in the case of HfO_2. It also gives the wrong localisation of gap states even when filled. To correct for the band gap error, methods which go beyond LDA such as hybrid functional must be used. Xiong [124] used the screened exchange (SX) method to calculate the defect excitation energies for HfO_2 with a 48 atom supercell. The geometry was relaxed in GGA and the energy levels calculated in SX. This was repeated recently for a 96 atom cell. Similar results were later found by Gavartin [211], Broqvist [127], Choi [212] and Lyons [213].

The O vacancy creates singly degenerate gap state of near spherical A_1 symmetry. It is occupied by 2 electrons for the neutral vacancy. The state is strongly localised on the d orbitals of the adjacent Hf ions. In c-HfO_2, the relaxed neutral vacancy gives a gap state at 3.8 eV above the oxide VB, in Fig 30. The ionic positions do not relax much from their ideal positions in the neutral vacancy, the Hf-Hf distance is 3.59 Å compared to 3.54 Å in bulk HfO_2.

At the positive vacancy, V^+, the A_1 defect state is now singly occupied. Its net positive charge causes the adjacent Hf^{4+} ions to relax outwards from the vacancy. The Hf-Hf spacing becomes 3.74 Å. This relaxation causes the defect state to move upwards from 3.2 eV to 4.7 eV, Fig 33. At V^{2+}, the A_1 state is now empty. The greater positive charge causes further outward relaxation of the Hf ions so the Hf-Hf separation is 3.90 Å and the gap state rises to 5.2 eV.

The vacancy can also trap one or two *electrons* (despite being an anion vacancy). A trapped electron causes the adjacent Hf ions to distort asymmetrically (by the Jahn-Teller effect), pulling down an extra, singly-degenerate state of B_1 symmetry out of the conduction band. It is singly occupied for V^- and doubly occupied for V^{2-}. The A_1 state is full in both cases. The complete spectrum of the vacancy levels is summarised in Fig 33.

The formation energy of a defect, H_q, can be calculated as a function of the Fermi energy (ΔE_F) from the valence band edge E_V and the relative chemical potential ($\Delta\mu$) of element α [213],

$$H_q(E_F,\mu) = [E_q - E_H] + q(E_V + \Delta E_F) + \sum_\alpha n_\alpha(\mu_\alpha^0 + \Delta\mu_\alpha) \qquad (17)$$

where (E_q) is the total energy for the defect cell with charge q, E_H is the total energy for the perfect cell, $q.E_V$ is the change in energy of the Fermi level when charge q is added and n_α is the number of atoms of species α. The oxygen chemical potential (μ_O) can vary between the O-rich limit which is taken to be that of the O_2 molecule $\mu_O = 0$ to the O-poor limit which corresponds to the Hf:HfO_2 equilibrium, which is $\mu(O) = -5.9$ eV, the experimental heat of formation of HfO_2 per O atom [214].

Fig 34(a) shows the defect formation energy of the vacancy vs Fermi energy for the O-rich limit, and for the O-poor limit. At each value of Fermi energy we look for the lowest energy charge state, the most stable. The neutral state is the most stable for E_F between 3.2 eV and 5.2 eV. Below 3.2 eV, the V^{2+} is most stable. Above E_F = 5.2 eV, the V^- and then V^{2-} become the stable states.

The formation energies for the O-poor limit are simply those for the O-rich limit displaced downwards, Fig 34(b). In the O-poor limit, the cost of an oxygen vacancy is quite small, only 0.8 eV [214]. This is in fact standard. The cost of an O vacancy of any oxide is close to zero in the O-poor limit. The collorary is that the formation energy of an O vacancy in the O rich limit is roughly the bulk heat of formation per O atom.

The other main defect in HfO_2 is the oxygen interstitial [124,201,207,209,214]. It can have various charge states, see Fig 30. The energy levels were calculated using SX [214]. The simplest configuration is the closed shell species I^{2-}, equivalent to an extra O^{2-} ion. In this state, the interstitial O is well separated from the other O^{2-} ions and it adds filled O 2p states to the valence band. At the O^-, removing 1 electron leaves a hole at the VB edge. This radical anion moves slightly closer to another O^{2-} without actually forming a full O-O bond, the O-O distance is 2.0Å. The neutral interstitial or O^0 has two holes in the O 2p levels. The two holes allow this interstitial to form a true O-O bond, giving the dumb-bell shaped superoxy anion O_2^{2-}. The O-O bond length is 1.49Å. This O-O bond creates a filled bonding (σ) orbital at

–6.0 eV just below the main valence band and an empty antibonding (σ*) orbital at 4.1 eV in the upper gap region. It also has filled double degenerate pπ and π* orbitals at –3.0 eV in the valence band and at +0.3 eV just above the VB edge (Fig 33). Fig 34 shows the formation energy of the O interstitial for O-rich and O-poor conditions.

The I^0 could trap a further hole to give the O^+ interstitial, or superoxyl radical. This O^+ ion forms a shorter O-O bond with a O^{2-} ion of length 1.39 Å, giving a dumbbell O_2^- ion. This gives rise to an empty σ* state in the upper gap at 4.5 eV, (Fig 32). It also has a filled π state and a half-filled π* state. This O_2^- ion is called the superoxyl radical. The hole resides in one of the π* states, breaking their degeneracy. This radical has a characteristic g factor and has been seen by electron spin resonance in HfO_2 thin films [215].

5.2 HfO_2 defects: Experimental observations

The charge trapping characteristics of HfO_2 defects have been intensively measured. The trapping characteristics follow the same curves on repeated cycles, indicating that traps get filled and emptied, with no new defects created [216,217], Fig 35.

Kerber [218] interpreted the trapping curves as fast trapping and detrapping of electrons in the oxide. and that the trapping data were consistent with an electron trap level lying just above the Si conduction band edge. Using electron detrapping data over a wider temperature range, Mitard [219] gave levels at 0.8 eV and 1.5 eV below the HfO_2 conduction band edge, or more accurately at 0.7 eV and 1.3 eV above the midgap of the underlying Si. Cartier [220] noted that the levels measured by 'amplitude charge pumping' (ACP) agreed well with the calculated energy levels of the O vacancy, and that their density correlated with the oxygen deficiency for variously prepared samples. The energy spectra of the traps can also be derived by inelastic tunnelling spectroscopy [221], charge pumping and CV methods [222]. The density of levels found by ACP correlated linearly with bias stress voltage change measured on differently prepared gate oxides. This indicates that the O vacancy is the primary cause of the charge trapping instability in HfO_2.

Optically, Takeuchi [223] identified an absorption band at 4.5 eV in spectroscopic ellipsometry on HfO_2 films oxidised to different degrees. They attribute this to transitions from the valence band to an oxygen vacancy level at 4.5 eV. The peak was seen in optical absorption by Nyugen [224]. The transition was seen by cathodo-luminescence in HfO_2 films by Walsh [225]. There was concern that the absorption band might correspond to the E2 absorption of the underlying Si substrate, but the other spectroscopic tools suggest that the identification with the vacancy still holds.

The oxygen vacancy is the main mechanism for oxygen diffusion in HfO_2 and related oxides, so there have been a number of efforts to correlate vacancy concentrations as a function of oxygen partial pressure by Guha [226,227], McIntyre [228], and of oxygen diffusion measurements by Zafar [229].

The chemical nature of the traps can usually be determined directly by electron spin resonance (ESR). So far, many of the defects seen by ESR in HfO_2 on Si have been related to the interfacial Si dangling bond, the so-called the P_b centre [230,231]. Kang [215] identified two paramagnetic defects in bulk HfO_2 produced by ALD; the Hf^{3+} ion (an electron trapped at Hf^{4+} or V^+) and the superoxy radical. The problem with the ESR data for the O vacancy is that the observed ESR g matrix has an axial symmetry [232] which does not fit the expected spherical symmetry of an A_1 state. However, it is now realised that LDA gives defect wavefunctions that are too delocalised. Fig. 36(a) shows the symmetric wavefunction found by LDA. If hybrid functionals such as B3LYP or SX are used instead, these methods find a more localised wavefunction and lower symmetry defect, as seen in Fig 36(b), and this is now consistent with the experimental ESR signature [233,208].

The conduction processes in insulating thin films can be classified as limited by bulk or interface prcocesses. Bulk processes include hopping through traps (Poole-Frenkel) and space-charge limited current (SCLC). For HfO_2 and ZrO_2, Poole-Frenkel hopping may be dominant for thicker films, over 4 nm. For thinner films, Houssa [234] attributes conduction to trap-assisted tunnelling (TAT). Tunnelling

should be essentially independent of temperature, hopping T-dependent. The technologically relevant films of HfO_2 tend to be only 2-3 nm thick. In this range, TAT occurs for V<0.5V [48, 235], and direct tunnelling occurs for higher voltages. In all cases, conduction is by electrons, because the CB barrier is lower. The relevant traps are the oxygen vacancy levels.

5.3 Defect Passivation

The defect densities in HfO_2 can be reduced by passivation. The standard method to passivate dangling bond type defects in covalent semiconductors or SiO_2 is a forming gas anneal in hydrogen. The hydrogen ties off the dangling bond, and moves the states out of the gap. HfO_2 is different, it has ionic bonds and the defects are not dangling bonds. Different strategies are now required.

Annealing in ammonia or nitrogen was found to lower leakage currents, which might be realted to lowering the defect density. Umezawa [236] noted a possible mechanism of nitrogen passivation of O vacancies in which two nitrogens substituted for oxygen next to a neutral oxygen vacancy, VN_2, removed the vacancy–related gap state. The passivation occurs because each substitutional N would leave a hole in the VB (Fig 37b), so the two electrons of V^0 fall into the hole states, making an effective doubly postively charged vacancy [202]. The Hf ions adjacent to the vacancy relax outwards, as in the simple V^{2+}, but here the relaxation repels the A_1 level completely out of the gap, Fig 37(a). The configuration now has a 'closed shell', so it should not give rise to gap states, Fig 37(c).

Gavartin [237] studied other configurations of N in HfO_2. These configurations still give gap states, so they are not passivating the defects. Nitrogen introduces N 2p states in the lower gap, which lie above the normal valence band edge [238], so this reduces the local band gap. However, the valence band offset is large, so this does not have a deleterious effect.

The vacancy can also be passivated by the substitution of two Hf sites by a trivalent metal such as La [239,240] (Fig 38). In this case, two La ions are substituting for two Hf ions, next to the O vacancy. The two trivalent La sites lead to two holes in the valence band, into which the two electrons of the neutral vacancy fall. As above for N, this leaves a closed shell and a V^{2+} vacancy. As in the case of nitrogen above, the relaxed V^{2+} pushes its A_1 state up out of the gap, into the conduction band. Both these methods can be used to improve the reliability of HfO_2.

Fluorine passivation has also been found to be beneficial by Tseng [241] and McIntyre [242], probably because F might insert into oxygen vacancies. According to calculations, the F lies in the vacancy, and repels any vacancy states into the oxide conduction band, thereby passivating the vacancy [243] (Fig 34). However, a disadvantage is that too much fluorine will lower K.

It turns out that many inpuririte and defects can be passivated in HfO_2 because of the nature of wide band gap systems [244].

5.4 Defects in Al_2O_3

Al_2O_3 is the other widely used high K oxide. This is partly because of its ability to remain amorphous, and partly because it is a good atomic diffusion barrier. It is widely known to have a fairly high concentration of defect states. This can be advantageous for some memory applications.

The lower symmetry θ-Al_2O_3 phase is used as a model for the amorphous phase [109,245]. Fig 39 shows the defect formation energy as a function of Fermi energy for the O vacancy. It is seen that the O vacancy has 5 stable charge states in the gap, +2, +1, 0, -1, and -2. This means that there are four transition levels, +2/+1, +1/0, 0/-1 and -1/-2. This may be why the defect levels of Al_2O_3 appear to be broadly distributed across the gap.

The calculated transition states have ben compared to experimental data. Liu [109] showed that the 0/-1 level corresponds to the main hopping level observed in transport experiments [246-249]. Choi [245] has studied the defects in α-Al_2O_3.

Defect levels have also been calculated for La_2O_3 and the perovskites $LaAlO_3$ and $LaLuO_3$ [250] as shown in Fig. 40.

6 Metal gates

6.1 Work function requirements of metal gates

The purpose of the gate electrode in CMOS is to shift the surface Fermi level E_F of the channel to the other band edge, to invert the transistor. An NMOS FET consists of a p-doped Si channel. A gate electrode of low work function (~4.05 eV) will move its surface Fermi level from the Si valence band to the conduction band, inverting the channel. Similarly, a PMOS device has a n-doped Si channel, and a gate with a work function of 5.15 eV shifts its E_F to its valence band, inverting the channel. This requires a work function change of 1.1 eV, the Si band gap. The work functions of metals are tabulated by Michaelson [251].

For previous MOSFETs with SiO_2 dielectric, the gate electrodes were polycrystalline Si highly doped n-type or p-type respectively, for NMOS and PMOS respectively. This gives work functions of 4.05 and 5.15 eV, respectively. Poly-Si has the advantage that it is a refractory material, easily deposited, and compatible with SiO_2 and the associated process flows. However, doped poly-Si has a limited carrier density, and so it adds a depletion length of ~3Å to the ECT, as in Fig 4. Real metals have a depletion lengths under 0.5Å, so using them lowers ECT by 3-4 Å.

6.2 Effective Work Functions

The requirement for the two metal gate replaced doped poly-Si is that they should be able to swing E_F over that 1.1 eV range of work functions. The key point is that SiO_2 is an essentially perfect insulator so that a work function applied on the top of a thin SiO_2 layer gives a work function of the same value at the Si:SiO_2 interface. This is not necessarily the case for metals on thin HfO_2, for various reasons. The ability to swing the surface work function of the Si is measured by the CV plot.

We first recall the description of Schottky barriers and MIGS in section 4.4. The Schottky barrier pinning factor S given by

$$S = d\phi_{FB}/d\Phi_M$$

defines how strongly the Schottky barrier height (SBH) is pinned. If the density of MIGS is large, there is strong pinning and S = 0. If the MIGS density is small, there is little pinning and S = 1. SiO_2 behaves almost like a vacuum, its MIGS are very weak, and there is no pinning, so S = 1. This means that metal work function act as if at a vacuum interface.

This is not the case for the HfO_2 surface. Using formula (15) gives S ~ 0.5 for HfO_2. Some of the experimental data suggests that this value is correct. Therefore, moderate Fermi level pinning was expected for HfO_2 on Si. Yeo [252] noted that this would be a disaster for HfO_2. Rather than chosing metals with a work function difference of 1.1 eV between nFeT and pFET, we would need a work function swing of 2.2 eV to obtain a SBH swing of 1.1 eV. The work function of Pt is 5.65 eV, so that a work function of 3.4 eV would be needed for an nFET gate. This would be an extremely electropositive, reactive metal like Sc.

This led to the use of 'effective work function' (EWF) as a way of defining how much voltage shift a given gate electrode would provide, when referenced to the vacuum level. Formally, it references the surface potential on Si to say the Si conduction band energy, and then adds the Si electron affinity (Fig 42). The EWF or $\Phi_{M,eff}$ can also be thought of as linearising the pinning effect, as

$$\Phi_{M,eff} = \Phi_{CNL} + S(\Phi_{M,vac} - \Phi_{CNL})$$

where a reference energy such as the CNL energy Φ_{CNL} is used for convenience.

6.3 Practical control of the Work Function

Figs 43 shows some data for the barrier heights of some metals on HfO_2 as measured by CV or by internal photoemission. Some data such as from Afanasev [169,170] suggest that S ~ 0.7. On the other hand, data by Koyama [253] taken with more annealing suggested larger S values. Zafar [254] derived barrier height of metals from a conductivity method and found that the SBHs of three refractory metals (TaSiN, W and Re) on HfO_2 corresponded to S=1.

The first extensive compilation of EWFs by Schaeffer [255] in Fig 44 found a low value of S, suggesting a problem. These results suggested some intrinsic Fermi level pinning. Similarly, a Fermi level pinning effect at poly-Si gate / HfO_2 interfaces seen by Hobbs [62,64] was attributed to the formation of Hf-Si bonds at the HfO_2-Si interface [66].

On the other hand, Schaeffer [256] showed that the effective work function of Pt depended reversibly on its treatment by a forming gas (reducing) or oxidising anneals, implying a large extrinsic effect. Cartier [257] showed that the work function of a Re electrode depended greatly on its annealing in reducing or oxidising conditions, as in Fig 45. These data indicate that the WF shifts on p-type metals are an extrinsic effect due to defects or chemistry, not due to MIGS.

Majhi [258] and Wen [259] carried out a detailed study of more refractory metal electrodes (typically TiSiN, TaSiN etc). Because the flat band voltage can depend in general on both charge defects in the oxide and the interfacial potentials, the EWF was extracted usig a more reliable method using terraced oxide or 'wedding cake' samples [260], as in the inset to Fig 46(a). Here, the thickness of the interfacial SiO_2 varies, the HfO_2 thickness is constant. The data in Fig 46(a) showed that the measured range of EWFs of metals on HfO_2 was less than on SiO_2, but not hugely less, and more importantly, they could span the band gap of Si, and invert both NMOS and PMOS. This data is replotted in Fig 46(b). By assuming S=1 for metals on SiO_2, we extract a value of S ~ 0.82 for metals on HfO_2. This then led to an era of searching for manufacturable metal combinations to use as NMOS and PMOS metal gates.

There were two approaches. First, Tseng [261] and Schaeffer [262] found that sufficiently refractory metal carbides such as TaC_x had a low and stable EWF on HfO_2 of about 4.2 eV, reasonably useful for nFETs. This method works because TaC is so strongly bound that it does not react significantly with the HfO_2. On the other hand, there was no clear pFET solution using electronegative metals.

The extrinsic pinning effect led to a new industrial solution, gate last vs gate first (Fig 6). The gate first process follows the standard process flow, but with a metal gate replacing the poly-Si gate. This appoach was followed by IBM [263,264]. It is more difficult metallurgically because the gate metal must withstand the full process 1000C temperature.

Alternatiively, in order to avoid electrode reactions occurring at high temperatures, the gate last process was developed. It makes a dummy poly-Si gate as in the standard process. The 1000C post-deposition anneal on the channel dopants is carried out, then the dummy gate is removed and the replacement metal gate is put into the gate space. It is then subjected to a much lower temperature anneal of order 550C. This process has more process steps but avoids metallurgical reactions. It requires a high degree of control of the chemical mechanical polishing (CMP) that planarises the dummy gate area to enable its removal.

6.4 Work function control

These experimental observations show the need to improve our understanding of Schottky barriers. To understand metal-HfO_2 interfaces in more detail, the SBHs for epitaxial interfaces of various metals on cubic HfO_2 were calculated [265,266]. This calculation requires that the metal is lattice-matched to the HfO_2. Only Ni and Co are closely lattice-matched to HfO_2. For other metals, we force the lattices to match in the interface plane, and allow them to relax normal to the interface. In addition, we take all the metals to be FCC, even if this is not their most stable phase. The vertical dimension and all atomic positions were allowed to relax.

The barrier heights were calculated from the offset of the valence band local density of states on metal and oxide atoms far from the interface. The offsets can be adjusted for the GGA band gap error by lowering the oxide valence band edge by the GW correction of 1.23 eV if desired [187].

Interfaces can be polar or non-polar [267,268]. The simplest non-polar (type 1) face of HfO_2 is (110), while (111) is a type 2 non-polar face. The (100) face is polar, and can be O-terminated or Hf-terminated. A non-polar (100) face can be made by removing half of the terminating oxygens in the O-rich interface. Fig 47 shows these various interfaces for HfO_2 on Ni.

The lattice constant of HfO_2 is ~1.4 times greater than that of Ni. The lattice-matching occurs by rotating the Ni lattice by 45^0 on (100). This rotation will also allow matching on (110), but not (111). A modified interface was constructed for (111).

Fig 48 plots the calculated barrier heights of metals on HfO_2 against their experimental work function from Michaelson [251] for both the non-polar and polar interfaces. We see that there is a large offset between the barrier height for the two cases; the O-rich interface has a much lower valence band offset, or a higher EWF. Secondly, the slope of band offset versus work function, S, is calculated to be 0.92, or close to 1. Thus, first principles calculations find the interface to be essentially *unpinned*. The fact that the pure metal:HfO_2 interface is unpinned is important. It is consistent with the experimental observations of metals on HfO_2 as seen in Fig 46 [259].

6.5 Extrinsic pinning models

It is clear from the above result and also the ability to vary the gate threshold voltages reversibly by annealing in a hydrogen atmosphere that the pinning is extrinsic. The Fermi level pinning mechanism for electronegative (pFET) metals involves oxygen vacancies and band-bending in the oxide [260-262]. The vacancies are created by the high temperature anneal. The O vacancy is neutral, and it has an energy level in the oxide near the Si conduction band energy occupied by two electrons [120]. These electrons can gain energy by falling down to the metal E_F [269,270], which is large for electronegative metals, Fig 49(a). This gives the vacancy levels a positive charge, which causes upward band bending of the oxide layer, thereby reducing the EWF of the gate electrode, referred to the channel, Fig 49(b). However, it turns out that the vacancy formation energy is too large at an O chemical potential of $\mu_O = 0$ eV, for there to be enough charged O vacancies to cuase much band bending [269-271]. However, the HfO_2 can react with the underlying Si, the μ_O is greatly reduced, and many vacancies can form.

The simplest way to understand it follows from the formation energy diagram, Fig 50. The formation energy of the vacancy depends on the charge state, via the Fermi energy, but also on the O chemical potential μ_O. For $\mu_O = 0$ eV, that of the O_2 molecule, then the vacancy formation energy is large, 6.8 eV. This μ_O is appropriate for the as-deposited film. However, the HfO_2 gate oxide is not as-deposited, it is annealed sitting next to a large excess of Si. This excess can greatly reduce the oxygen chemical potential, once the temperature rises to allow O diffusion to react with the Si and form more SiO_2, Fig 51. The O vacancy now is much easier to form [271].

Fig. 50 plots the O vacancy formation energy for $\mu_O = -4.7$ eV, the O chemical potential of the Si/SiO_2 equilibrium. The neutral oxygen vacancy now costs 1.3 eV. The O vacancy formation energy then becomes negative when E_F lies less than 3.5 eV above the HfO_2 valence band, that is for effective WFs larger than 5 eV. This leads to the creation of +2 vacancies, which cause band-bending next to the gate electrode. This reduces the EWF of high WF metals. For this reason, obtaining a sufficiently p-type gate electrode is extremely difficult once HfO_2 is annealed above the O diffusion temperature of ~550 C.

This model accounts for the observations of Cartier [257] and Schaeffer [256]. The pinning occurs above ~ 600^0C because the O must diffuse to react with the Si. Cartier noted that the pinning can be reversed by O saturation if the vacancies are back-filled by oxygen [272].

The extrinsic Fermi pinning is most noticeable for p-metals on smaller EOT stacks. This is known as the V_t roll-off effect [12], as was shown in Fig 52. Song [273], Akiyama [274], Schaeffer [275] and Bersuker [276] have produced models to explain this effect, based on oxygen transfer. Bersuker [276] attributes rol-off to the formation of positively charged O vacancies close to the channel. Roll-off limits

the scalability of pFETs in the gate-first approach, and was a considerable influence in the move to gate-last.

6.6 Oxide Dipole layers

When the gate electrode was doped poly-Si, gate voltage control was arranged by changing the EWF of the electrode, by doping it n- or p-type. The first choice for metal gates was to choose two metals with WFs similar to those of n-type Si and p-type Si. This can lead to difficult lithography.

An alternative option is to have a single, stable metal electode like TiN with a midgap work function, and using an oxide 'capping layer' under the gate to control the net EWF through the gate stack, Fig 53.

It is found that oxides of electropositive group IIA and IIIA metals on top of the HfO_2 layer would shift the overall V_{FB} of the gate stack towards an n-type value, as achieved by Narayaanan [277], Guha [278], and AlShareef [278-279]. On the other hand, layers of Al_2O_3 can be used to shift the V_{FB} in a p-type direction [280,281]. The shift is roughly proportional to the capping layer thickness. In other words, it does not give a fixed V_{FB} value like for example doped poly-Si.

Finding the underlying mechanism of the capping layers was not simple. First, the $LaHfO_x$ alloy data of Wang [282] showed that the interfacial fixed charge was small, so that the effect was truly a dipole shift. Second, medium energy ion scattering showed that the capping layer did not remain at the upper surface. Under a 1000 C anneal, the La oxide distributes across the dielectric layer (Guha [277]) (Fig 54).

Yamamoto [283] and Iwamoto [284] then showed by a series of alternate depositions, that the interface determining the V_{FB} shift is not the top gate-oxide interface, but rather the lower SiO_2 –high K interface, because the capping layer oxide had diffused through the HfO_2 Fig 55. It was no longer a 'capping layer'. This applies to both La_2O_3 and to Al_2O_3 dipole layer systems. The effect might be due to the strong reaction of La_2O_3 and SiO_2 to form a silicate.

Presently three atomic scale mechanisms have been proposed. Guha [267] suggested that the group II or III metals substituting into the HfO_2 lattice would create oxygen vacancies, due to their different valence, and the charge oxygen vacancies would cause the dipole shift. Second, Kirsch [285] measured the V_{FB} shifts for a range of capping oxides, and found that the EWF shifts correlated with the dipole moment of the M-O bond, expressed on a Pauling scale of ionicities. Third, Jagannathan [286] noted that the V_{FB} shifts correlate with the metal electronegativity of the capping oxide, using the group electronegativity concept of Schaffer [287]. Most recently, Kita and Toriumi [288] proposed that the V_{FB} shifts correlate with the oxygen ion density in the various oxides.

These are all empirical models without any first principles modelling. In order to understand the atomic level mechanism, some periodic atomic models of the SiO_2-HfO_2 interface were constructed by Lin and Robertson [289,290], with substitutional La, Sr, Al, or Nb ions. These are based on the model interfaces of Sharia [291] with the (100) face of β-cristobalite SiO_2 matched to the (100) face of cubic HfO_2, if the HfO_2 lattice is rotated by 45^0. The interface has no broken Si-O bonds. A HfO_2 layer then contains 4 oxygens per layer, a SiO_2 layer contains 2 oxygen per layer, and the interfacial plane has 3 oxygens.

The La, Al, Nb, Sr or Mg dopants are then introduced into this supercell by substituting at Hf sites, especially at the interfaces, as in fig 56. Charge neutrality is mainrained. For trivalent dopants (La, Al), we introduce two La's and remove one oxygen from the HfO_2 or SiO_2 sub-layer. For divalent Sr or Mg dopants, we add one Sr and remove one oxygen. For pentavalent Nb, we substitute two Nb for Hf's and add back an oxygen at the interface layer to make four oxygens, to balance charges (Fig 56(e).

The atomic positions are then relaxed by LDA total energy methods. The electronic structure is calculated and the valence band offsets (VBO) are derived from the local density of states of HfO_2 and SiO_2 layers away from the interface. The VBO is written as positive if the HfO_2 VB edge is deeper than SiO_2 below the vacuum, to have the same sign convention as the flat band voltage.

Fig 56(a) shows the relaxed atomic structure of a pure HfO_2:SiO_2 interface. Fig 56(b) shows the structure of substitutional La_{Hf} sites at the HfO_2:SiO_2 interface. Their local atomic structure has relaxes so

that La sites become 6-fold bonded. Substitutional Al_{Hf} sites relax to become 4-fold coordinated, as in amorphous Al_2O_3 (Fig 57c). Interfacial substitutional Sr_{Hf} becomes 6-fold coordinated.

Fig 57(a) plots the VBOs of cells with various substitutional dopants at interfacial sites against the experimental V_{fb} shifts for Sr and La oxides from Kirsch [285], for Al_2O_3 from Linder [292], and the positive shift of Nb, compared to the base case of the pure HfO_2:SiO_2 system. We see that the shift direction is proportional to the experimental shift in each case. We find that the VBO does vary with the separation of the dopant and the vacancy, but this effect is much smaller than the main shift. Thus, the model reproduces the observed chemical trends.

Fig 57(b) plots the VBO shift versus the dopant valence. The calculated VBOs and experiment are similar for some cases. *However*, the trivalent dopants La and Al both introduce O vacancies but the calculated shifts are in *opposite* directions. On the other hand, trivalent Al and pentavalent Nb shift in the *same* direction. This argues against the vacancy model of Guha [277].

Fig 57(c) plots the calculated VBO shift against the work function of the dopant's parent metal, which is effectively its electronegativity. We see that the VBO shift varies *monotonically* with the dopant work function. Note that the shift of La and Al are in the opposite directions, consistent with La having a lower WF than Hf and Al having a higher WF. On the other hand Al and Nb have a calculated shift in the *same* direction, despite their different valences, but consistent with both having similar WFs, both higher than Hf. Note that the V_{fb} shift of Sr is larger than that of La, consistent with the calculated VBO shift, and with the lower work function of Sr than La.

Hence, the VBO shift correlates with dopant electronegativity/work function, not with its valence. Our supercells have the same oxygen ion density, by construction, but the calculated VBOs differ greatly. Thus, the VBO does not correlate with oxygen ion density [288]. Hence, our models exactly reproduce the experimental trends of V_{fb} and allow us to eliminate a number of models.

These results still need a simple explanation [289,290]. Is the dipole due to bulk bonds or interface bonds? There are two arguments against a bulk dipole model. First, if the bulk is represented by layers A-B-A-B..., the dipole A^+-B^- on average cancels the dipole B^-- A^+, Fig 58(a), so that a network of bulk bonds does not create a net dipole. Second, a dipole is given by the product of charge and distance, Q•d. but Sr gives a larger V_{FB} shift than La, although Sr is 2+ while La is 3+ and their ionic radii are quite similar. Thus, the effect must arise from an interface or graded interface not a bulk effect.

The shift arises simply because there is a large change in dielectric constant, K, at the interface going from HfO_2 to SiO_2, Fig 58(b). The potential step due to a dipole is given by

$$\Delta V = \frac{nQd}{K}$$

where n is the ion density, Q its charge, d the bond length, not just the basic dipole Q.d. In this case, a dipole A^+-B^- does not cancel the dipole B^-- A^+, as in the bulk, because each dipole is screened by a different K value.

The V_{fb} shift between a pure HfO_2 and a doped HfO_2 is related to the change in mean electrostatic potential across the interface, and thus in the group electronegativity. This accounts for the trends in Fig 57(c). This gives an explicit atomic model of the flat band voltage shifts introduced by metal-oxide capping layers. The V_{fb} shifts in the observed directions for all cases studied. The shifts correlate with the work function of the metal of the metal oxide, not with its valence or bond dipole.

7 Electrical performace

7.1 Mobility Degradation

The objective of device scaling is to create smaller, faster devices. High speed requires high source-drain current, which in turn depends on the carrier mobility. Carriers in the FET behave like a two-dimensional electron gas. The carrier density is determined by the vertical (gate) electric field which

induces them. The carrier mobility in a 2D electron gas is found to depend in a 'universal' way on the gate field, according to a so-called 'universal mobility model', such as that by Takagi [293], in which the mobility of electrons and holes depends only on the effective gate field and the Si face, [100], [110] or [111]. The individual scattering processes ν_i add up into a total scattering rate ν,

$$\nu = \nu_1 + \nu_2 + \nu_3$$

so the processes limiting mobility add up according to Matthiessen's rule,

$$\frac{1}{\mu} = \frac{1}{\mu_C} + \frac{1}{\mu_{PH}} + \frac{1}{\mu_{SR}} \qquad (17)$$

where C= Coulombic scattering, PH = phonon scattering, SR = interface roughness. The mobility is limited by different mechanisms at different gate fields, as in Fig 59. At low fields, the mobility is limited by Coulombic scattering by trapped charges in the oxide and/or interface; at moderate field it is mainly limited by phonon scattering, and at high fields it is mainly limited by interface roughness scattering. The different mechanisms also have different temperature dependences, with Coulomb scattering and roughness scattering being T independent.

CMOS devices with a SiO_2 gate oxide have carrier mobilities close to the 'universal limit'. In that case, the mobility is limited mainly by the $Si:SiO_2$ interface roughness. The mobilities of high K gate oxide devices initially lay well below this universal curve, as seen by the data of Gusev [17], Ragnarsson [294], Guha [295], Hiratani [296], Torii [297] plotted in Fig 60, particularly for NMOS devices.

There are two main mechanisms of mobility lowering. The first mechanism is remote phonon scattering (RPS) by low energy polar phonon modes in the oxide by Fischetti [298], Fig 61. The second mechanism is remote Coulomb scattering (RCS) by trapped charge of Saito [299]. RCS is clearly important, as some high K oxides such as Al_2O_3 *with no soft modes* do show mobility degradation [17].

A lower nominal mobility might also arise from reduced carrier density, due to some of the induced charge being trapped at interface traps and not contributing to the mobile charge (Zhu [300]). This effect can be recognised by Hall measurements of mobility, where a direct decrease in Hall mobility can be seen in Ragnarrson [301].

Fischetti [298] noted that the high K of most oxides results from their low-lying polar vibration modes, the same modes that make a high K. The oxides are incipient ferroelectrics and these soft polar modes would drive a ferroelectric instability if their frequency fell to zero. These polar modes have a strong coupling to carriers in the Si channel – hence 'remote scattering'. On the other hand, in SiO_2 such modes have a much higher frequency and do not have a large coupling.

The importance of remote phonon scattering is that it is intrinsic and so it could be a *fundamental* limit to mobility in small EOT devices. On the other hand, remote Coulomb scattering (RCS) is an extrinsic effect, which one might hope to reduce by processing and reducing trap densities. RCS would be preferred technologically.

The two mechanisms can be distinguished by their temperature, field and thickness dependence. Phonon scattering is the only mechanism whose mobility decreases as the temperature is raised, because the phonon numbers increase with T. Surface roughness is independent of T, and mobility limited by Coulombic scattering can increase at higher temperatures, see Fig. 59. Ren [302] found there is indeed a T dependence of 1/mobility in the mid-field range where it is expected.

A second method to distinguish the mechanisms is to plot the mobility against oxide thickness, as in the work of Ragnarsson [301], Gusev [17], Casse [303], Lee [12], Narayanan [304] and Ragnarsson [305]. In this case, a device is made with a variable thickness of ALD-grown SiO_2 layer below a fixed thickness (30Å) of ALD HfO_2 layer. The SiO_2 layer spaces the scatterer (charge defects or phonons) away from the carriers. The mobility can be expressed as an 'additional inverse mobility' compared to the reference mobility for a gate stack with only the minimum SiO_2 thickness,

$$\frac{1}{\mu_{add}} = \frac{1}{\mu_{HfO2}} - \frac{1}{\mu_{ref}}$$

The extra inverse mobility is found to decrease exponentially with the SiO_2 layer thickness, t, (Fig 61) as

$$\Delta\left(\frac{1}{\mu_{add}}\right) = \frac{1}{\mu_0} exp(-2\beta.t)$$

where μ_0 is a constant and β equals the thermal wavevector, $\beta = (2mkT)^{1/2}/\hbar$. k is Boltzman's constant. Interestingly, RPS and RCS from the HfO_2 layer both decay with the *same* rate with *t* (Fig 62). Casse [303] showed data for non-optimised samples with a sizable mobility reduction. Ragnarrson [305] gave data for highly scaled, scavenged gate stacks.

Generally, remote Coulomb scattering is dominant at lower fields and phonon scattering at moderate fields. The excess scattering was found to vary linearly with gate field at low gate fields for varying SiO_2 thickness, Fig 63. This linear dependence is as expected for remote Coulomb scattering. This is strong evidence for RCS. The temperature dependence of the excess could also be derived. The total mobility plot was then re-assembled from the Mattheisen's rule and it was found to describe well the experimental data and its T dependence (Casse [303]). Thus, although the mobility is reduced at both low and medium fields, the main cause is RCS.

These observations have allowed firms to engineer a solution to the mobility problem, as seen in Fig 64. It is useful that there is an SiO_2 layer between the channel and HfO_2 layer to screen the remote scattering. The high K oxide layer should be thin, so that the defect density is low, and there are few traps Narayanan [304] optimised the annealing and nitrogen content of the HfO_2 interface to obtain the best mobility vs. T_{inv} performance. Their data in the upper part of Fig 64 now approaches the RPS limit, and is not so far below the universal mobility model limit.

The data was then extended by data from scavenged gate stacks, by Ragnarrson [305]. The interfacial oxide is of high quality, and the data is seen to follow the same trend. The mobility decreases as t_{inv} declines, and it is bounded by the theory curve (Fig 64).

7.2 Reliability

Generally speaking, the reliability for HfO_2 gate stacks arises from trapping at existing defects rather than the creation of additional defects [217]. Novel pulsed measurement methods have ben developed to speed up data collection [306].

There are two basic instabilties, negative bias stress instability (NBTI) which occurs in nFETs and positive bias stress instability (PBTI) which occurs in pFETs. In nFET and PBTI, the gate voltage is positive, and electrons are injected from the Si channel into the gate oxide at the energy of the Si conduction band. At this energy, the electrons are injected into the V^0 state of the O vacancy, Fig 65 [218,307]. This causes V_t to shift as a power law with time,

$$\Delta V_t = At^n$$

where the exponent n ~ 0.15 to 0.2. This mechanism causes a *large increase* in PBTI compared to a reference SiON dielectric, Fig 66.

On the other hand, in pFET and under NBTI, the gate is sent negative, and holes are injected into the oxide valence band. There is no particular hole trap in HfO_2 at this energy, and the holes become trapped at defects in the interfacial SiO_2 layer, Fig 65, causing NBTI [295]. Again, the V_t shifts follows the same power law as PBTI. In this case, the mechanism involves trapping in SiO_2 so the size of NBTI is *not* much larger than for the reference SiON case. This is shown schematically in Fig. 66.

The size of NBTI and PBTI both depend strongly on the thickness of the SiO_2 interlayer. Therefore NBTI and PBTI both increase strongly as the EOT is reduced by scavenging. Fig 67 shows a normalized version after Cartier [307]. The slope is seen to be very high. An unnormalised version is given by Ragnarrson [305], Fig 68. Fig 68 plots the gate bias voltage that would cause a 30 mV total PBTI or NBTI shift over a period of 10 years, the required lifetime. Thus, a small gate voltage implies an unstable device. This shows that NBTI does not allow EOT to be decreased below 6.5 A, on this basis. This makes reliability the limiting feature of small t_{inv} values. Thus, minimum oxide thickness does depend ultimately on reliability, just as in the 'Doomsday plot', but in a different era.

There are certain engineering solutions to improve the PBTI and NBTI reliability margins. PBTI due to electron injection into the O vacancy level can be reduced by removing the vacancy level by adding some nitrogen [305] or La [308]. As described in the defect section 5.3, N or La next to an O vacancy will repel the vacancy level to higher energies in the gap, so that electrons are no longer injected into that level.

NBTI can be reduced by band engineering of the channel band line-up. The exact nature of the hole trap in NBTI is not well known. Therefore it is not possible to passivate it. On the other hand, Franco [309,310] have found that in SiGe devices, the Ge-Si band offset can be used to cover up the defect level, to mitigate this trapping.

7.3 Scavenging and ultra-low EOT

The continued scaling of EOT below 1.0 nm and towards 0.5 nm requires us to either reduce the thickness of the interfacial layer, or increase the K values. In 2006-2010 there was considerable work towards developing oxides with higher K than HfO_2, as described in section 4.3. However, Ando [91] pointed out that the SiO_2 based interlayer makes the dominant contribution to EOT so that a higher K would have little effect. To solve this problem Ando [95] suggested increasing the K of the interlayer, for example by alloying it with lanthanides. However, there are disadvantages to adding La, as it affects the gate threshold voltage. These layers had an undesired effect on carrier mobility.

The remaining method was to reduce the interfacial SiO_2 layer thickness. The SiO_2 layer can be thinned by the oxide scavenging process, in which an electropositive metal is placed in the gate to extract O from the SiO_2 by diffusion through the HfO_2 layer, Fig 69. This reduces the SiO_2 back to Si. Fig 70 shows a TEM cross section of the gate stack after scavenging. This process requires that the heat of formation per O atom of the metal's oxide is greater than that of SiO_2 (Fig 71). Ando [95] and Frank [97] have carried out extensive work on this process. Fig 71 shows that W or Ta will not scavenge from SiO_2 but that Ti, Hf and La will do so. Ti is arguably the most suitable because the heat of formation of TiO_2 is larger than SiO_2 but not too large, and TiN has a mid gap work function whixch is also useful.

The scavenging process can be arranged so that the scavenging metal is placed in various locations, as shown in Fig 69. The temperature dependence of the scavenging effect depends on the oxgygen diffusion through HfO_2, as shown in Fig 72. The onset is at 450-550 C. Scavenging can be used in both gate first and gate last processes, by Ando [95] and Ragnarsson [305]. Scavenging can even be used in conjunction oxide capping layers setting the gate work function, in gate last process, with appropriate choice of anneal temperature to allow diffusion of both O and the cation. The electron mobility in scavenged stacks (Fig 73) follows a similar curve to that shown previously [94], fig 64.

The importance of the gate last process is that it enables the use of much lower process temperatures for the oxide. Given that scavenging can still be used for gate last, it is important to understand the degree of V_t control that can be achieved [311-313]. In particularly, there is the problem of V_t roll-off for the pFET [275]. Fig 74 plots the V_t vs EOT for gate last stacks, including the scavenged regime [312]. We see that the V_t's are not as close to the band edges in the linear regime as in Fig. 52. We see that V_t is constant down to lowest EOT values for nFET. For pFET, we see that V_t is constant down to EOT = 8 Å, and then turns down sharply, as the roll-off starts. It is notable that this critical thickness of 0.8 nm is much lower than the 2.5 nm for gate-first in Fig 52.

The net result is that scaling can continue to very small effective oxide thicknesses, as summarised in the Moore's Law plot in fig 75.

With the development of FinFET type device geometries, the need to use near band edge gate work functions is relaxed. It is possible to use TiN and $TiON_x$ drived from oxidised TiN as the n-type and p-type metal gates instead, Fig 76 [97].

8 Ge Oxides

8.1 Ge/GeO_2 interface

Germanium was employed for the original transistor, but was then abandoned in favor of Si due to its small band gap [314]. There has recently been a resurgence of interest in Ge [315-321], primarily due to its high injection velocity needed for continued scaling of CMOS.

Of the possible alternative semiconductors to Si, Ge stands out as a solution for both higher electron and hole mobilities. Ge has the highest hole mobility of any tetrahedral semiconductor, much higher than of Si (Table 4). However, the band gap of its native oxide is 33% lower and the bond energy of Ge-O bonds is over 35% lower than that of Si-O bonds. The Ge^{2+} state has higher stability than the equivalent Si^{2+} state. The charge neutrality level of Ge lies close to its valence band top, rather than 30% up the gap as in Si. Each of these aspects causes less easy device processing.

For devices, the performances of Ge pFETs are very good, with on-currents corresponding to the high hole mobilities. However, until recently, nFETs had poorer performances, not reflecting the high electron mobility, largely due to the higher D_{it} in the upper band gap [322,323]. Overall, D_{it} is an order of magnitude higher than for SiO_2 [321]. Thus we must understand the Ge interfaces better.

There are some well known problems with the $Ge:GeO_2$ system. The native oxide of Ge is hygroscopic. Second, GeO_2 is more defective, and the Ge/GeO_2 system had a much worse interface in CV plots [324]. However, if GeO_2 is deposited on SiO_2 and not in direct contact with Ge itself, then GeO_2 is a good insulator with few defects [325]. The problem with the $Ge:GeO_2$ system is the interface, not the GeO_2. The contact with Ge acts as a constant source of Ge, and under annealing, Ge and GeO_2 react to form volatile GeO molecules.

$$Ge + GeO_2 = 2\ GeO \uparrow$$

These problems lead to the formation of interface gap states. GeO formation can be suppressed by using a high pressure of O_2, as noted by Toriumi [326,327], and Kuzum [328].

The abruptness of the Si/SiO2 interface is seen by the low density of intermediate oxidation states between Si and Si^{4+} in the XPS core level spectra by Himpsel [56]. Keister [57] showed that the SiO_x phases at a non-abrup Si/SiO_2 interface would disproportionate into Si and SiO_2 giving a more abrupt interface.

Nevertheless, the $Ge:GeO_2$ interface can be flat and abrupt, as shown by the TEM cross sectional images and core level XPS data of Sasada [329], Fig 77. Secondly, Delabie [330] showed that the Ge/GeO_2 interface prepared in an optimum way can have a reasonanlby low D_{it} density, reminiscent of the desire for a SiO_2 interfacial layer below HfO_2 on Si.

The thermal stability of GeO_2 has been examined in detail in the context of the gate stack structure. The mechanism of GeO evolution from the GeO_2/Ge interface was studied by Ge and O isotopic labeling and thermal desorption spectroscopy methods by Kita [331,332]. It showed that O vacancies were the mobile species in GeO_2. The O vacancies are created by the interfacial reaction at the Ge/GeO_2 interface, the O vacancy diffuses to the top surface, and then it reacts with a GeO_2 unit to evolve as an GeO molecule, as summarised in Fig 78. It is not like a Deal-Grove process where an interstitial molecule diffuses through the oxide.

Hence, GeO formation must be supressed for better performance. This can be controlled through the use of high-pressure oxidation of Ge (>70 atm. O_2) followed by a lower temperature oxidation step [333]. It was recently shown that alloying an oxide of electropositive metal such as Y increases the

formation energy of the O vacancy, and thus reduces the diffusion rate of O vacancies in GeO_2. This reduces the etch rate of the GeO_2 and the volatilisation rate of GeO [334].

The band offsets for various Hf and Zr oxides on Ge have been measured by internal photoemission, separating out the band offsets of the GeO_2 interfacial layer by Afanasev [335,336] and by XPS by Ohta [337]. The offsets are quite similar to those on Si, the CB offset being higher by 0.1 eV. A problem for Ge is that GeO_2 has a much smaller CB offset than SiO_2, while the VB offset is similar to that of SiO_2 on Si [338,339], Fig 79. This arises because the band gap of GeO_2 is much smaller, while the VB top of GeO_2 and SiO_2 consists of O 2p states, so the VB offset is similar in both cases.

8.2 Ge dangling bond

A problem with Ge interfaces is that the Fermi energy is often pinned towards the bottom of the gap, and so it is difficult to invert from p-type to n-type [340]. The CV plots can appear poor. The low pinning energy has been attributed to the lower energy of the Ge dangling bond (DB) level than in Si [341], or equivalently to the low CNL energy. We recall that the DB lies near midgap in Si, and gives rise to two D_{it} peaks corresponding to its +/0 and 0/- transitions [342]. Weber [341] suggested that the neutral Ge DB level actually lies below the Ge valence band top, so that it is always in its negative configuration. In addition they suggest that the hydrogen interstitial level is also below the Ge VB top, so that hydrogen is also negative, and thus Ge^- and H^- will repel each other and prevent atomic hydrogen from passivating the Ge DB and forming a Ge-H bond. However, Broqvist [343] showed that Ge DB level lies low in the band gap, but just above the Ge VB top, and this DB should be observable. Note that the Fermi level at the Ge-metal interface is pinned low in the Ge gap [344,345], but the relevant question is where it is pinned at the Ge-oxide interface.

A further question about the Ge/GeO_2 interface is that the chemical identity of the interface states is not known. For Si/SiO_2 interfaces, Brower [346] could identify the P_b center as a Si DB from its ESR hyperfine spectrum.

In Ge, the interfacial Ge DB level (or Ge P_b centre) is difficult to observe by ESR. Houssa [347] suggested that the Ge P_b centre is less readily observed because of thermal effects, Fig 80. The temperature of viscous flow relaxation of GeO_2 is much lower than for SiO_2, so that annealing is presently carried out at a slightly too high temperature to observe Ge P_b. The GeO_2 network has relaxed sufficiently that the Ge P_b centers have been annealed away.

Recently, Stesmans et al [348,349] have observed the Ge P_b state center by ESR in Ge-Si alloys, in the 60-80% Ge composition range. Baldovino [350,351] have observed the Ge P_b by optical detected magnetic resonance at Ge/GeO_2 interfaces. Thus, the Ge DB does exist in the gap. The Ge DB signal has finally been observed at a defective $Ge:GeO_2$ interfaces by Paleari [352] using electrically detected magnetic resonance, Fig 81. It shows the angular response expected for a P_b center. Recently, the reaction of hydrogen with the Ge P_b center has been observed by Stesmans [353]. The difficulty of passivating the Ge DB arises from the distribution of activation energies for the passivation and depassivation reactions, so that only 60% of Ge P_b's are passivated in typical conditions, whereas 99.98% of Si P_b's are passivated for the Si/SiO_2 interface, because of a more favourable set of kinetic parameters. If the Ge parameter distribution could be narrowed, then the Ge system could also be better passivated (eg by flatter interfaces).

The structure of atomic defects at the $Ge:GeO_2$ interface may be more complicated than at the $Si:SiO_2$ interface. The simplest defect is the O vacancy. But this defect can also re-arrange to form a valence alternation defect, with a 3-fold Ge site and a 3-fold O site, as noted by Broqvist [354] and Li [355]. Both these defect sites give gap states. The 3-fold Ge site gives a state just below the Ge VB edge, and the 3-fold O site gives a state localised on adjacent Ge sites that lies just above the Ge conduction band, as shown in Fig 82. Zhang [361] has noticed that carrier localisation in these resonant states lowers the field effect mobility in nFET and pFET below there expected values.

8.3 ALD on Ge

The study of ALD high-k dielectrics on Ge has been underway for several years [356]. It is found that direct contact of Ge with a high-k dielectric results in inferior electrical behavior due to interface state generation resulting in mobility degradation [357,358]. As a result, Caymax [359] investigated using a thin SiO_2 (k=3.9), GeO_2 (K=5.2-5.8) or GeON (K~6.0) layer between the high-K and Ge substrate. From a scaling perspective, it would be desirable to minimize a low-K dielectric in the gate stack [2], and so the most recent work has emphasized avoiding the introduction of a thin Si layer at the interface resulting in relatively low-K SiO_2 formation.

Recent studies of an ALD process on the GeO_x surface have shown that the various oxidation states of Ge undergo a reaction with trimethyl-aluminum (TMA) [360]. This so-called "clean-up" effect, observed originally on III-V substrates, severely reduces surface oxides. As seen in Fig. 83, a Ge(100) surface etched with de-ionized water results in a surface with various Ge oxidation states. Exposing this surface to the ALD reactor vacuum ambient causes further surface oxidation. However, the oxides are immediately reduced upon exposure to the first ALD precursor pulse, TMA. Subsequent water and TMA exposures result in a gradual reduction of the GeO_x. Similar results are seen for a clean Ge surface, where the ALD vacuum ambient causes surface oxide formation again (Fig. 83(b)). These results demonstrate the power of in-situ studies vs. ex-situ analysis, and furthermore present a contrast to entirely UHV studies, where the initial oxidation always present in a commercial ALD tool is absent.

Fig 83 shows the corresponding ex-situ XPS of the interface formed from the post-ALD plasma oxidation process with substantial concentrations of the Ge^{+3} oxidation state observed. A correlation of the extracted D_{it} with GeO_x thickness indicates the Ge^{+3} state is correlated with lower D_{it} values and thus better interface passivation (Fig. 83(b)). A minimum GeO_x thickness for sufficient device passivation of 0.5 nm is also noted. Other work by Zhang et al [361-364] examining the effects of plasma oxidation of the Ge surface *prior* to ALD indicate a somewhat higher D_{it} level is detected, particularly as the GeO_x is thinned below 2.7nm. This degradation was attributed to "ALD damage", i.e. reactions of the GeO_x layer during the subsequent ALD process.

An alternative approach for Ge interface passivation is to use ozone oxidation at 400°C prior to ALD of Al_2O_3 [363].

Alternative interfacial layers have also been investigated previously, such as GeON integrated with high-k dielectrics [364-367]. Fig. 83(c) shows that in-situ studies of the GeON/Ge interface is relatively robust compared to the GeO_2/Ge interface as far as reactions with the TMA precursor are concerned [358]. It is seen that the interfacial chemistry is minimally affected upon exposure to the TMA/H_2O process and likely due to the strong oxynitride bonding. However, electrical characterization indicates that a somewhat higher D_{it} for an ALD HfO_2 dielectric on GeON after a forming gas anneal (370 °C, 30min.) was recently reported [367], compared to that noted above for a GeO_x interface with Al_2O_3. Therefore, recent work appears to emphasize work on engineered GeO_2 as noted above, with the ALD high-k dielectric in place before exposure to the post-deposition oxidation process. Sulfur passivation of Ge using H_2S in conjunction with ALD is also a useful factor [368-371].

Recently, fundamental studies of Al ALD on atomically clean Ge has been investigated by Kummel [372] using in-situ dosing, STM and XPS analysis in conjunction with first-principles calculations. TMA was exposed to the Ge surface at 5×10^{-9} Torr at room temperature to result in a near-saturation exposure of 10000 L, resulting in a coverage of 0.8 monolayers (ML) of the adsorbed species according to STM imaging. The actual coverage of Al on the surface is estimated to be ~20% of the surface, based on in-situ XPS measurements, and likely results from steric effects of the methyl ligands. Some ordering of the adsorbed species is observed by STM, and a dissociation of TMA to form a dimethyl-Al (DMA) and mono-methyl (MMA) complex on the Ge dimer is posited to be the stable structure at room temperature. Subsequent annealing of the TMA dosed surface to 250°C under UHV results in a decrease in surface carbon concentration while the Al surface concentration remains constant, with the formation of volatile C_2H_6 and CH_4 species suggested as the principle reaction channels. An adsorbed species coverage of 0.4 ML is reported. Further annealing to 450°C under UHV again results in

a further reduction in the detected C surface concentration to ~20%, while the Al concentration remained constant at ~20%, and an adsorbed species coverage of 0.15ML. The remaining C is suggested to be present as remaining DMA and MMA species.

In comparison to reactions from using a standard ALD tool, where the precursor is entrained in flowing N_2, reactor pressures ~ 7 Torr are utilized with pulse times ~0.1 s, corresponding to exposures of the TMA (and H_2O) on the order of 10^6 L are employed [358]. In addition, the Ge surface is not typically atomically clean, but likely has a native or chemical oxide on the surface initially (or upon exposure to the ALD reactor ambient), as seen in Fig. 84. So the correlation to the reactions under actual ALD conditions remain to be mapped out, although such UHV studies certainly points toward important reaction channels. In this regard, Lee et al [372] have examined Ge surfaces saturated with H_2O (~10^6 L) followed by TMA exposure (~60,000 L). An enhanced reaction of the TMA with the hydroxylated surface is observed, as expected, with somewhat higher Al concentrations (~ 40%) detected on the surface.

Advanced Ge stacks and Device performance

A way to minimise the O diffusion problem that creates interfacial defects is to use a very thin Al_2O_3 diffusion barrier layer. A good Ge/GeO_2 interface has perhaps given the lowest interface state density. A very thin Al_2O_3 layer is deposited on top of this. O diffusion through the Al_2O_3 is small so this suppresse s any outward O vacancy diffusion that would cause an interfacial reaction [374]. Zhang [359-361] created this type of stack by depositing Al_2O_3 and then sub-cutaneously oxiding the Ge by a room temperature oxygen plasma (Fig 85). This appears to provide substantial passivation of interfacial defects, and promising electrical results. A reduction of the interface state density (D_{it}) from the 10^{12} $cm^{-2}eV^{-1}$ to as low as 5×10^{10} $cm^{-2}eV^{-1}$ have been reported for capacitors. HfO_2 can be deposited on top of this to complete the gate stack if necessary. A thicker Al_2O_3 layer is to be avoided as this has a higher defect density. Han [380] has found that a nitrogen plasma on the Al_2O_3 can further lower D_{it}.

Fig 86 compares Ge MOSFET field effect mobilties. Shang [320] achieved an electron mobility of 100 cm2/V.s for 8 nm EOT in 2004. Toriumi used the high pressure/lowe pressure annealing technique to inhibit interface defects and achieved an electron mobility of 1100 cm2/V.s in 2009 for an unknown EOT. The Al_2O_3 diffusion barrier method allowed Zhang [359] to achieve electron mobilities of up to 937 cm2/V.s on EOTs of 1.1 nm and electron mobility of 754 cm2/V.s for an EOT of 0.82 nm.

This approach has allowed a reduction of the interface state density (D_{it}) from the 10^{12} $cm^{-2}eV^{-1}$ to as low as 5×10^{10} $cm^{-2}eV^{-1}$ to be reported for capacitors, a corresponding peak mobility of 437 cm^2/Vs was reported for pMOS transistors fabricated on Ge(100) [361].

It is noted that high inversion carrier concentration (high field) mobilities are also substantially (x2) higher than the unoxidized Al_2O_3/Ge stack, and much higher (~4×) that for the Si "universal" mobility curve. Further work on nMOS Ge devices also appears promising, with peak mobilities of 937 cm^2/Vs reported [359].

These results generally indicate that an engineered GeO_2 layer, with attention to the sequence of the plasma oxidation process, may provide a useful route to controlling the interfacial defect states. Further work is needed to optimize the gate dielectric properties, as border traps are detected in the films. Interfaces between the dielectrics (e.g. GeO_2/Al_2O_3) appear to be a focus of this research as well.

8 Summary

This paper has reviewed the materials chemistry, bonding and electrical behaviour of oxides needed to replace SiO_2 as the gate oxide in CMOS devices. The new oxides must satisfy six conditions to be acceptable as gate dielectrics, a high enough K value, thermal stability, kinetic stability, band offsets, good interface quality with Si, and low bulk defect density. HfO_2 and Hf silicate have emerged as the preferred oxides. The necessary deposition and processing to produce working devices has been achieved. However, the oxides need to be optimised substantially further, in order to achieve high performance devices. This requires improvement of flat band voltage and lower defect densities. The main defects in

the oxides are oxygen vacancies and interstitials. Oxygen vacancies are the largest problem as they give rise to defect levels close to the Si conduction band. Flat band voltage instability is due to electron trapping at the O vacancy. Mobility degradation is largely due to remote charge scattering by charged defects or soft phonons in the oxide. DC flat band voltage shifts tend to be due to interaction and reaction of the gate electrode and the high K oxide.

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References

1. M T Bohr, R S Chau, T Ghani, K Mistry,' The high-k solution', IEEE Spectrum 44 29 (2007)
2. G Wilk, R M Wallace, J M Anthony, J App Phys **89** 5243 (2001)
3. A I Kingon, A I Kingon, J P Maria, S K Streiffer, Nature **406** 1032 (2000)
4. R M Wallace, G Wilk, eds, MRS Bulletin 27 (March 2002)
5. J Robertson, Euro Phys J Appl Phys **28** 265 (2004)
6. M Houssa, 'High K Gate oxides', IOP, London (2003)
7. A A Demkov, A Navrotsky, 'Gate oxides', Kluwer, Amsterdam (2004)
8. H Huff, D Gilmer, 'Gate oxides', Springer, Berlin, (2004)
9. J Robertson, Rep Prog Phys **69** 327 (2006)
10. E P Gusev, V Narayanan, M M Frank, IBM J Res Dev 50 387 (2006)
11. M Ieong, V Narayanan, D Singh, A Topol, V Chan, Z Ren, Materials Today 9 26 (June 2006)
12. B H Lee, J Oh, H H Tseng, R Jammy, H Huff, Materials Today 9 32 (June 2006)
13. B H Lee, S C Song, P Kirsch, IEEE Trans ED **55** 8 (2008)
14. S H Lo, D A Buchanan, Y Taur, W Wang, IEEE ED Lett **18** 209 (1997)
15. K Mistry, C Allen, C Auth, B Beattie, D Bergstrom, M Bost, M Buehler, A Cappelani, R Chau, C H Choi, G Ding, K Fischer, T Ghani, R Grover, W Han, D Hanken, M Hattendorf, J He, J Hicks, D Huessner, D Ingerley, P Jain, R James, L Jong, S Joshi, C Kenyon, K Kuhn, K Lee, H Liy, B McIntyre, P Moon, J Neiynck, C Parker, D Parsons, L Pipes, M Prince, P Ranade, T Reynolds, J Sandford, L Schifren, J Sebastian, J Seiple, D Simon, S Sivakumar, P Smith, C Thomas, T Troeger, P Vanderyoon, S Williams, K Zawadzi, IEEE IEDM Tech Digest (2007) p10.2;
16. M Chudzik, B Doris, R Mo, J Sleight, E Cartier, C Dewan, D Park, H Bu, W Natzle, W Yan, .. M Khae, T C Chen, Tech Digest VLSI (IEEE, 2007) p194
17. E P Gusev, D A Buchanan, E Cartier, A Kumar, S Guha, A Callegari, S Zafar, P C Jamison, D A Neumayer, M Copel, M A Gribelyuk, H Okorn-Schmidt, C D'Emic, P Kozlowski, K Chan, N Bojarczuk, L A Ragnarsson, P Ronsheim, K Rim, R J Fleming, A Mocuta, A Ajmera, Tech Digest - IEDM (2001a) p455
18. J Koomen, Solid-State Electronics, **16** 801 (1973)
19. C G Sodini, T W Ekstedt, J L Moll, Solid-State Electronics, **25** 833 (1982)
20. J Robertson, J Vac Sci Technol B **18** 1785 (2000)
21. H J Hubbard, D G Schlom, J Mater Res **11** 2757 (1996);
22. D G Schlom, J H Haeni, MRS Bull **27** 198 (2002)
23. M Copel, M Gribelyuk, E Gusev, App Phys Lett **76** 436 (2000)
24. M Gutowski, J E Jaffe, C L Liu, M Stoker, R I Hegde, R S Rai, P J Tobin, App Phys Lett **80** 1897 (2002)
25. Y H Wu, M Y Yang, A Chin, W J Chen, C M Kwei, IEEE ED Lett **21** 341 (2000)
26. H Iwai, et al, Tech Digest IEDM (IEEE, 2002); M K J Okamoto, H Iwai, proc ESSDERC (2007) p199
27. J Kwo et al, App Phys Lett **77** 130 (2000)
28. A Fissel, H J Osten, E Bugiel, J Vac Sci Technol B 21 1765 (2003)
29. G D Wilk, R Wallace, J M Anthony, J App Phys 87 484 (2000)
30. J-F Damlencourt, et al, Solid-State Elec **47**, 1613 (2003).
31. G. Bersuker, et al, J. Appl. Phys. **100**, 094108 (2006).
32. M P Agustin, G Bersuker, B foran, L A Boatner, S Stemmer, J App Phys **100**, 024103 (2006)
33. A Deshpande, R Inman, G Jurisch, C.G.Takoudis J App Phys **99**, 094102 (2006)
34. C. Maunoury, et al, J App Phys **101**, 034112 (2007)
35. M T Ho, R T Brewer, L S Wiehlunski, Y J Chabal, N Moumen, M Boleslawski, App Phys Lett 87 133103 (2005)
36. P E Batson, Microsc Microanal **11**(Suppl 2) 2164 (2005).

37. D. Schmeisser, F Zheng, F J Himpsel, H J Engelmann, E. Zschech, MRS Symp Proc, **917**, E10-02 (2006)
38. P-G Mani-Gonzalez, M-O Vazquez-Lepe, F Espinosa-Magaña, A Herrera-Gomez, J. Vac. Sci. Technol A **31**, 010601 (2013)
39. J Robertson, C W Chen, App Phys Lett **74** (1999) 1168
40. X Zhang, A Demkov, L Hao, X Hu, Y Wei, J Kulik, Phys Rev B 68 125323 (2003)
41. E P Gusev, E Cartier, D A Buchanan, M Gribelyuk, M Copel, Microelec Eng **59** 341 (2001b)
42. S Guha, E Cartier, N A Bojarczuk, J Bruley, L Gignac, J Karasinski, App Phys Lett **90** 512 (2001)
43. S Guha, E P Gusev, H Okorn-Schmidt, L A Ragnarsson, N A Bojarczuk, App Phys Lett 81 2956 (2002)
44. W Tsai, et al (IMEC) Tech Digest IEDM (2003) paper 13.2
45. Y C Yeo, T J King, C Hu, App Phys Lett **81** 2091 (2002)
46. M R Visokay, J J Chambers, A L P Rotondaro, A Shanware, L Colombo, App Phys Lett **80** 3183 (2002)
47. R M Wallace, R A Stoltz, G D Wilk, US Pat. Nos. 6013553; 6020243 (2000); US Pat. Nos. 6291866; 6291866 (2001)
48. B H Lee, L Kang, R Nieh, W J Qi, J C Lee, App Phys Lett **76** 1926 (2000)
49. H Kim, P C McIntyre, C O Chui, K C Saraswat, S. Stemmer, J Appl Phys **96** 3467 (2004)
50. J Morais et al, App Phys Lett **81** 2995 (2002); **79** 4192 (2001)
51. M A Quevedo-Lopez, et al, App Phys Lett **81** 1074 (2002);
52. M A Quevedo-Lopez, et al, App Phys Lett **82** 4669 (2003)
53. R M C de Almeida, I J R Baumvol, Surf Sci Rep 49 1 (2003)
54. B W Busch, O Pluchery, Y J Chabal, D A Muller, R Opila, D A Muller, J R Kwo, E Garfunkel, Mat Res Soc Bull (March 2002) p206
55. S Ferrari, G Scarel, J App Phys **96** 144 (2004)
56. F J Himpsel, F R McFeely, A Taleb-Ibrahami, J A Yarnoff, G Hollinger, Phys Rev B 38 6084 (1988);
57. J W Keister et al, J Vac Sci Technol B 17 1250 (1999)
58. E H Poindexter, P J Caplan, Prog Surf Sci **14**, 201 (1983)
59. R E Mikawa, P M Lenahan, J App Phys **59**, 2054 (1986)
60. A Stesmans, Appl Phys Lett **68**, 2723 (1996a); *ibid.* **68**, 2076 (1996b)
61. A Stesmans, V V Afanasev, Phys Rev B57 10030 (1998)
62. C Hobbs et al, VLSI Symp (2003) p9
63. D C Gilmer et al, Microelectron Eng **69** 138 (2003)
64. C Hobbs et al, IEEE Trans ED **51** 971 (2004); **51** 978 (2004)
65. R Chau, J Brask, S Datta, G Dewey, M Doczy, B Doyle, J Kavalieros, M Radosavljevic, Microelectronic Eng **80** 1 (2005)
66. K Xiong, P W Peacock, J Robertson, App Phys Lett 86 012904 (2005)
67. M M Frank, Proc ESSDERC (2011)
68. J E Mahan, *Physical Vapor Deposition of Thin Films,* Wiley-Interscience (2000).
69. J L Vossen, W Kern, *Thin Film Processes*, Academic Press (1978); (1991)
70. J P Lehan, T Mao, B G Bovard, H A Macleod, Thin Sol Films **203**, 227 (1991)
71. H Harris, K Choi, N Mehta, A Chandolu, N Biswas, G Kipshidze, S Nikishin, S Gangopadhyay, H Temkin, App Phys Lett **81** 1065 (2002)
72. K Choi, H Temkin, H Harris, S Gangopadhyay, L Xie, M White, App Phys Lett **85**, 215 (2004)
73. M Ritala, in 'High K gate dielectrics' ed M Houssa, (Inst Physics, Bristol, UK 2004)
74. M Ritala, K Kukli, A Rahtu, P I Raisanen, M Leskela, Science 288 319 (2000)
75. S M George, Chem Rev 110 111 (2010)
76. A C Jones, P R Chalker, J Phys D 36 R80 (2003)
77. M L Green, M Y Ho, B Busch, G D Wilk, T Sorsch, T Conard, B Brijs, W Vandervorst, P I Raisanen, D A Muller, M Bude, J Grazul, J App Phys 92 7168 (2002)

78. L A Ragnarrson, N A Bojarczuk, J Karaninski, S Guha, IEEE ED Let **24** 689 (2003)
79. M M Frank, Y J Chabal, G D Wilk, App Phys Lett **82** 4758 (2003)
80. M M Frank, Y J Chabal, M L Green, A Delabie, B Brijs, G D Wilk, M Y Ho, I J R Baumvol, App Phys Lett **83** 740 (2003)
81. D M Hausmann, E Kim, J Becker, R G Gordon, Chem Mat 14 4350 (2002)
82. D M Hausmann, R G Gordon, J Crystal Growth, 249 251 (2003)
83. J S Becker, E Kim, R G Gordon, Chem Mats 16 3497 (2004); B S Lim, A Rahtu, R G Gordon, Nature Mats 2 749 (2003)
84. T Q Ngo, A Posadas, M D McDaniel, D A Ferrer, J Bruley, C Breslin, A A DEmkov, J G Ekerdt, J Crystal Growth 363 150 (2013); X Wang, L Dong, J Zhang, Y Liu, P D Ye, R G Gordon, Nanoletts 13 594 (2013)
85. G B Rayner, D Kang, G Lucovsky, J Vac Sci Technol B **21** 1783 (2003)
86. J P Maria, D Wicaksana, A I Kingon, B Busch, H Schulte, E Garfunkel, T Gustafsson, J App Phys **90** 3476 (2001)
87. S Stemmer, Y Li, B Foran, P S Lysaght, S K Streiffer, P Fuoss, S Seifert, App Phys Lett **83** 3141 (2003)
88. H Kim, P C McIntyre, J App Phys **92** 5094 (2002)
89. S Stemmer, Z Chen, C G Levi, P S Lysaght, B Foran, J A Gisby, J R Taylor, Jpn J App Phys **42** 3593 (2003)
90. C Zhao, O Richard, E Young, H Bender, G Roebben, S Haukka, S DeGendt, M Houssa, R Carter, W Tsai, O Van der Biest, M Heyns, J Non-Cryst Solids **303** 144 (2002)
91. S Stemmer, J Vac Sci Technol B **22** 791 (2004)
92. V Naraynan, S Guha, M Copel, N A Bojarczuk, P L Flaitz, M Bribelyuk, App Phys Lett **81** 4183 (2002)
93. T Ando, et al, Tech Digest IEDM (2009); T Ando, et al, Tech Digest IEDM (2011);
94. T Ando, Materials 5 478 (2012)
95. T Ando, M Copel, J Bruley, M M Frank, H Watanabe, V Narayanan, App Phys Lett 96 132904 (2010)
96. M M Frank, E A Cartier, T Ando, S W Bedell, J Bruley, Y Zhu, V Narayanan, ECS Solid Letters 2 N8 (2013)
97. T Ando, B Kannan,. U Kwon, W L Lai, B P Linder, E A Cartier, R Haight, M Copel, JBruly, S A Krishnan, V Narayanan, Tech Digest VLSI Technol (2014) p6.1.
98. M.Copel, E Cartier, F M Ross, App Phys Lett **78** 1607 (2001)
99. M Copel, E Cartier, V Narayanan, M C Reuter, S Guha, N Bojarczuk, App Phys Lett **81** 4227 (2002)
100. H S Kim, P C McIntyre, C O Cui, K C Saraswat, S Stemmer, J App Phys 96 3467 (2004)
101. H Watanabe, M Saitoh, N Ikarashi, T Tatsumi, App Phys Lett **85** 449 (2004)
102. H Shimizu, K Kita, K Kyuno, A Toriumi, Jap J App Phys **44** 6131 (2005)
103. P W Peacock, J Robertson, J App Phys **92** 4712 (2002)
104. J H Choi, Y Mao, J P Chang, Mat Sci Eng R 72 97 (2011)
105. R. H. French, J Am Ceram Soc **73** 477 (1990)
106. P Lamparter, R Kniep, Physica B **234** 405 (1997)
107. H Momida, T Hamada, Y Takagi, T Yamamoto, T Uda, T Ohno, Phys Rev B **73** 054108 (2006)
108. V V Afanaev, A Stesmans, J App Phys 102 081301 (2007)
109. D Liu, J Robertson, App Phys Lett 94 042904 (2009)
110. R H French, S J Glass, F S Ohuchi, Y N Xu, W Y Ching, Phys Rev B **49** 5133 (1994)
111. J E Medvedeva, A J Freeman, C B Geller, D M Rishel, Phys Rev B 76 235115 (2007)
112. H S Lee, S J Clark, J Robertson, Phys Rev B 86 075209 (2012)
113. G Lucovsky, Y Zhang, J L Whitten, D G Schlom, J L Freeouf, Microelec Eng **72** 288 (2004)
114. G M Rignanese, X Gonze, A Pasquarello, Phys Rev B **63** 104305 (2001)
115. K Xiong, Y Du, K Tse, J Robertson, J App Phys 101 024101 (2007)

116. P Broqvist, A Pasquarello, App Phys Lett 90 082907 (2007)
117. J Morais, L Miotti, K P Bastos, S R Teixeira, I J R Baumvol, A L P Rotondaro, J J Chambers, M R Visokay, L Colombo, M C MartinsAlves, App Phys Lett **86** 212906 (2005)
118. C A Pignedoli, A Curioni, W Andreoni, Phys Rev Lett 98 037602 (2007)
119. H Kato, T Nango, T Miyagawa, T Katagiri, K S Seol, Y Ohki, J App Phys **92** 1106 (2002)
120. K Xiong, J Robertson, S J Clark, App Phys Lett 89 022907 (2006)
121. S G Lim, S Kriventsov, T N Jackson, J H Haeni, D G Schlom, A M Balbashov, R Uecker, P Reiche, J L Freeouf, G Lucovsky, J App Phys **91** 4500 (2002)
122. D G Schlom, S Datta S Guha, MRS Bull (Nov 2008)
123. M Sousa, C Rossel, C Marchiori, H Siegwart, D Caimi, J P Locquet, D J Webb, R Germann, J Fompeyrine, K Babich, J W Seo, C Diker, J App Phys 102 104103 (2007)
124. K Xiong, J Robertson, M C Gibson, S J Clark, App Phys Lett **87** 183505 (2005)
125. J Robertson, K Xiong, S J Clark, Phys Stat Solidi B 243 2054 (2006)
126. A Alkauskas, P Broqvist, F Devynck, A Pasquarello, Phys Rev Lett 101 106802 (2008)
127. P Broqvist, A Pasquarello, App Phys Lett 89 082908 (2006)
128. B Kralik, E K Chang, S G Louie, Phys Rev B **57** 7027 (1998)
129. J Drabowski, V Zavodinsky, A Fleszar, Microelect Reliab **41** 1093 (2001)
130. X Zhao, D Vanderbilt, Phys Rev B **65** 233106 (2002)
131. G M Rignanese, X Gionze, G Jun, K J Cho, A Pasquarello, Phys Rev B **69** 184301 (2004)
132. P Delugas, V Fiorentini, A Filippetti, Phys Rev B **71** 134302 (2005)
133. J Robertson, J App Phys 104 123111(2008)
134. R D Shannon, J App Phys 73 348 (1993)
135. R Hegde, et al, Tech Digest IEDM (2005) p59
136. R I Hegde, D H Triyoso, S B Samavedam, B E White, J App Phys 101 074113 (2007)
137. D H Triyoso, R I Hegde, J K Schaeffer, J Vac Sci Technol B 25 845 (2007)
138. K Tomida, K Kita, A Toriumi, App Phys Lett 89 142902 (2006)
139. D Tsoutsou, G Apostopoulos, S F Galata, P Tsipas, A Sotiropoulos, G Mavrou, Y Panayiotatos, A Dimoulas, A Lagoyannis, A G Karydas, V Kantarelou, S Harrissopoulos, J App Phys 106 024107 (2009)
140. P Li, I W Chen, J E Penner-Hahn, J Am Ceram Soc **77** 118 (1991)
141. J P Goff, W Hayes, S Hull, M T Hutchings, K N Clausen, Phys Rev B **59** 14202 (1999)
142. G Stapper, M Bernasconi, N Nicoloso, M Parrinello, Phys Rev B **59** 797 (1999)
143. D Fischer, A Kersch, App Phys Lett 92 012908 (2008)
144. C K Lee, E Cho, H S Lee, C S Hwang, S Han, Phys Rev B 78 012102 (2008)
145. L F Edge, D G Schlom, S A Chambers, E Cicerrella, J L Freeouf, B Hollander, J Schubert, App Phys Lett **84** 726 (2004)
146. L F Edge, D G Schlom, P Sivasubramani, R M Wallace, B Hollander, J Schubert, App Phys Lett 88 112907 (2006)
147. J M J Lopes, M Roekerath, T Heeg, E Rije, J Schubert, S Mantl, V V Afanasev, S Shamuilia, A Stesmans, Y Jia, D G Schlom, App Phys Lett **89** 222902 (2006)
148. J M J Lopes, M Roekerath, T Heeg, U Littmark, J Schubert, S Mantl, Y Jia, D G Schlom, Microelec Eng **84** 1890 (2007)
149. J Schubert, O Trithaveesak, W Zander, D G Schlom, App Phys A 90 577 (2008)
150. M Wagner, et al, App Phys Lett 88 172901 (2006)
151. R Thomas, et al, App Phys Lett 89 232902 (2006)
152. A Laha, H J Osten, A Fissel, App Phys Lett 90 113508 (2007)
153. E D Ozban, J Lopes, M Roeckerath, D G Schlom, J Schubert, S Mantl, App Phys Lett **93** 052902 (2008)
154. K Xiong, J Robertson, App Phys Lett 95 022903 (2009)
155. S A Shevlin, A Curioni, W Andreoni, Phys Rev Lett **94** 146401 (2005)
156. E Bonera, G Scarel, M Fanciulli, P Delugas, V Fiorentini, Phys Rev Lett **94** 027602 (2005)

157. A Baldereschi, A Baroni, R Resta, Phys Rev Lett **61** 734 (1988)
158. C G van de Walle, Phys Rev B **39** 1871 (1989)
159. R T Tung, Phys Rev Lett **84** 6078 (2000); R T Tung, Phys Rev B **64** 205310 (2001)
160. W Mönch, Phys Rev Lett **58** 1260 (1987)
161. W Mönch, Surface Sci **300** 928 (1994)
162. J Tersoff, Phys Rev Lett **52** 465 (1984)
163. A W Cowley, S M Sze, J App Phys **36** 3212 (1965)
164. J Robertson, Tech Digest IEDM (2009); App Phys Lett 94 152104 (2009)
165. J Robertson, J Vac Sci Technol A 31 050821 (2013)
166. S A Chambers, Y Liang, Z Yu, R Dropad, J Ramdani, K Eisenbeiser, App Phys Lett **77** 1662 (2000)
167. R Ludeke, M T Cuberes, E Cartier, App Phys Lett **76** 2886 (2000)
168. D J Maria, J App Phys **45** 5454 (1974)
169. V V Afanasev, M Houssa, A Stesmans, M M Heyns, App Phys Lett **78** 3073 (2001)
170. V V Afanasev, M Houssa, A Stesmans, M M Heyns, J App Phys **91** 3079 (2002)
171. V V Afanasev, A Stesmans, F Chen, X Shi, S A Cambell, App Phys Lett **81** 1053 (2002)
172. V. V. Afanesev, A. Stesmans, M. Passlack, and N. Medendrop, App Phys Lett **85** 597 (2004)
173. S Sayan, E Garfunkel, S Suzer, App Phys Lett **80** 2135 (2002)
174. G B Rayner, D Kang, Y Zhang, G Lucovsky, J Vac Sci Technol B **20** 1748 (2002)
175. Oshima, S Toyoda, T Okumura, J Okabayashi, H Kumigashira, App Phys Lett **83** 2172 (2003)
176. O. Reynault, N T Barrett, D Samour, S Quiais-Marthon, Surface Sci **566** 526 (2004)
177. C C Fulton, R J Nemanich, J App Phys **96** 2665 (2004)
178. T Hattori, T Yosihda, T Shiraishi, K Takahashi, H Nohira, S Joumori, K Nakajima, M Suzuki, K Kimura, I Kashiwagi, C Ohshima, S Ohmi, H Iwai, Microelect Eng **72** 283 (2004)
179. S Miyazaki, J Vac Sci Technol B **19** 2212 (2001)
180. G Seguini, E Bonera, S Spiga, G Scarel, M Fanciulli, App Phys Lett 85 5316 (2004)
181. V. V. Afanasev, A Stesmans, D Droopad, App Phys Lett 89 092103 (2006)
182. A Ohta, M Yamaoka, S Miyazaki, Microelectr Eng **72** 154 (2004)
183. J W Keister et al, J Vac Sci Technol B **17** 1831 (1999)
184. J L Alay, M Hirose, J App Phys **81** 1606 (1997);
185. J Robertson, B Falabretti, J App Phys 100 014111 (2006)
186. V V Afanasev, M Badylevich, A Stesmans, App Phys Lett 93 212104 (2008)
187. V Fiorentini, G Gulleri, Phys Rev Lett **89** 266101 (2002)
188. A Fissel, J Dabrowski, H J Osten, J App Phys **91** 8986 (2002)
189. P W Peacock, J Robertson, Phys Rev Letts **92** 057601 (2004)
190. P W Peacock, K Xiong, K Tse, J Robertson, Phys Rev B 73 075328 (2006)
191. C J Forst, C Ashman, K Schwarz, P E Blochl, Nature **427** 56 (2004)
192. S J Wang, C K Ong, App Phys Lett **80** 2541 (2002)
193. Y F Dong, Y P Feng, S J Wang, A C H Huan, Phys Rev B **72** 045327 (2005)
194. Y F Dong, S J Wang, J W Chai, Y P Feng, A C H Huan, App Phys Lett **86** 132103 (2005)
195. Y F Dong, S J Wang, Y P Feng, A C H Huan, Phys Rev B **73** 045302 (2006);
196. R Puthenkovilakam, E A Carter, J P Chang, Phys Rev B **69** 155329 (2004)
197. J Garavin, L Fonseca, G Bersuker, A L Shluger, Microelectronic Eng **80** 412 (2005)
198. P Broqvist, A Pasquarello, Microelec Eng 84 2022 (2007);
199. J Robertson, Solid State Electronics 49 283 (2005)
200. A S Foster, V B Sulimov, F L Gejo, A L Shluger, R N Nieminen, Phys Rev B **64** 224108 (2001)
201. A S Foster, F L Gejo, A L Shluger, R N Nieminen, Phys Rev B **65** 174117 (2002)
202. K Xiong, J Robertson, J App Phys 99 044105 (2006)
203. K Torii, K Shirashi, S Miyazaki, K Yamabe, M Boero, T Chikyow, K Yamada, H Kitajima, T Arikado, Tech Digest IEDM (2004) p129
204. J Kang, E C Lee, K J Chang, Y G Jin, App Phys Lett **84** 3894 (2004)

205. W L Scopel, A J R da Silva, W Orellana, A Fazzio, App Phys Lett 84 1492 (2004)
206. Y. P. Feng, A T L Lim, and M F Li, App Phys Lett **87** 062105 (2005)
207. M Ikeda et al, Mat Res Soc Symp Proc 786 E5.4 (2004)
208. D M Ramo, A L Shluger, J L Gavartin, Phys Rev Lett 99 155504 (2007)
209. J X Zheng, G Ceder, W K Chim, Phys Stat Solidi RRL 2 227 (2008)
210. C Tang, R Ramprasad, PRB 81 161201 (2010)
211. J L Gavartin, D M Ramo, A L Shluger, G Bersuker, App Phys Lett 89 082908 (2006)
212. E A Choi, K J Chang, App Phys Lett 94 122901 (2009)
213. J L Lyons, A Janotti, C G Van de Walle, Microelec Eng 88 1452 (2011)
214. J Robertson, S J Clark, Phys Rev B 83 075205 (2011)
215. A Y Kang, P M Lenahan, J F Conley, App Phys Lett **83** 3407 (2003)
216. G Bersuker, P Zeitzoff, G Brown, H R Huff, Mats Today 7 (Jan 2004) p26
217. S Zafar, A Callegari, E Gusev, M V Fischetti, J App Phys **93** 9298 (2003)
218. A Kerber, E Cartier, L Pantisano, R Degraeve, T Kauerauf, Y Kim, G Groeseneken, H E Maes, U Schwalke, IEEE ED Lett **24** 87 (2003)
219. J. Mitard, C. Leroux, G. Ghibaudo, G. Reimbold, X. Garros, B. Guillaumot, and F. Boulanger, Microelectronic Eng **80** 362 (2005)
220. E A Cartier, B P Linder, V Narayanan, V K Paruchuri, Tech Digest IEDM (2006)
221. W He, T P Ma, App Phys Lett **83** 5461 (2003)
222. E P Gusev, C P D'Emic, App Phys Lett **83** 5223 (2003)
223. H Takeuchi, D Ha, T J King, J Vac Sci Technol A 22 1337 (2004)
224. N V Nguyen, A V Davydov, D Chandler-Horowitz, M MM Frank, App Phys Lett **87** 192903 (2005)
225. SA Walsh, L Fang, J K Schaffer, E Weisbrod, L J Brillson, App Phys Lett 90 052901 (2007)
226. S Guha, Phys Rev Let 98 196101 (2007)
227. S Guha, P Solomon, App Phys Lett 92 012909 (2008)
228. C Ko, M Shandalov, P C McIntyre, S Ramanathan, App Phys Lett 97 082102 (2010)
229. S Zafar, H Jagannath, L F Edge, D Gupta, App Phys Lett 98 152903 (2011)
230. A Stesmans, V V Afanas'ev, Appl Phys Lett **80**, 1957 (2002)
231. A Stesmans, V V Afanasev, App Phys Lett **82** 4074 (2003)
232. R C Barklie, S Wright, J Vac Sci Technol B 27 317 (2009)
233. R Gillen, S J Clark, J Robertson, App Phys Lett (2012)
234. M Houssa, V V Afanasev, A Stesmans, M M Heyns, App Phys Lett **77** 1885 (2000)
235. H S Kim, P C McIntyre, K C Saraswat, App Phys Lett 82 106 (2003)
236. N Umezawa, K Shiraishi, T Ohno, H Watanabe, T Chikyow, K Torii, K Yamabe, K Yamada, H Kitajima, T Arikado, App Phys Lett **86** 143507 (2005)
237. J L Gavartin, A L Shluger, A S Foster, G I Bersuker, J App Phys **97** 053704 (2005)
238. N Shang, P W Peacock, J Robertson, App Phys Lett 84 106 (2004)
239. N Umezawa, K Shiraishi, App Phys Lett 91 132904 (2007)
240. D Liu, J Robertson, App Phys Lett 94 042904 (2009)
241. H H Tseng, et al, IEDM (2005)
242. P McIntyre, et al, IEDM (2005)
243. K Tse, J Robertson, App Phys Lett 89 142914 (2006); Microelec Eng 84 663 (2007)
244. H Li, Y Guo, J Robertson, App Phys Lett 104 192904 (2014)
245. J R Weber, A Janotti, C G van de Walle, J App Phys 109 033715 (2011); M Choi, A Janotti, C G Van de Walle, J App Phys 113 044501 (2013)
246. C C Yeh, T P Ma, N Ramasawamy, N Rocklein, D Gealy, T Graettinger, K Min, App Phys Lett 91 113521 (2007)
247. M Specht, M Stadele, S Jakschik, U Schroder, App Phys Lett 84 3076 (2004)
248. R DeGraeve et al, Tech Digest IEDM (2008) p353
249. X F Zheng et al, Tech Digest (2009) p139

250. K Xiong, J Robetson, S J Clark, App Phys Lett 89 022907 (2006); K Xiong, J Robertson, App Phys Lett 95 022903 (2009)
251. H B Michaelson, J App Phys **48** 4729 (1977)
252. Y C Yeo, T J King, C Hu, J App Phys **92** 7266 (2002)
253. M Koyama, Y Kamimuta, T Ino, A Kancko, S Inumiya, K Eguchi, M Takayanagi, A Nishiyama, Tech Digest IEDM (2004) p499
254. S Zafar, et al, Tech Digest VLSI symp (IEEE, 2005) p44
255. J K Schaeffer, C Capasso, L Fonseca, S Samavedam, D Gilmer, Y Liang, O Adetutu, C Hobbs, E Lckowski, R Gregory, Z X Jiang, K Moore, B Y Nguyen, D Roan, B E White, P J Tobin, Tech Digest IEDM (2004), p287
256. J K Schaeffer, L R C Fonseca, S B Samavedam, Y Liang, P J Tobin, B E White, App Phys Lett **85** 1826 (2004)
257. E Cartier, F R McFeely, V Narayanan, P Jamison, M Copel, G Shahidi, Tech Digest VLSI Symp (IEEE, 2005) p15
258. P Majhi et al, presented at MRS (Spring 2005)
259. H C Wen, P Majhi, K Choi, C S Park, H N Alshareef, H R Harris, H Luan, H Miimi, H B Park, G Bersuker, P S Lysaght, D L Kwong, S C Song, B H Lee, R Jammy, Microelec Eng **85** 2 (2008)
260. R Jha, J Gurganos, Y H Kim, R Choi, J Lee, V Misra, IEEE ED Lett **25** 420 (2004); H C Wen, et al, IEEE ED Letts **27** 598 (2006)
261. H H Tseng et al, Tech Digest IEDM (2004) p821
262. J K Schaeffer, C Capasso, R Gregory, D Gilmer, L R C Fonseca, M Raymond, C Happ, M Kottke, S B Samavedam, P J Tobin, B E White, J App Phys **101** 014503 (2007);
263. V Narayanan, V K Paruchuri, N A Bojarczuk, B P Linder, B Doris, Y H Kim, S Zafar, J Stathis, S Brown, J Arnold, M Copel, E Cartier, A Callegari, S Guha, G Shahidi, T C Chen, Tech Digest VLSI symp (IEEE, 2006) p178;
264. V Narayanan, K Maitra, B P Linder, V K Paruchuri, E P Gusev, M M Frank, M L Steen, D LaTulipe, J Arnold, R Carruthers, D L Lacey, E Cartier, IEEE ED Lett 27 501 (2006);
265. K. Tse, J. Robertson, Phys. Rev. Lett. **99** 086805 (2007)
266. K Tse, D Liu, J Robertson, Phys Rev B 81 035325 (2010)
267. P W Tasker, J Phys C **12** 4977 (1979)
268. C Noguera, J Phys Cond Mat **12** R367 (2000)
269. K Shiraishi, K Yamada, K Torii, Y Akasaka, K Nakajima, M Konno, T Chikyow, H Kitajima, T Arikado, Jpn. J. Appl. Phys. **43** L1413 (2004) poly
270. Y Akasaka, G Nakamura, K Shiraishi, N Umezawa, K Yamabe, O Ogawa, K Nakamura, Jpn. J. Appl. Phys. **45** L1289 (2006)
271. J Robertson, O Sharia, A A Demkov, App Phys Lett **91** 132912 (2007)
272. E Cartier, M Hopstaken, M Copel, App Phys Lett 95 042901 (2009)
273. S C Song, C S Park, J Price, R Choi, H H Tseng, B H Lee, R Jammy, IEDM (2007) 13.3
274. K Akiyama, W Wang, W Mizubayashi, M Ikeda, H Ota, T Nabatame, A Toriumi, Tech Digest VLSI (IEEE, 2008) p8.3
275. J Schaeffer, D C Gilmer, S Samevadam, M Raymond, A Haggag, S Kalpat, B Seimie, C Capasso, B E White, J App Phys 102 074511 (2007)
276. G Bersuker, C S Park, H C Wen, K Choi, J Price, P Lysaght, H H Tseng, O Sharia, A Demkov, J T Ryan, P Lenahan, IEEE Trans ED 57 2047 (2010)
277. V Narayanan, V K Paruchuri, N A Bojarczuk, B P Linder, B Doris, Y H Kim, S Zafar, J Stathis, S Brown, J Arnold, M Copel, E Cartier, A Callegari, S Guha, G Shahidi, T C Chen, Tech Digest VLSI symp (IEEE, 2006) p178;
278. S Guha, V K Paruchuri, M Copel, V Narayanan, Y Y Wang, P E Batson, N A Bojarczuk, B Linder, B Doris, App Phys Lett **90** 092902 (2007)

279. H N AlShareef, M Quevedo-Lopez, H C Wen, R Harris, P Kirsch, P Majhi, B H Lee, R Jammy, D J Lichtenwalner, J S Jur, A I Kingon, App Phys Lett **89** 232103 (2006); H N AlShareef, K Choi, H C Wen, H Luan, H Harris, Y Senzaki, P Majhi, B H Lee, R Jammy, App Phys Lett **88** 072108 (2006)
280. H N Alshareef, H F Luan, K Choi, H R Harris, H C Wen, M A Quevedo-Lopez, P Majhi, B H Lee, App Phys Lett **88** 112114 (2006)
281. H J Li, M I Gardner, IEEE ED Letts **26** 441 (2005)
282. X P Wang, M F Li, A Chin, C X Zhu, J Shao, W Lu, X C Shen, X F Yu, R Chi, C Shen, A C H Huan, J S Pan, A Y Du, P Lo, D S H Chan, D L Kwang, Solid State Electronics **50** 986 (2006)
283. Y Yamamoto, K Kita, K Kyuno, A Toriumi, Jpn J App Phys **46** 7251 (2007)
284. K Iwamoto, Y Kamimuta, A Ogawa, Y Watanabe, S Migata, T Nabatame, A Toriumi, App Phys Lett **92** 132907 (2008)
285. P D Kirsch, P Sivasubramani, J Huang, C D Young, M A Quevedo-Lopez, H C Wen, H Alshareef, K Choi, C S Park, B H Lee, H H Tseng, App Phys Lett **92** 092901 (2008)
286. H Jagannathan, V Narayanan, S Brown, Electrochem Soc Trans 16 19 (2008)
287. J K Schaeffer, et al, Microelec Eng 84 2196 (2007)
288. K Kita A Toriumi, App Phys Lett 94 132903 (2009)
289. L Lin, J Robertson, App Phys Lett 95 012906 (2009)
290. L Lin, J Robertson, J App Phys 109 094502 (2011)
291. O. Sharia, A A Demkov, G Bersuker, B H Lee, Phys Rev B **75** 035306 (2008); **77** 085326 (2008)
292. B P Linder, V Narayanan, V K Paruchuri, E Cartier, S Kanakasabapathy, Tech Digest SSDM (Tsukuba, 2007) p16
293. S Takagi, A Toriumi, M Iwase, H Tango, IEEE Trans ED **41** 2357 (1994)
294. L A Ragnarsson, S Guha, M Copel, E Cartier, N A Bojarczuk, J Karasinski, App Phys Lett **78** 4169 (2001)
295. S Guha, N A Bojarczuk, V Narayanan, App Phys Lett **80** 766 (2002)
296. M Hiratani, S Saito, Y Shimamoto, K Torii, Jpn J App Phys **41** 4521 (2002)
297. K Torii et al, Microelectron Eng 65 447 (2003)
298. M V Fischetti, D A Neumayer, E A Cartier, J App Phys **90** 4587 (2001)
299. S Saito, D Hisamoto, S Kimura, M Hiratani, Tech digest IEDM (2003) 33.3
300. W Zhu, J P Han, T P Ma, IEEE Trans-ED **51** 98 (2004)
301. L A Ragnarsson, L Pantisano, V Kaushik, S I Saito, Y Shimamoto, S DeGendt, M Heyns, Tech Digest IEDM (2003) p87
302. Z Ren, M V Fischetti, E P Gusev, E A Cartier, M Chudzik, Tech Digest IEDM (2003) paper 33.2
303. M Casse, L Thevenod, B Guillaumot, L Tosti, F Martin, J Mitard, O Weber, F Andrieu, T Ernst, G Reimbold, T Billon, M Mouis, F Boulanger, submitted to IEEE Trans ED (2005)
304. V Narayanan, K Maitra, B P Linder, V K Paruchuri, E P Gusev, M M Frank, M L Steen, D LaTulipe, J Arnold, R Carruthers, D L Lacey, E Cartier, IEEE ED Lett 27 501 (2006);
305. L A Ragnarsson, et al, Microelec Eng (2011); Tech Digest IEDM (2010)
306. A Kerber, E A Cartier, IEEE Trans Device Mater Reliab 9 147 (2009)
307. E A Cartier, et al, Tech Digest IEDM (2011)
308. B Kaczer et al, Microelec Eng 86 1894 (2010)
309. J Franco et al, Tech Digest IEDM (2010) p4.1
310. J Franco, B Kaczer, P J Roussel, J Mitard, M Cho, L Witters, T Grasser, G Groeseneken, IEEE Trans ED 60 396 (2013)
311. T Ando, E A Cartier, J Bruly, K Choi, V K Narayanan, IEEE EDL 34 729 (2013)
312. A Veloso, et al, Tech Digest VLSI (2011) p 34
313. S Hyun et al, Tech Digest VLSI (2011) p32
314. M Bosi, G Attolini, Prog. Crystal Growth and Charact. Mat. **56** 146 (2010).
315. R Pilarisetty, Nature **479** 324 (2011)
316. S Takagi, IEDM short course (2012)
317. P S Goley, M K Hudait, Materials 7 2310 (2014)

318. Y. Kamata, Materials Today **11**(1-2) 30 (2008)
319. C Claeys, J Mitard, G Hellings, C Eneman, B DeJaeger, L Witters, R Loo, A Delablie, A Sioncke, M Caymax, ECS Trans 54 25 (2013)
320. E Simeon, J Mitard, G Hellings, Mat Sci Semiconductor Proc 15 588 (2012)
321. Q Xie, S Deng, M Schaekers, D Lin, M Caymax, A Delablie, X P Qu, Y L Jiang, D Deduytsche, C Detavernier, Semicond Sci Technol 27 074012 (2012)
322. C O Chui, et al Tech Digest IEDM (2002) p437
323. H L Shang, K L Lee, P Kowlowski, C D'Emic, B E Sikorski, M Ieong, H S P Wong, K Guarini, W E Haensch, IEEE ED Lett 25 135 (2004)
324. A Dimoulas, et al, App Phys Lett 86 032908 (2005)
325. K Kita, S Suzuki, H Nomura, T Takahashi, T Nishimura, A Toriumi, Jpn J App Phys 47 2349 (2008)
326. A Toriumi, T Tabata, C H Lee, T Nishimura, K Kita, K Nagashio, Microelec Eng 86 1571 (2009)
327. C H Lee, T Tabata, T Nishimura, K Nagashio, K Kita, A Toriumi, App Phys Expr **2** 071404 (2009)
328. D Kuzum, T Krishnamohan, A Nainani, Y Sun, P A Pianetta, H S-P Wong, K C Saraswat, IEEE IEDM Tech Digest (2009) 453
329. T Sasada, Y Nakakita, M Takenaka, S Takagi, J App Phys 106 073716 (2009)
330. A Delabie, et al, App Phys Lett 91 082904 (2007)
331. K Kita, S K Wang, M Yoshida, C H Lee, K Nagashio, T Nishimura, A Toriumi, IEDM Tech Digest (2009) p29.6
332. S Wang, K Kita, T Nishimura, K Nagashio, A Toriumi, Jpn J App Phys **50** 04DA01 (2011)
333. C H Lee, T Nishimura, K Nagashio, K Kita, A Toriumi, IEEE Trans ED 58 1295 (2011) p209
334. C H Lee, C Lu, T Tabata, W F Zhang, T Nishimura, K Nagashio, A Toriumi, Tech Digest IEDM (2013) p2.5
335. V V Afanasev, A Stesmans, App Phys Lett 84 2319 (2004)
336. V Afanasev, A Stsmans, A Delabie, F Bellenger, M Houssa, M Meuris, App Phys Lett 92 022109 (2008)
337. A Ohta, S Miyazaki, et al, J Surf Sci Nanotech 4 174 (2006)
338. P Boqvist, F Binder, A Pasquarello, App Phys Lett 94 141911 (2009)
339. H Li, K Xiong, J Robertson, App Phys Lett 97 242902 (2010)
340. A Dimoulas, App Phys Lett 89 252110 (2006)
341. J R Weber, A Janotti, P Rinke, C G van de Walle, App Phys Lett 91 142101 (2007)
342. E H Poindexter, G J Gerardi, M E Rueckel, P J Caplan, N M Johnson, D K Biegelsen, J App Phys 56 2844 (1984)
343. P Broqvist, A Alkauskas, A Pasquarello, Phys Rev B 78 075203 (2008)
344. T Nishimura, K Kita, A Toriumi, App Phys Lett 91 123123 (2007)
345. H Seo et al, Phys Rev B 89 115318 (2014)
346. K L Brower, App Phys Lett 43 1111 (1983)
347. M Houssa, G Pourtois, M Caymax, M Meuris, M M Heyns, V Afanasev, A Stesmans, App Phys Lett 93 161909 (2008)
348. A Stesmans, P Somers, V V Afanasev, Phys Rev B 79 195301 (2009)
349. P Somers, A Stesmans, L Souriau, V V Afanasev, J App Phys 112 074501 (2012)
350. S Baldovino, M Fanciuli, App Phys Lett 93 242105 (2008)
351. S Baldovino, A Molle, M Fanciulli, App Phys Lett 96 222110 (2010)
352. S Paleari, A Baldovino, A Molle, M Fanciulli, Phys Rev Lett 110 206101 (2013)
353. A Stesmans, T N Hoang, V V Afanasev, J App Phys 116 044501 (2014)
354. P Broqvist, J F Binder, A Pasquarello, Physica B 407 2926 (2012)
355. H Li, J Robertson, Microelec Eng 109 244 (2013); H Li, J Robertson, given at SISC, San Diego (2013)
356. R M Wallace, P C McIntyre, J Kim, Y Nishi, MRS Bulletin **34** 493 (2009)
357. H Kim, C O Chui, K C Saraswat, P C McIntyre App Phys Lett **83** 2647 (2003)

358. S Takagi, T Maeda, N Taoka, M Nishizawa, Y Morita, K Ikeda, Y Yamashita M Nishikawa, H Kumagai, R Nakane, S Sugahara, N Sugiyama, Microelectronic Eng **84** 2314 (2007)
359. M Caymax, M Houssa, G Pourtois, F Bellenger, K Martens, A Delabie, S Van Elshocht, App Surface Sci **254** 6094 **(**2008)
360. M Milojevic, R Contreras-Guerrero, M Lopez-Lopez, J Kim, R M Wallace, App Phys Lett **95** 212902 (2009)
361. R Zhang, N Taoka, P-C Huang, M Takenaka, S Takagi, IEEE IEDM Tech Digest (2011), 642 (a)
362. R Zhang, T Iwasaki, N Taoka, M Takenaka, S Takagi, Microelectronic Eng **88**, 1533 (2011) (b)
363. R Zhang, T Iwasaki, N Taoka, M Takenaka, S Takagi, Tech Digest VLSI Symp (2011), 56 (c)
364. R Zhang, T Iwasaki, N Taoka, M Takenaka, S Takagi, J Electrochem Soc, G178 (2011) (d)
365. D Kuzum, J-H Park, T Krishnamohan, H S-P Wong, K C Saraswat, IEEE Trans Electron Dev **58** 1015 (2011)
366. H Kim, P C McIntyre, C O Chui, K C Saraswat, M H Cho, App Phys Lett **85** 2902 (2004)
367. C O Chui, F Ito, K C Saraswat, IEEE Trans. Electron Dev **53** 1501 (2006) (a)
368. C O Chui, H Kim, D Chi, P C McIntyre, K C Saraswat, IEEE Trans. Electron Dev **53** 1509 (2006**)**
369. Y Oshima, M Shandalov, Y Sun, P Pianetta, P C McIntyre, App Phys Lett **92** 183102 (2009)
370. Q Xie, J Musschoot, M Schaekers, M Caymax, A Delabie, X P Qu, Y L Jiang, S V Berghe, J Liu, C Detavernier, App Phys Lett **97**, 222902 (2010)
371. S Sioncke, H C Lin, L Nyns, G Brammertz, A Delabie, T Conard, A Franquet, J Rip, S DeGendt, M Mulle,r B Beckhoff, M Caymax, J App Phys 110 084907 (2011)
372. A Delabie, S Sioncke, J Rip, S Van Elshocht, M Caymax, G Pourtois, K Pierloot, J Phys. Chem C **115**, 17523 (2011)
373. C Fleischmann, K Schouteden, M Muller, P Honicke, B Beckhoff, S Sioncke, H G Boyen, M Meuris, C V Hasendoek, K Temst, A Vantomme, J Mat Chem C 1 4105 (2013)
374. J S Lee,T Kaufman-Osborn, W Melitz, S Lee, A Delabie, S Sioncke, M Caymax, G Pourtois, A C Kummel, J Chem Phys **135** 054705 (2011)
375. R Zhang, N Taoka, P C Huang, M Takenaka, S Takagi, Tech Digest IEDM (2011) p28.3
376. H Li, J Robertson, App Phys Lett 101 052903 (2013)
377. R Zhang, P C Huang, J C Lin, M Takenaka, S Takagi, Tech Digest IEDM (2012) p16.1
378. R Zhang, J C Lin, X Yu, M Takenaka, S Takagi, Tech Digest VLSI (2013) p3.1
379. R Zhang, P C Huang, J C Lin, M Takenaka, S Takagi, App Phys Lett 102 081603 (2013)
380. C H Lee, C Lu, T Tabata, K Nagashio, A Toriumi, Tech Digest VLSI (2013) p3.2
381. S Swaminathan, Y Oshima, M A Kelly, P C McIntyre, App Phys Lett **95**, 032907 (2009)
382. J Han, R Zhang, T Osada, M Hata, M Takenada, S Takagi, App Phys Expr 6 051302 (2013)
383. A Toriumi et al, Tech Digest IEDM (2009)
384. R Zhang et al, Tech Digest IEDM (2012)
385. R Zhang et al, Tech Digest IEDM (2013)

Table 1. Static dielectric constant (K), experimental band gap and (consensus) conduction band offset on Si of the candidate gate dielectrics.

	K	Gap (eV)	CB offset (eV)
Si		1.1	
SiO_2	3.9	9	3.2
Si_3N_4	7	5.3	2.4
Al_2O_3 sapphire	9	8.8	2.8
Al_2O_3 ALD	8	6.4	1.6
Ta_2O_5	22	4.4	0.35
TiO_2	80	3.5	0
$SrTiO_3$	2000	3.2	0
ZrO_2	25	5.8	1.5
HfO_2	25	5.8	1.4
$HfSiO_4$	11	6.5	1.8
La_2O_3	30	6	2.3
Y_2O_3	15	6	2.3
a-$LaAlO_3$	30	5.6	1.8
$LaLuO_3$	32	5.2	2.1

Table 2. Precursor molecules for atomic layer deposition (ALD)

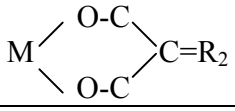
type	Formula	comments
chlorides	MCl_4	Non-volatile, corrosive byproduct
alkyls	M-R	Al, Zn OK, but few others
alkoxides	M-OR	Limited stability, better for MOCVD than ALD
Diketonates		Low reactivity, high melting point
Alkyl imide	M = N-R	Thermal stability
Alkyl amides	$M - NR_2$	good thermal stability
Alkyl amido	$M - (N=RR')_n$	good thermal stability
Pentadienyl		Low reactivity or low volatility
nitrates	$M (NO_3)_n$	

Table 3. Comparison of the calculated conduction band offset (by LDA method) and experimental values for various gate oxides, by various authors. * = ALD

	Calculated (eV)	Experiment (eV)	Ref
SiO_2		3.1	Alay (1999)
Ta_2O_5	0.35	0.3	Miyazaki (2001)
$SrTiO_3$	0.4	0	Chambers (2000)
ZrO_2	1.6	1.4 2.0 1.4	Miyazaki (2001) Afanasev (2002) Rayner (2002)
HfO_2	1.3	1.3 2.0	Sayan (2002) Afansev (2002)
Al_2O_3	2.4	2.8 2.2 *	Ludeke (2000) Afansev (2007)
a-$LaAlO_3$	1.0	1.8	Edge (2004)
La_2O_3	2.3	2.3	Hattori (2004)
Y_2O_3	2.3	1.6	Miyazaki (2001)
$LaLuO_3$	2.2	2.1	Lopes (2006)

Table 3 Physico-chemical properties of Ge compared to other semiconductors

	Si	Ge	GaAs
Band Gap (eV)	1.1	0.66	1.42
Electron mobility ($cm^2/V.s$)	1500	3900	8500
Hole mobility ($cm^2/V.s$)	450	1900	400

Table 4. Properties of the Ge and Si oxide compared.

	SiO_2	GeO_2
ΔH_f (eV)	-4.80	-3.27
Band gap (eV)	9.0	6.0
Si-H bond energy (eV)	3.3	3.1
CNL (of semiconductor) (eV)	0.3	0

Fig captions

1. The scaling of feature size, gate length, and oxide thickness according to the 2009 Semiconductor Roadmap
2. Leakage current vs voltage for various thickness of SiO_2 layers, after [14].
3. TEM image of SiO_2 based gate stack vs image of HfO_2 gate stack.
4. The three contributions to the capacitance of the gate/electrode stack; channel, dielectric and gate depletion.
5. Schematic of replacement of SiO_2 gate oxide and the poly-Si gate by high K gate oxide and metal gate, showing effect on gate capacitances.
6. Static dielectric constant vs band gap for candidate gate oxides [9].
7. Effect of reaction of Si with ZrO_2 making Zr silicide.
8. Need for band offsets of over 1 V.
9. Leakage current density vs. EOT for various high K oxides, for HfO_2 (Gusev [17]), ZrO_2 (Tsai [44]), Al_2O_3 (Gusev [17], Guha [42]) and La_2O_3 (Iwai [26]).
10. Comparison of the gate first and gate last (replacement gate, dummy gate) process.
11. Schematic of the cyclic process of Atomic Layer Deposition. Thanks to P C McIntyre.
12. Scanning electron microscope image of trench structure showing excellent coverage by ALD HfO_2. Thanks to P C McIntyre.
13. Annealing of the infra-red spectrum of a HfO_2 film grown by ALD with water as oxidant, showing the evolution of hydrogen [35].
14. Plan view TEM image of crystallisation in HfO_2 /SiO_2 alloy system (a) 40% HfO_2, (b) 80% HfO_2 [89]. Thanks to S Stemmer.
15. (a) Phase diagram of ZrO_2/SiO_2 showing miscibility gap. After Kim and McIntyre [88]. (b) Phase diagram of La_2O_3/SiO_2 with miscibility gap. After Maria[86].
16. HRTEM cross section showing interfacial layer of SiO_2 below the HfO_2 layer. Thanks to S Stemmer. (b) Schematic of need for MIPS to minimise oxygen ingress.
17. (a) Band structure and (b) Density of states of α-Al_2O_3 (corundum). (c) Band structure of θ-Al_2O_3
18. Local order in cubic, tetragonal and monoclinic HfO_2 or ZrO_2.
19. Band structure and density of states of cubic HfO_2.
20. Band structure and density of states of cubic ZrO_2.
21. Partial density of states of La_2O_3.
22. Partial density of states of crystalline $ZrSiO_4$.
23. Bands and Density of states of cubic $LaAlO_3$.
24. Density of states of cubic $LaLuO_3$.
25. Free energy of formation of various oxides per O atom, vs. Parent metal work function. Equivalent to an Ellingham diagram.
26. Schematic of how charge transfer at semiconductor interface controls its band line up, a) no charge transfer, b) charge transfer
27. (a) Origin of metal induced gap states (MIGS) at metal-semiconductor interface, (b) presence of MIGS type states at a semiconductor-semiconductor heterojunction, only in energy range where band states exist.
28. Predicted barrier heights for a range of high K gate oxides, after Robertson [9].
29. Bonding at (100)Si:HfO_2 interfaces. O-terminated, non-polar and Hf-terminated interfaces.

30. Bonding at Si-HfO2 interfaces. (a) unrelaxed O-terminated O_4 interface, (b) relaxed O_4 interface, (c) O_3 interface, and (d) O_2 interface.
31. Atomic bonding at relaxed metal-terminated interfaces (a) Hf_6, (b) Hf_{10} .
32. The relaxed structure of (a) neutral oxygen vacancy and (b) the neutral oxygen interstitial in HfO_2
33. Calculated defect energy levels of the oxygen vacancy and O interstitial in HfO_2 in various charge states.
34. Defect formation energy vs Fermi energy of O vacancy and O interstitial in cubic HfO2, in O-rich and O-poor condition. The stable charge state at any Fermi energy corresponds to the lowest energy.
35. Electron trapping in HfO_2 gate oxide layer. The hysteresis between the up and down ramps shows the presence of sizable trapping. The identical curves for up and down show that no new defects are created.
36. Calculated defect wavefunction of O vacancy in HfO_2, (a) in GGA and (b) SX, showing lowering of symmetry in SX result.
37. Passivatioon of O vacancy in HfO_2 by introduction of two nitrogens. Atomic strcuture, schematic energy levels, and partial density of states. Note absence of deep gap states.
38. Passivatioon of O vacancy in HfO_2 by introduction of two La atoms. Atomic strcuture, and partial density of states. Note absence of deep gap states.
39. Calculated defect formation energy vs Fermi energy of oxygen vacancy in θ-Al_2O_3.
40. Calculated defect energy levels of oxygen vacancy in La_2O_3 and $LaAlO_3$ in various charge states.
41. Prefered values of gate work functions for simple CMOS devices.
42. Schematic definition of effective work function (EWF). Energies referred to Si band edges, and thereby to the vacuum level.
43. (a) Effective work functions of metals on HfO_2, from internal photoemission data (Afanasev) and from CV data cited by Yeo [252]. (b) effective work functions of 3 refractory metals on HfO2 vs on SiO_2, by barrier height method, from Zafar [254], effective work functions of metals of HfO2 vs metal vacuum work function, from data of Koyama [253].
44. Effective work functions of metals on HfO_2 against metal index, from Schaeffer [255].
45. Flat band voltage vs annealing temperature for Re-HfO_2 stacks cyclically annealed in oxygen and forming gas, from Cartier [257].
46. (a) Effective work functions of refractory metals on HfO_2, $HfSiO_x$ and SiO_2 from Wen [259]. (b) Data replotted as EWF on HfO_2 vs. EWF on SiO_2. This gives a slope S ~ 0.82
47. O-terminated, non-polar, and metal-terminated interfaces of FCC metal on HfO_2.
48. Calculated valence band offsets (VBO) of metals on HfO_2 interfaces, for different interface terminations. Note S factor of 0.9, and the large shift between the non-polar (110) interface and the polar (100) interface. EWF is calculated from the VBO.
49. (a) Schematic of oxygen vacancy creation and charge transfer from vacancy to gate electrode for a metal-HfO_2-silicon stack. (b) resulting band bending due to positive vacancies.
50. Formation energy of O vacancies in HfO2 in contact with large excess of Si, at the Si/SiO2 equilibrium chemical potential. Note the very low formation energy of the O vacancy.

51. Overall reaction, forming charge O vacancy, electrons going to the gate, and oxygen atom reacting with the Si to form more SiO2.
52. EWF of p-type metals on HfO_2 vs EOT, showing the V_T roll-off effect at low EOT values, after Lee et al [8].
53. Schematic of oxide capping layer on HfO2 gate oxide, in gate first approach.
54. Cross sectional TEM image, and lateral EELS scan for oxide composition across gate stack having a La capping layer. Note that La has moved to the HfO2/SiO2 interlayer (IL) from its initial position at the TiN/HfO2 interface [276].
55. CV plots of different layer structures to find the active interface in capping layer system. Note that the Vt shift depends on nature of bottom layer, not the top layer.
56. Configurations of metals of different valence substitiing for Hf sites at a SiO_2:HfO_2 interface, in dipole layer scheme.
57. (a) Calculated valence band offset (VBO) vs experimental flat band voltage shift Vfb, for various metal oxides, for configurations of fig 56. (b) Calculated VBOs versus metal valence, showing anomalous case of Al, (c) calculated VBOs vs metal work function, showing consistency with observed results.
58. Dipole mechanism from change of screening across SiO2/HfO2 interface.
59. Schematic carrier mobility vs vertical (gate) field in FETs in the universal mobility model, showing the mechanisms which limit the mobility, and their temperature dependences.
60. (a), (b) electron and hole mobilities of FETS on 3 nm HfO_2 gate oxide on 1 nm SiO_2 with TiN gate electrodes, showing the stronger degradation of electron mobility [303].
61. Schematic of remote charge scattering, and remote phonon scattering, including the interfacial layer, which partially screens their effect.
62. Variation of additional mobility with thickness of the inter-layer, at different temperatures, for scaled oxides, after Ragnarsson [305].
63. Additional mobility vs gate field, at low fields and different temperatures, after Casse [303].
64. Mobility vs EOT for NMOS, using data from Nayaranan [264,10], Lee [12], Ragnarsson [303] and Ando [94].
65. Carrier injection into O vacancy levesl causing PBTI in nFET, and hole injection into SiO2 hole traps causing NBTI in pFETs, after Cartier [307].
66. PBTI and NBTI in HfO2 gate oxide compared to reference SiON system [307].
67. Normalised variation of PBTI and NBTI with changes in EOT for HfO2 gate oxide system, including scavenged oxide [307].
68. Maximum applied gate voltage to give 30 mV Vt shift after 10 year lifetime, for PBTI and NBTI, vs EOT, after Ragnrsson [305]
69. Schematic of reducing the oxide inter-layer by scavenging, for three different scavenger metal locations, after [94].
70. Cross sectional TEM showing reduction of SiO_2 interlayer after scavenging.
71. EOT reduction by scavenging, vs free energy of oxide formation per O atom. Electropositive metals are aggressive scavengers. Optimum scavengers are less aggressive, but more electropositive than Si, such as Ti.
72. Temperature dependence of scavenging reaction, showing onset at the O diffusion temperature of 500C [94].
73. Electron mobility vs EOT for scavenged gate stack, at 1 MV/cm vertical field.

74. Schematic of V_T roll-off vs. EOT dependence for scavenged oxide gate last stacks, from [312], showing roll-off occurring at a smaller EOT value than for gate first stacks.
75. T inversion vs ITRS node, showing small EOTs acheieved by use of HfO_2.
76. Flat band voltage of TiN gate electrodes for FinFET, TiN for nFET and TiON for pFET.
77. Cross sectional TEM image of (100) and (111) Ge/GeO_2 interfaces, showing their abruptness and flatness (Sasada [326])
78. Schematic of the GeO evolution mechanism, O vacancies are created at Ge/GeO_2 interface, causing traps, they diffuse across the oxide, and then react with the outside GeO_2 layer to form GeO molecules [329].
79. Calculated partial DOS of Ge/GeO_2 interface, giving valence band offset of 4.1 eV. (b) band alignemtn at Ge/GeO_2 interface, showing small conduction band offset.
80. Temperature dependence of stress and Pb density vs anneal temperature, after Houssa [345].
81. Magnetic field dependence of the EDMR sugnal of Ge P_b signal [350].
82. Valence alternation pair defect formed by re-arrangement of a relaxed O vacancy in GeO_2, consisting of a 3-fold O site and a 3-fold Ge site. 3-fold sote gives a state near Ev of Ge, 3-fold O site gives a state near Ec of Ge.
83. In-situ Ge 2*p* XPS spectra of ALD half cycles for (a) Ge(100) etched with deionized water, (b) clean Ge(100) surface, and (c) GeON surface. The 2*p* photoelectron line is chosen to enhance surface sensitivity due to the low photoelectron kinetic energy (~270 eV). After Milojevic 2009.
84. (a) The deconvoluted Ge 3*d* XPS spectra after plasma oxidation of an ALD Al_2O_3/Ge stack showing the dominance of the Ge^{3+} oxidation state. (b) The interface state density dependence on GeO_x thickness and oxidation state.
85. Use of Al_2O_3 as diffusion barrier on Ge for improve Ge/GeO_2 gate stacks. Oxidation of underlying Ge by ECR plasma is accomplished through the Al_2O_3 layer.
86. Electron and hole mobilties vs EOT for various FETs [320,356,331,378-380]

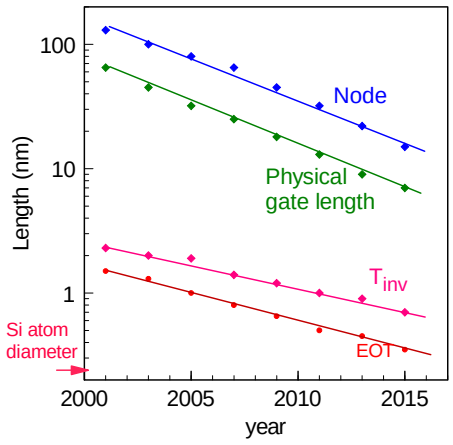


Fig. 1

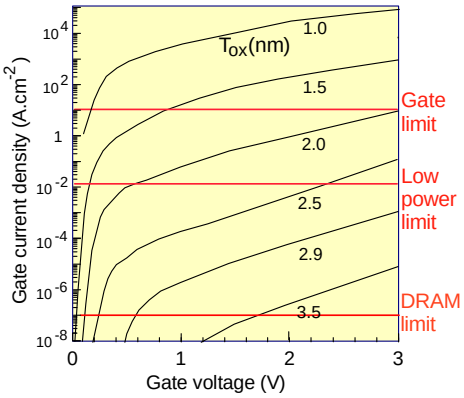


Fig 2

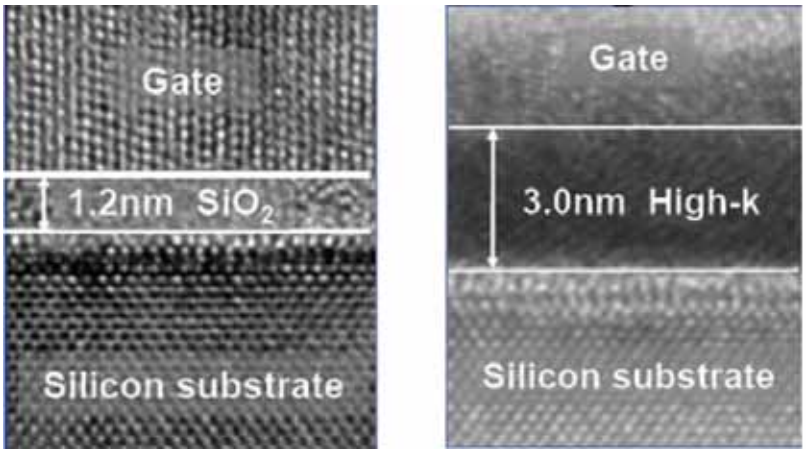


Fig 3

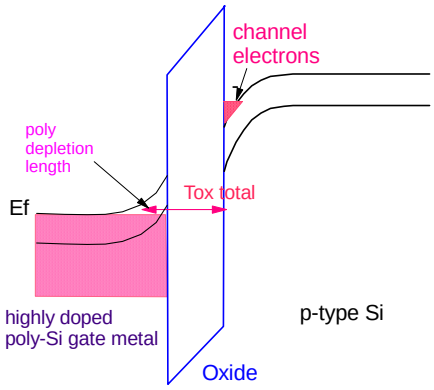


Fig 4

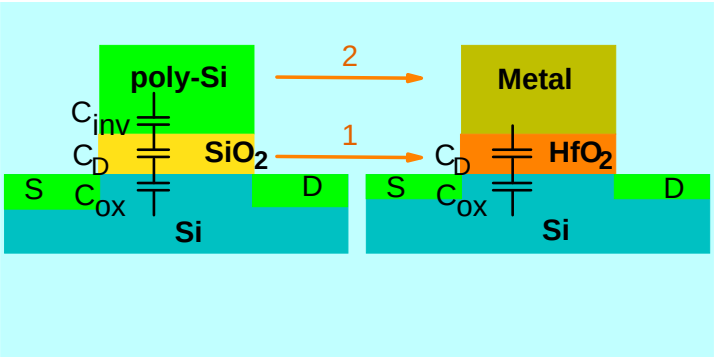


Fig. 5

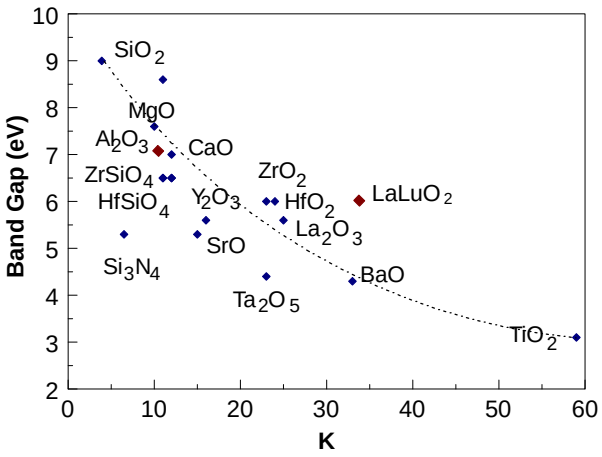


Fig 6

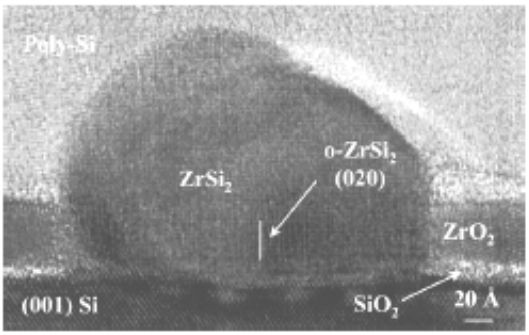


Fig 7

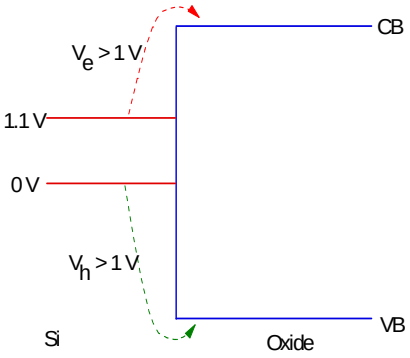


Fig 8

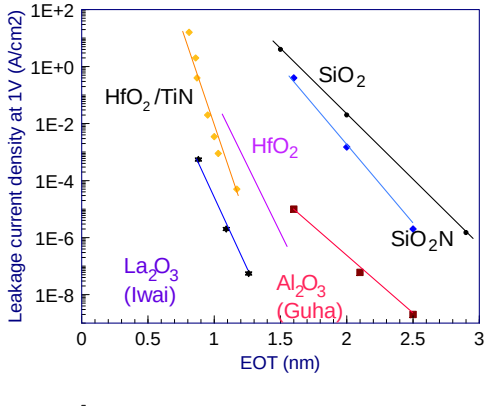


Fig 9

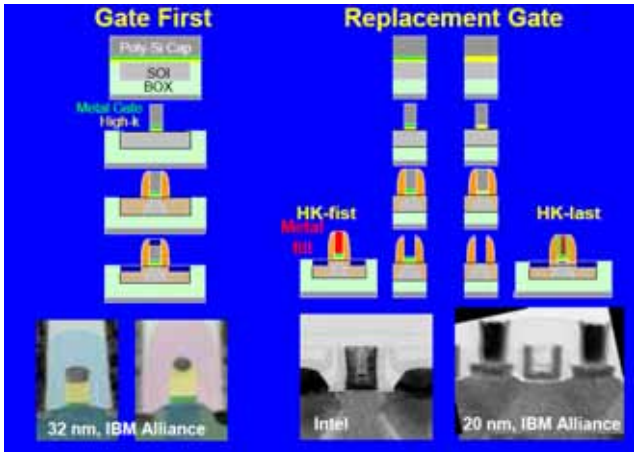


Fig 10.

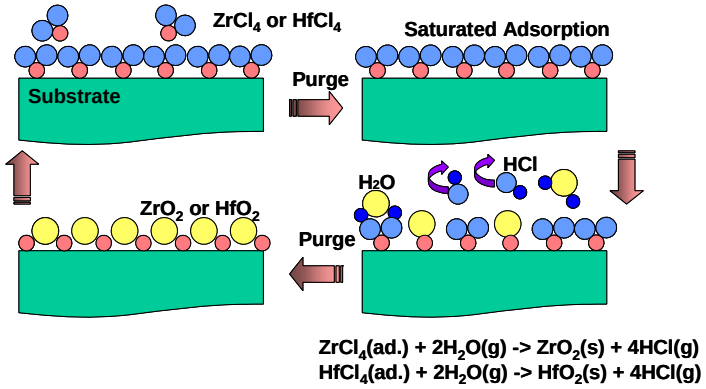


Fig 11

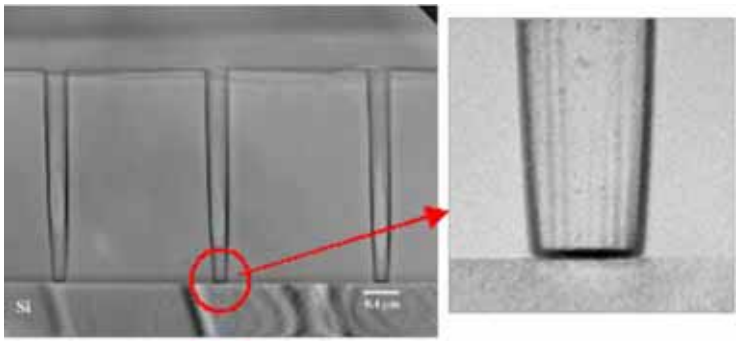


Fig 12

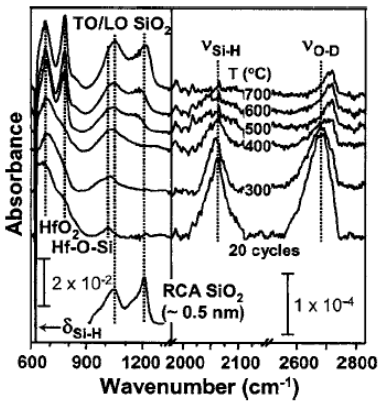


Fig 13

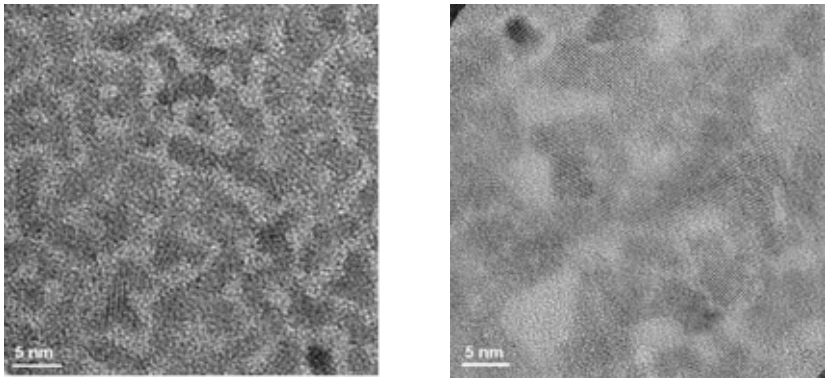


Fig 14

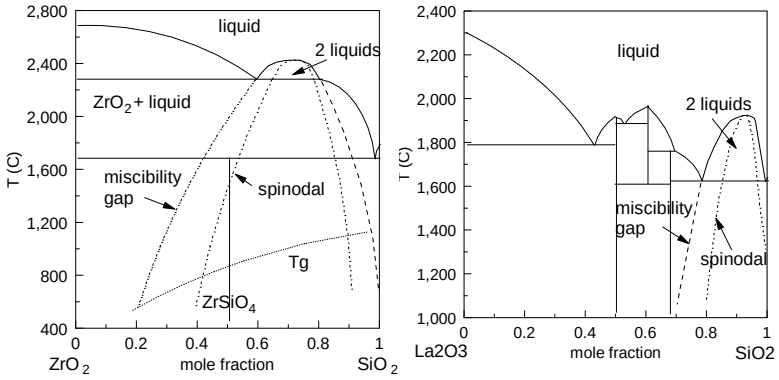
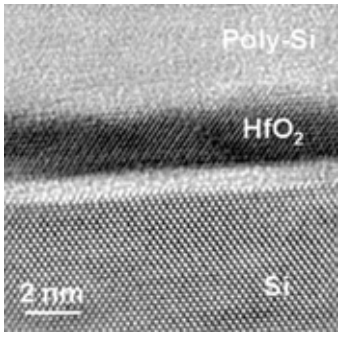


Fig 15



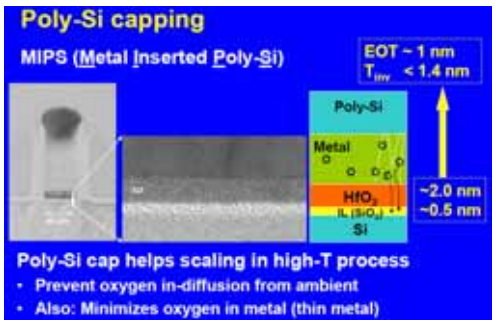
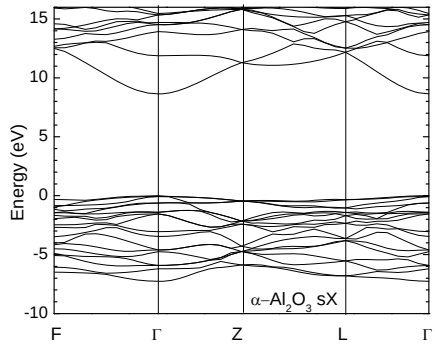
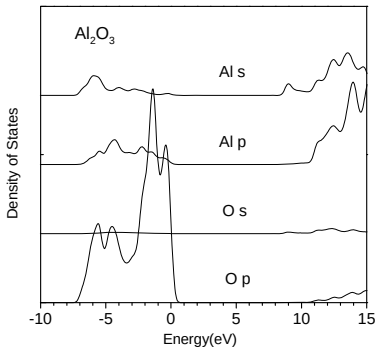


Fig 16





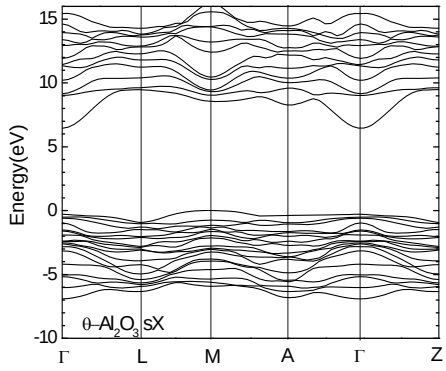


Fig 17

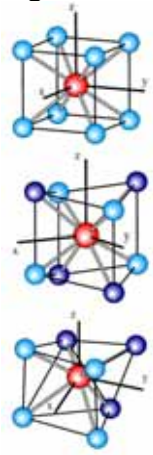


Fig. 18.

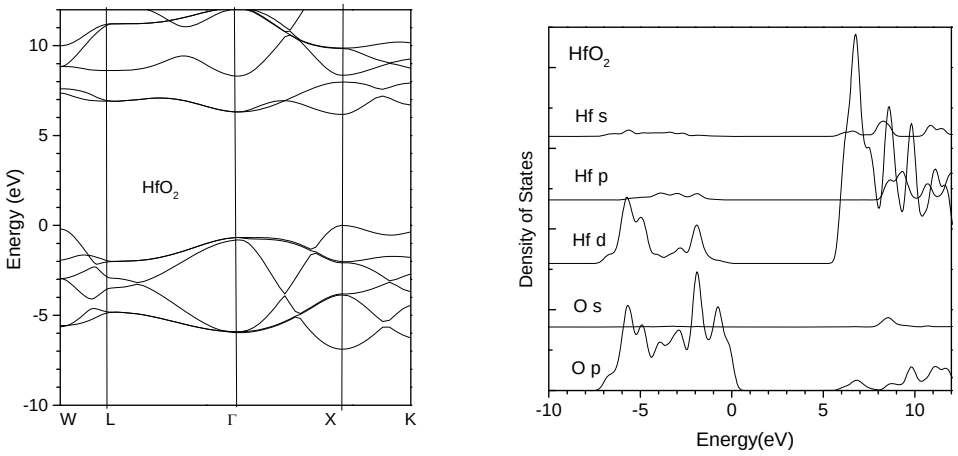


Fig. 19.

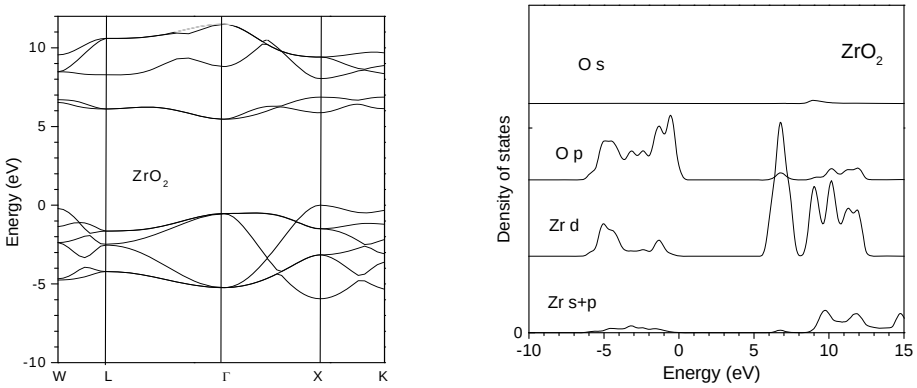


Fig 20

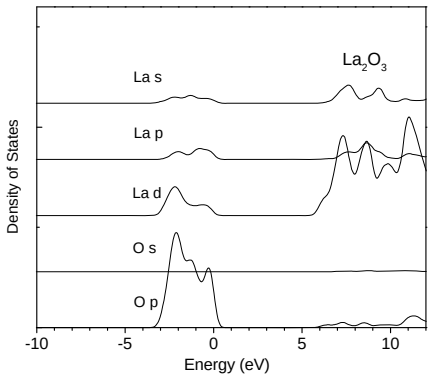


Fig 21

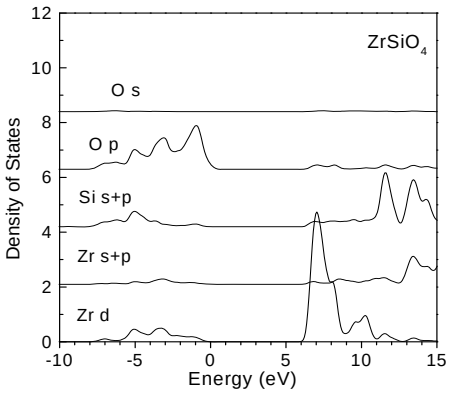


Fig 22

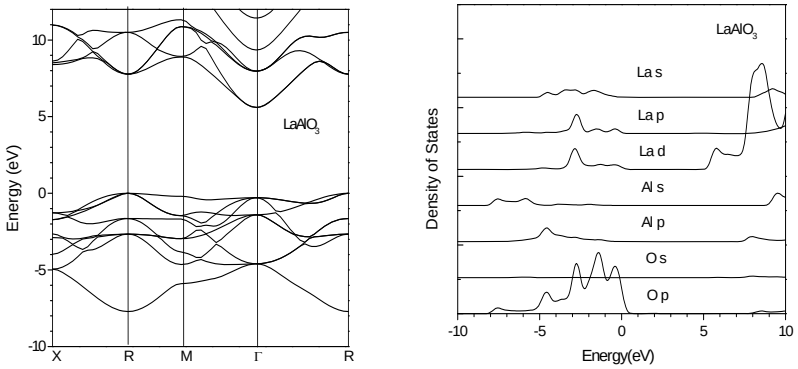


Fig 23

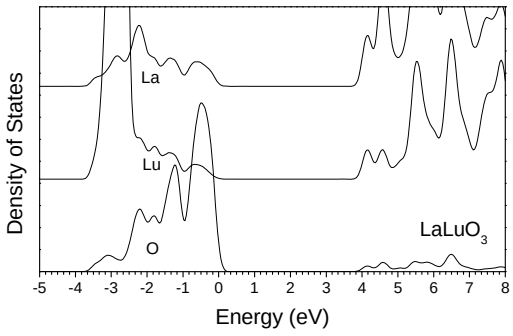


Fig 24

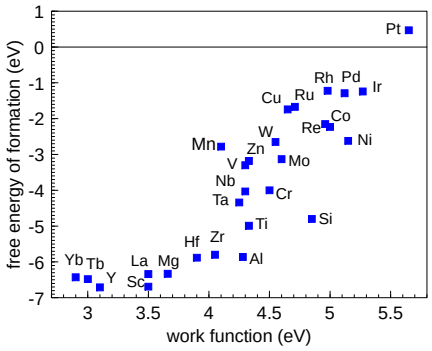


Fig 25.

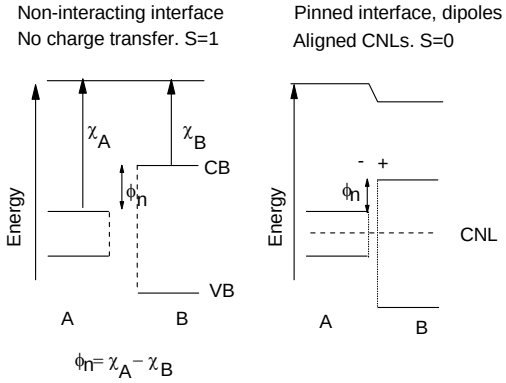


Fig 26

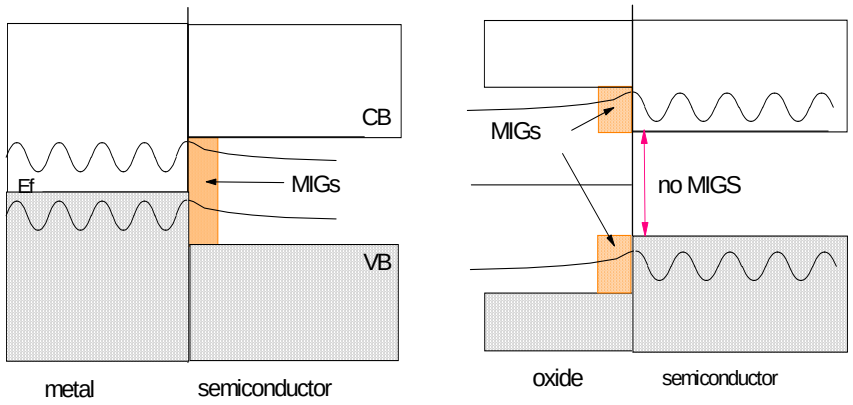


Fig. 27.

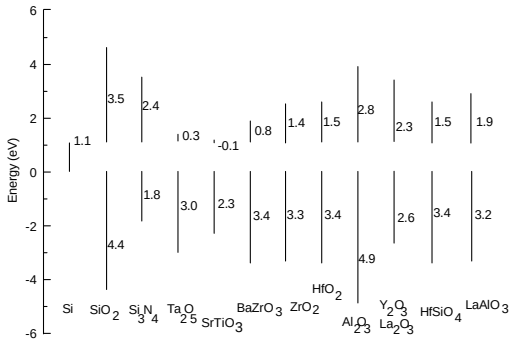


Fig 28

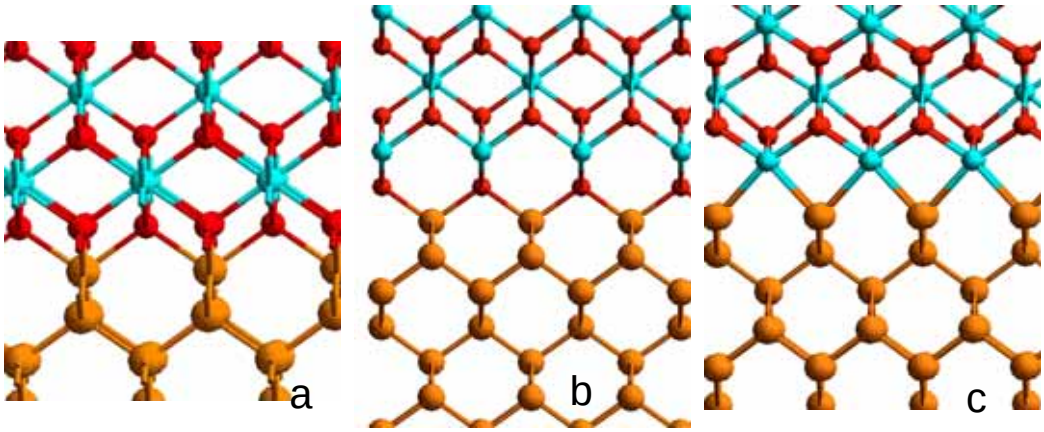


Fig. 29

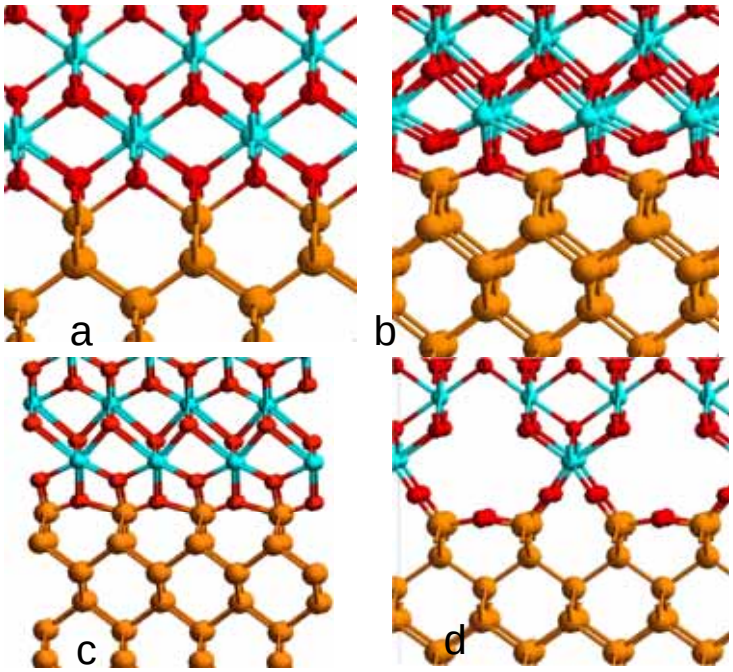


Fig. 30

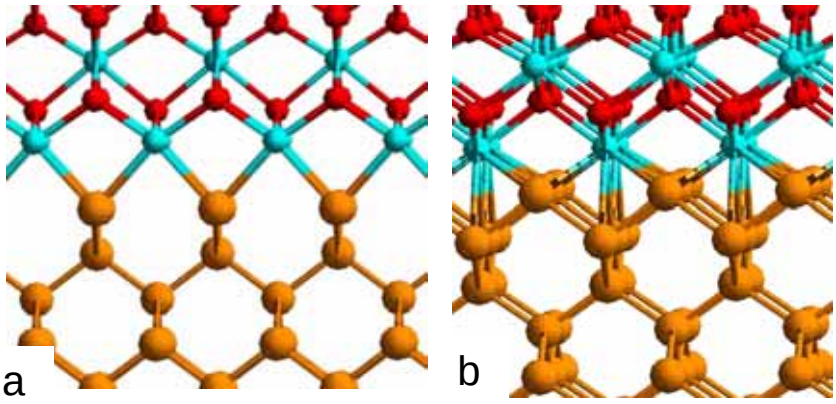


Fig. 31.

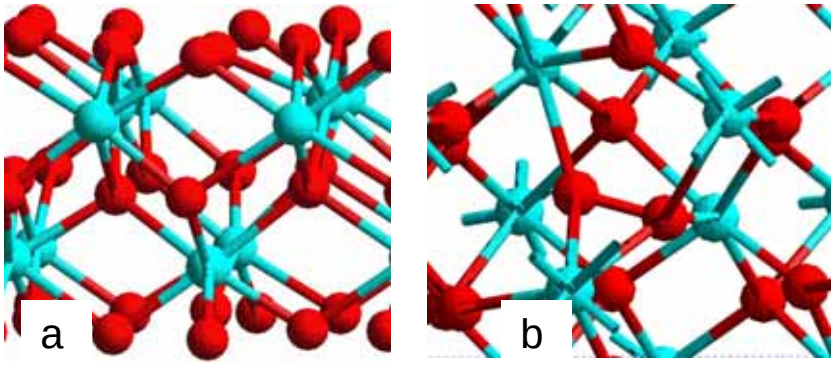


Fig 32

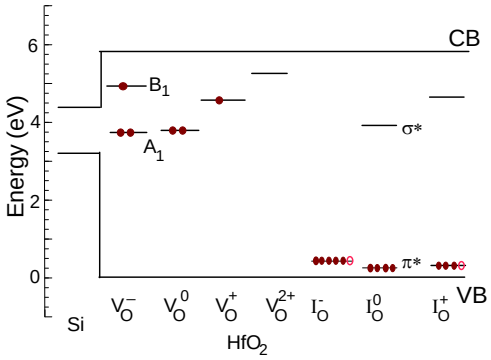


fig 33

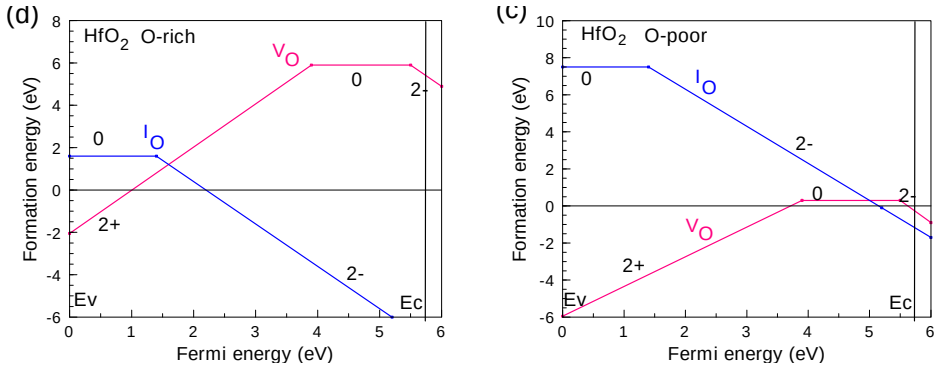


Fig 34.

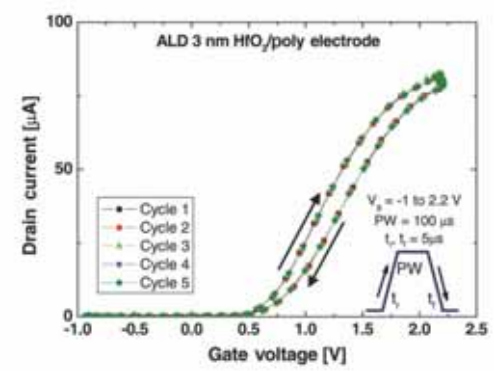


Fig. 35

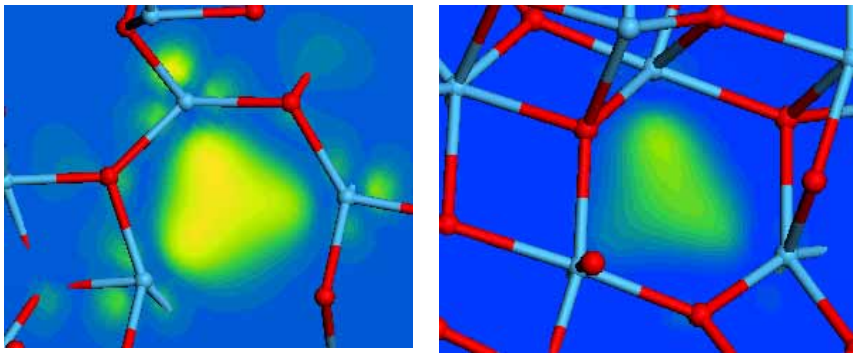


Fig 36

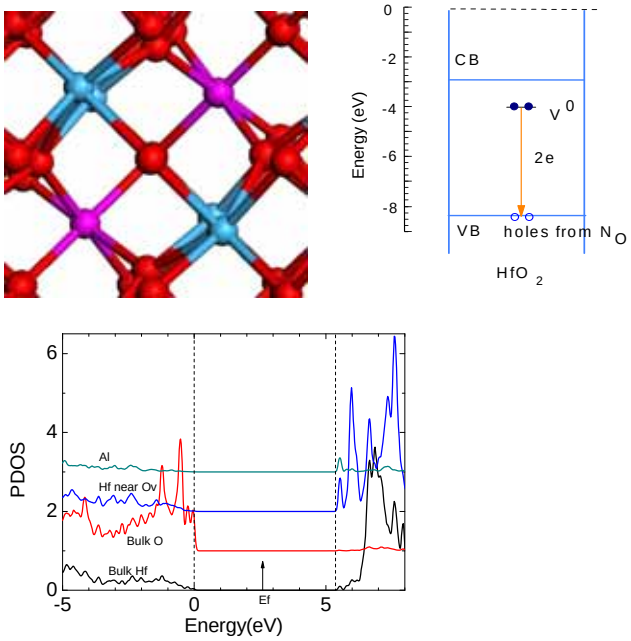


Fig. 37.

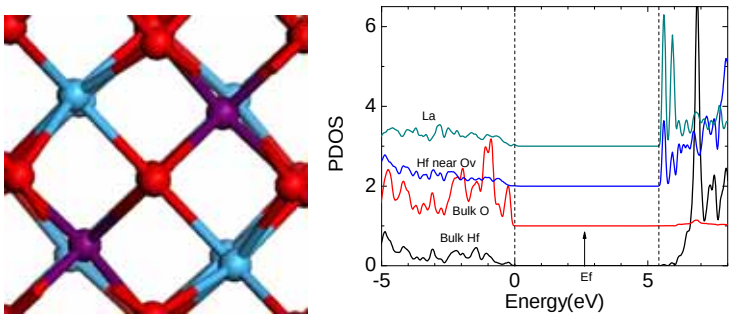


fig 38

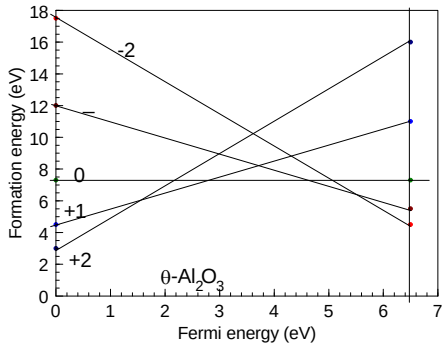


Fig. 39.

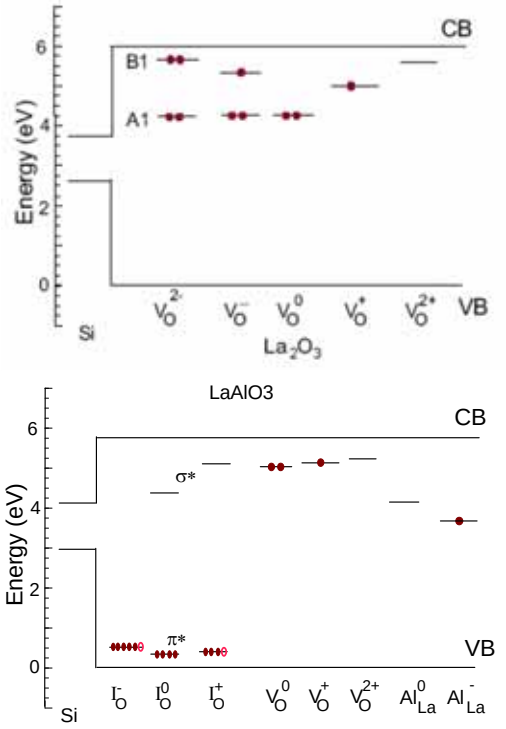


Fig 40

Fig 41

Fig 42

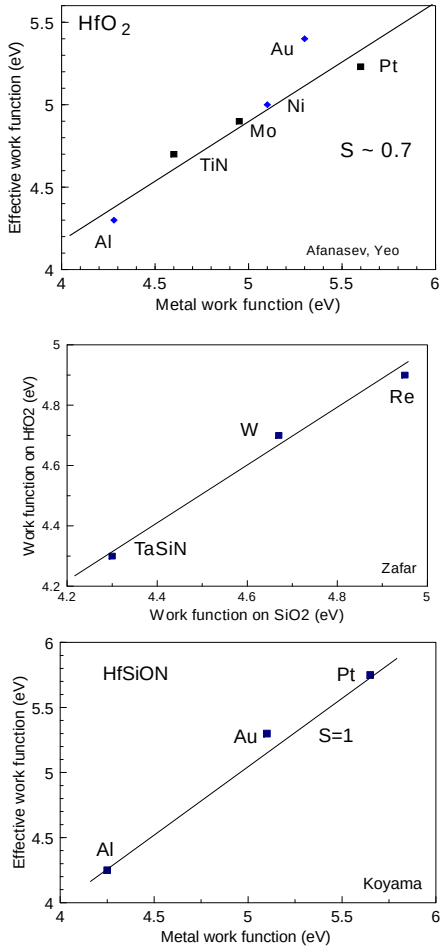

HfO 2
Au
Pt
Ni
Mo
S ~ 0.7
TiN
Al
Afanasev, Yeo
Effective work function (eV)
Metal work function (eV)
Work function on HfO2 (eV)
Re
W
TaSiN
Zafar
Work function on SiO2 (eV)
HfSiON
Pt
Au
S=1
Al
Koyama
Effective work function (eV)
Metal work function (eV)

Fig 43.

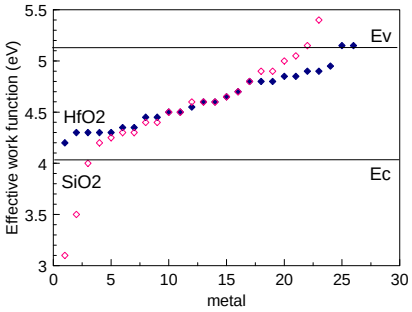

Ev
HfO2
SiO2
Ec
Effective work function (eV)
metal

Fig. 44.

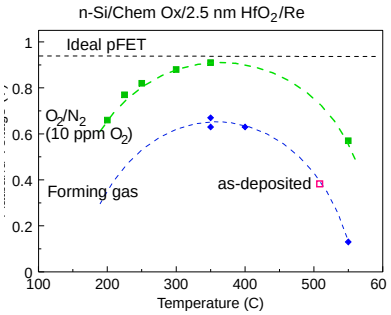


Fig. 45.

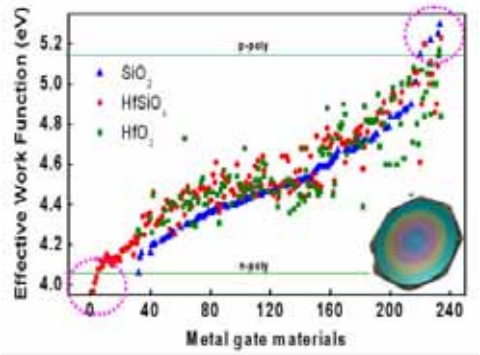
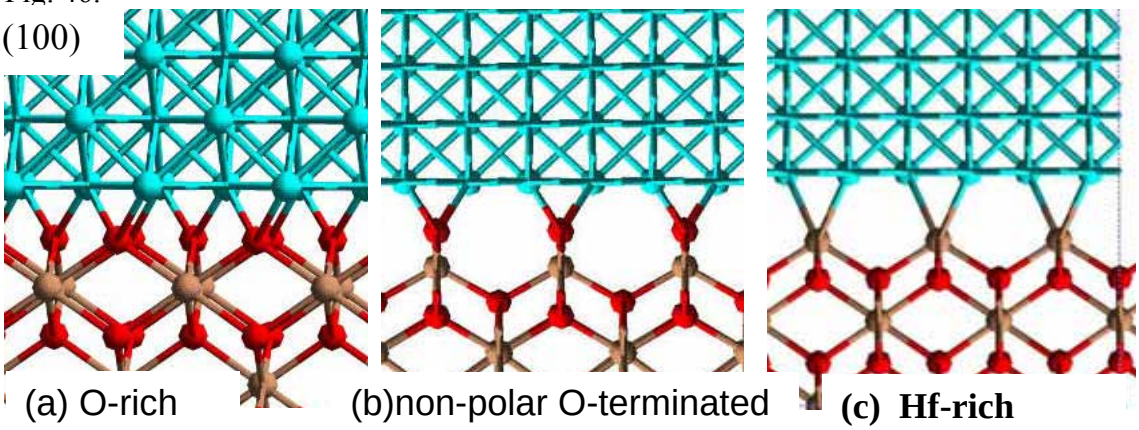


Fig. 46.

(100)



(a) O-rich (b)non-polar O-terminated **(c) Hf-rich**

fig 47

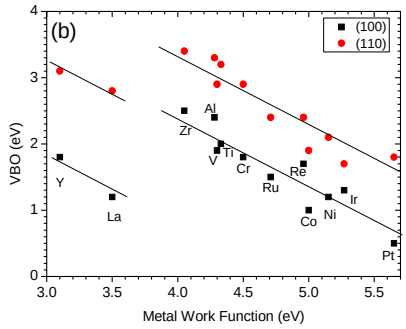


fig 48

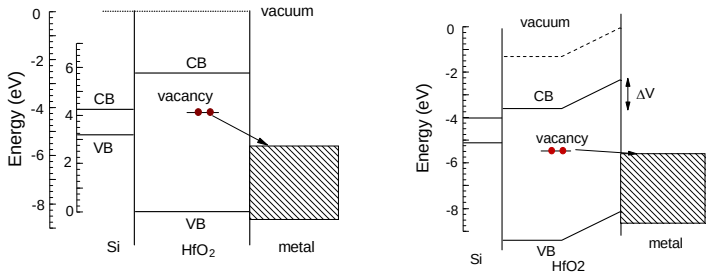


Fig. 49.

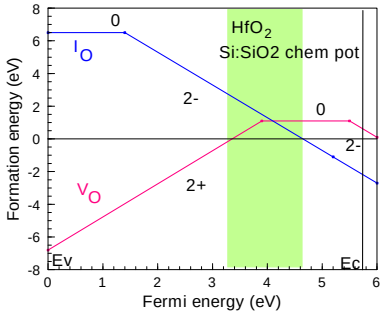


Fig 50

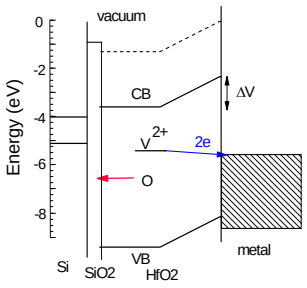


fig 51

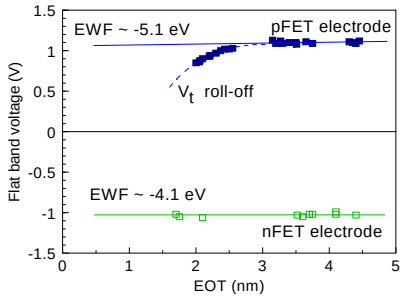


Fig 52

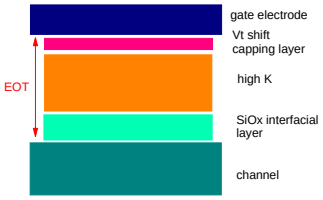


Fig 53

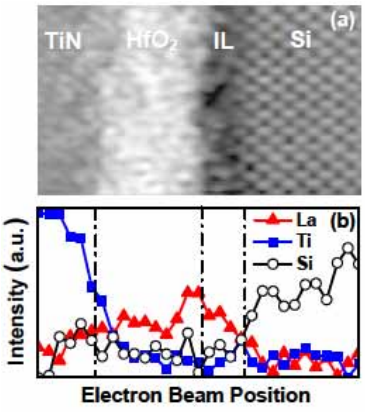


Fig 54

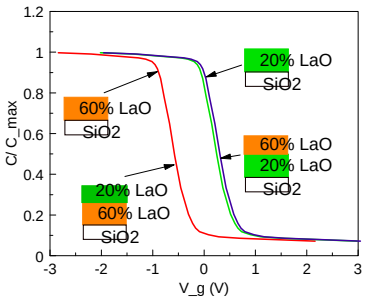


Fig 55

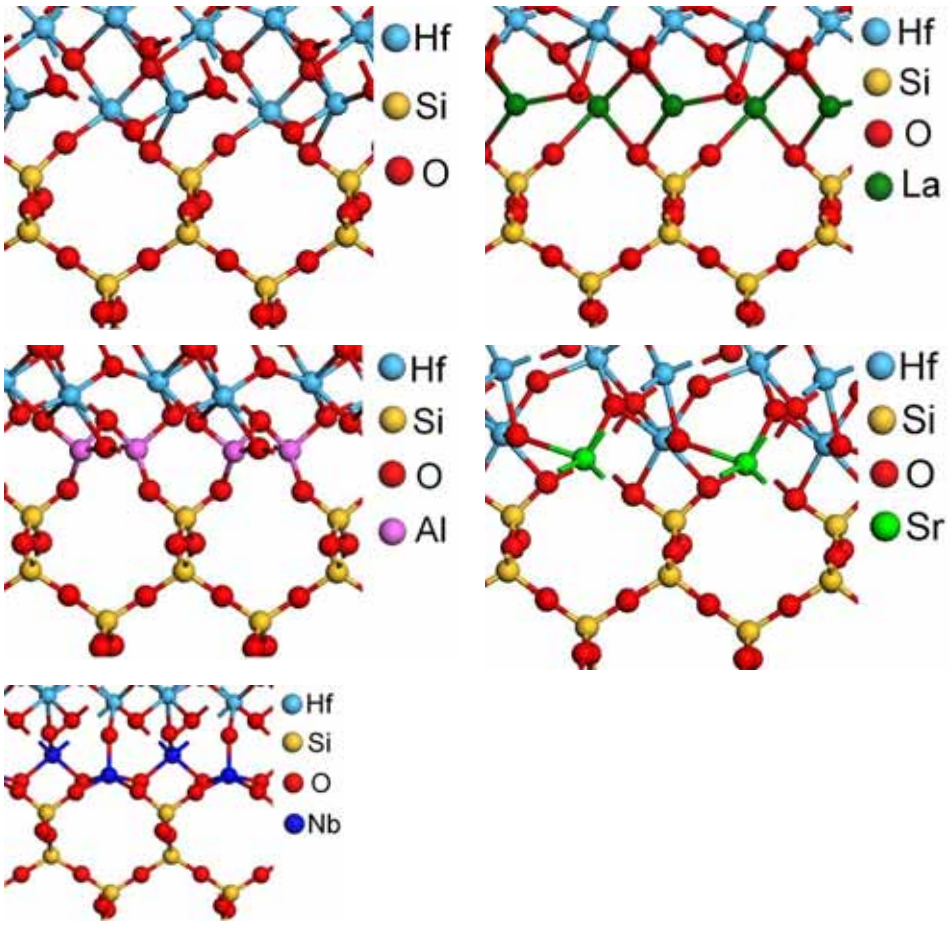


Fig 56

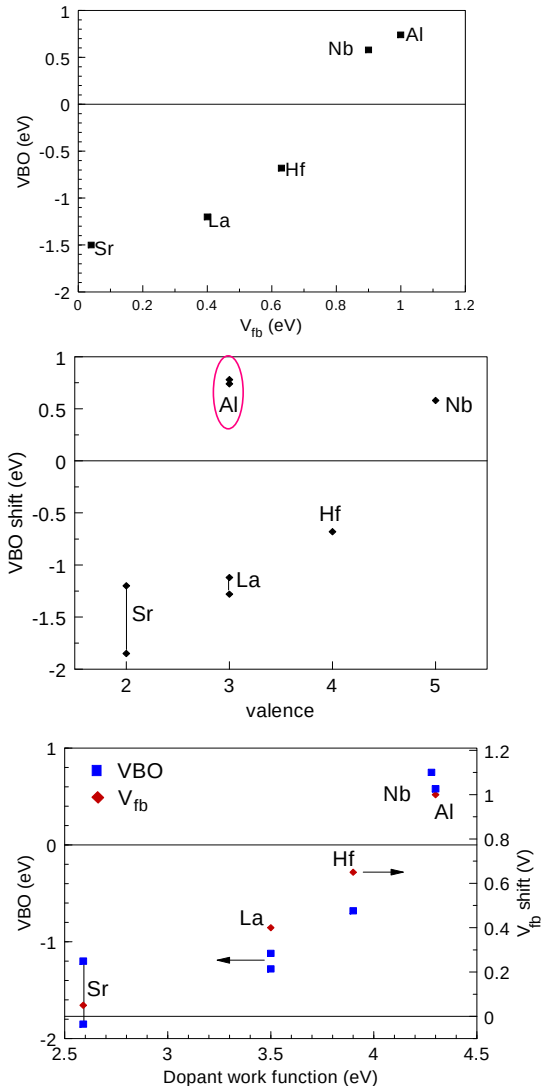

VBO (eV)
V_fb (eV)
Al
Nb
Hf
La
Sr
VBO shift (eV)
valence
VBO
V_fb
V_fb shift (V)
Dopant work function (eV)

Fig 57

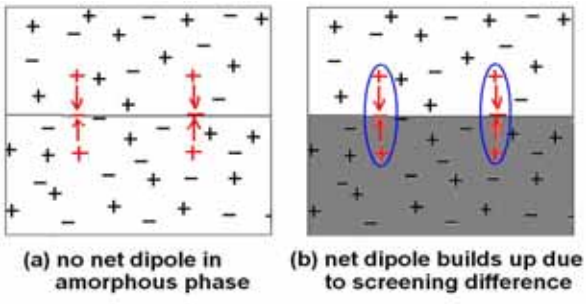

(a) no net dipole in amorphous phase
(b) net dipole builds up due to screening difference

Fig 58

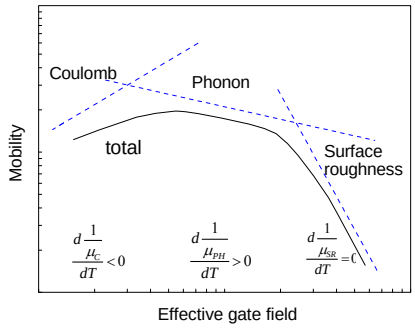


Fig 59

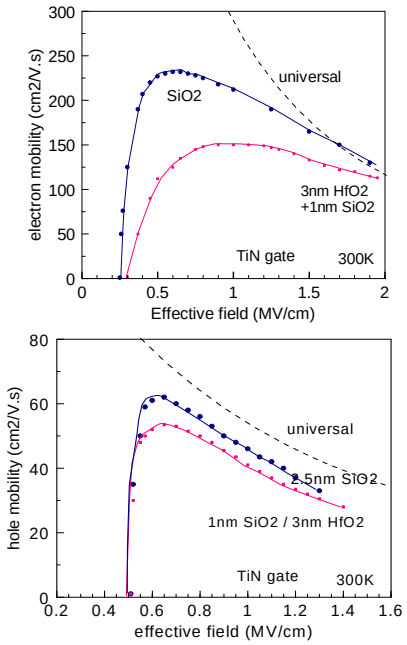


Fig 60.

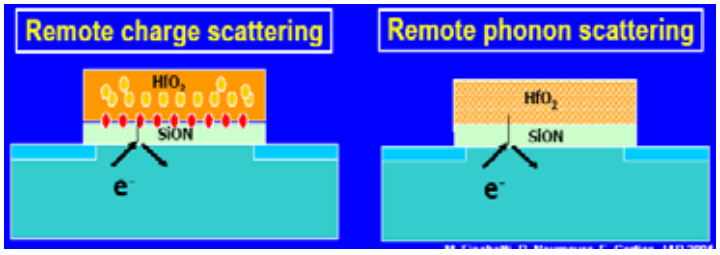


Fig 61

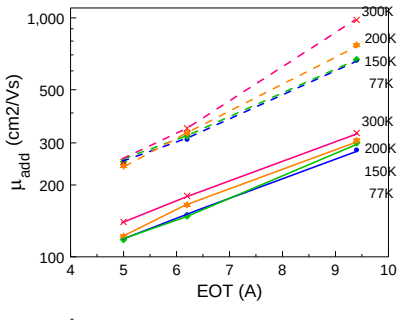


Fig 62.

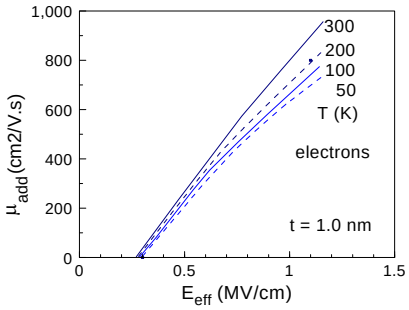


Fig 63

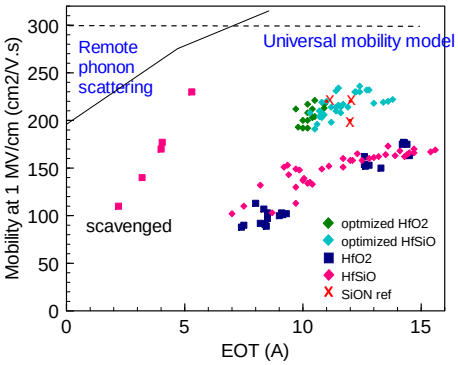


Fig 64

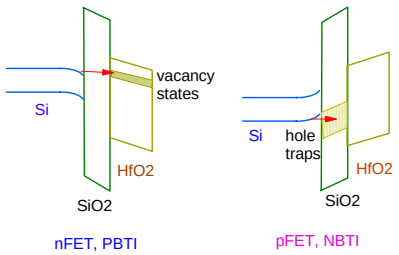


Fig 65.

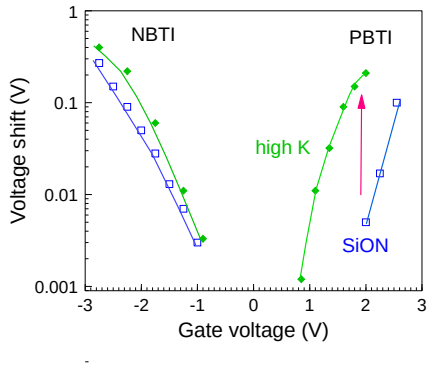


Fig. 66

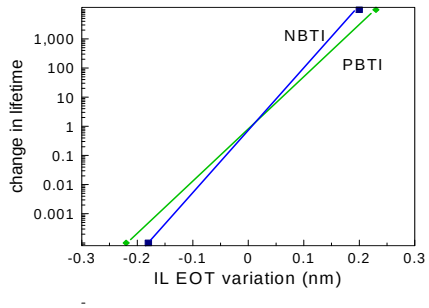


Fig. 67

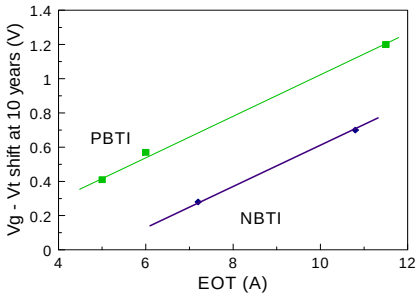


Fig 68.

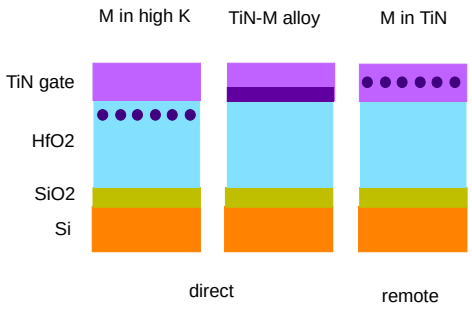


Fig 69.

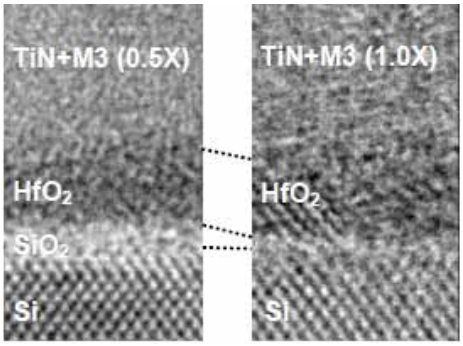


Fig 70

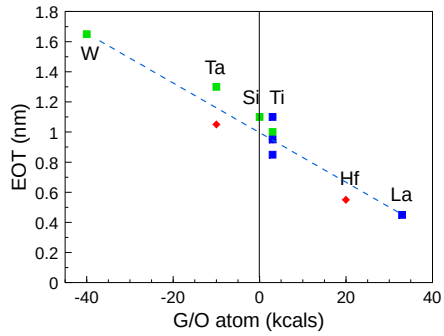


Fig 71.

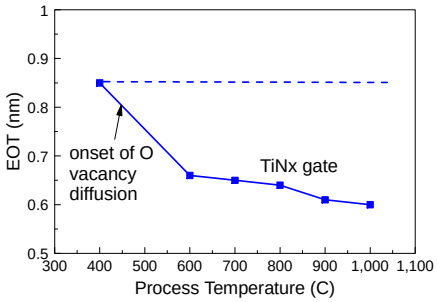


Fig. 72.

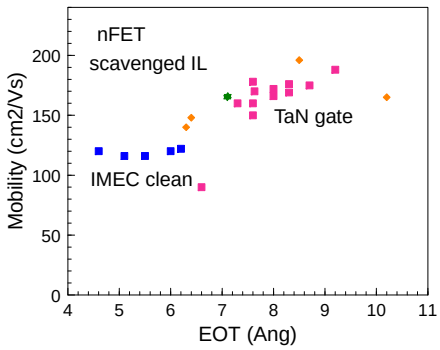


fig 73

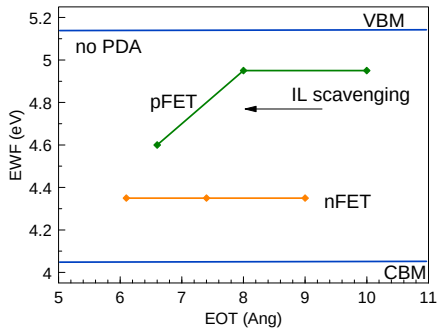


Fig 74

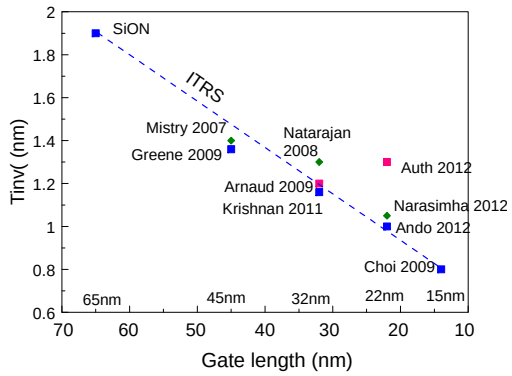


Fig 75

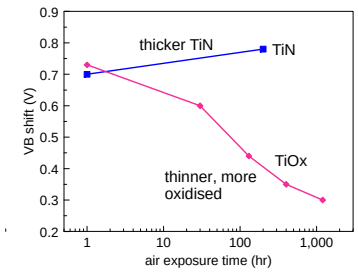


Fig 76.

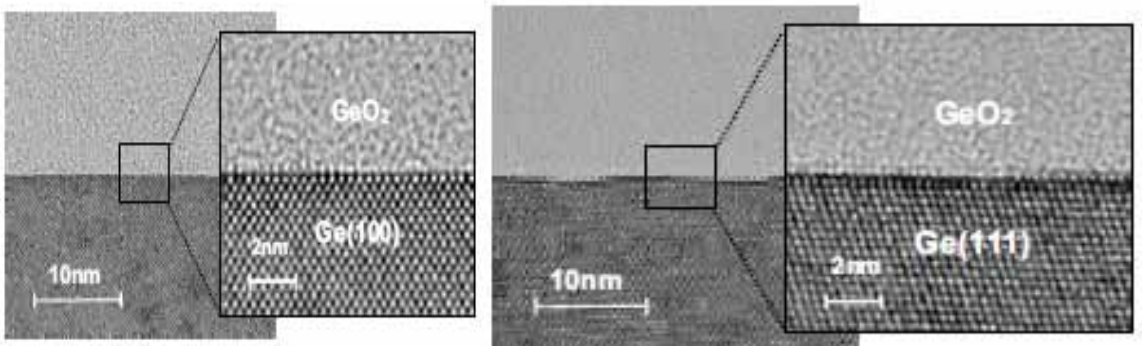


Fig 77.

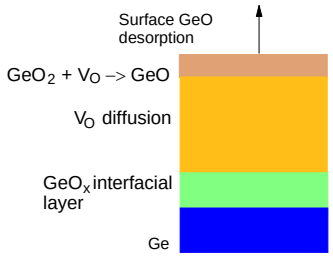
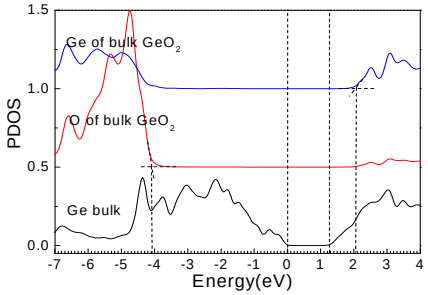


Fig 78.



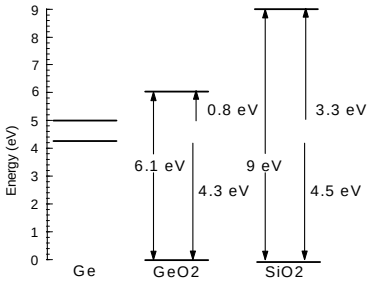


Fig 79

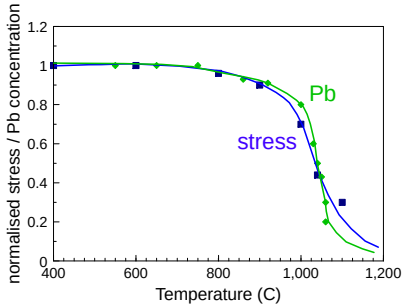


Fig 80

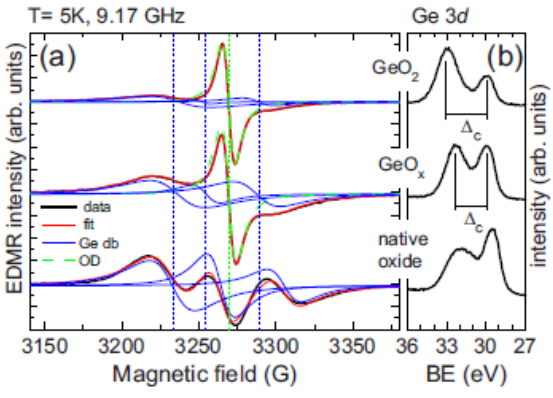


Fig 81

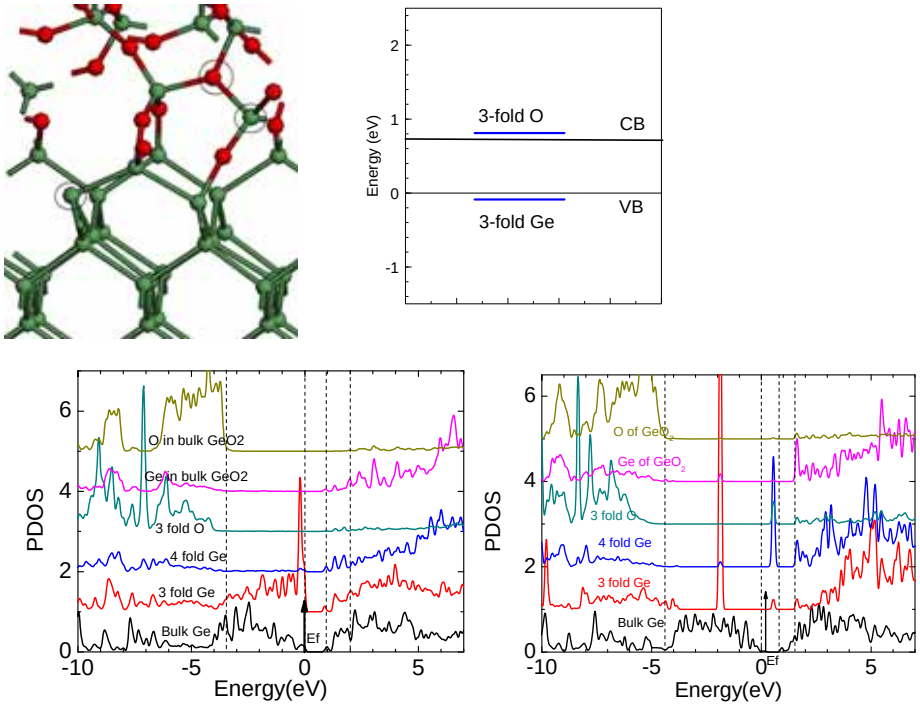

Energy (eV)
3-fold O
CB
VB
3-fold Ge
PDOS
O in bulk GeO2
Ge in bulk GeO2
3 fold O
4 fold Ge
3 fold Ge
Bulk Ge
Ef
Energy(eV)
O of GeO2
Ge of GeO2
3 fold O
4 fold Ge
3 fold Ge
Bulk Ge
Ef
Energy(eV)

Fig 82.

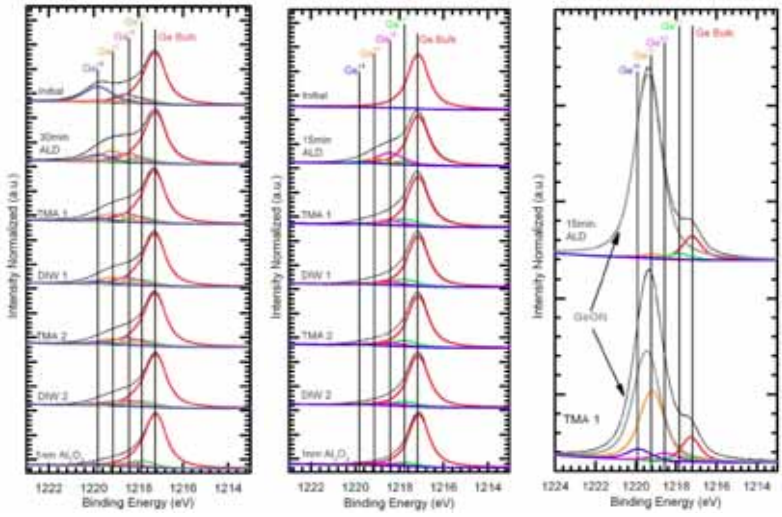

Intensity Normalized (a.u.)
Binding Energy (eV)
Intensity Normalized (a.u.)
Binding Energy (eV)
Intensity Normalized (a.u.)
GeON
TMA 1
Binding Energy (eV)

Fig 83.

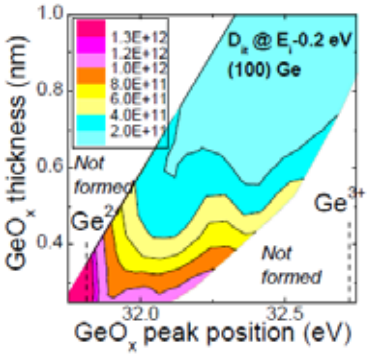


Fig 84

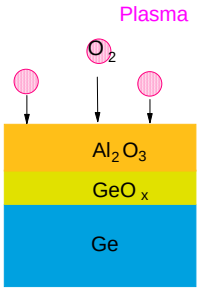


Fig 85

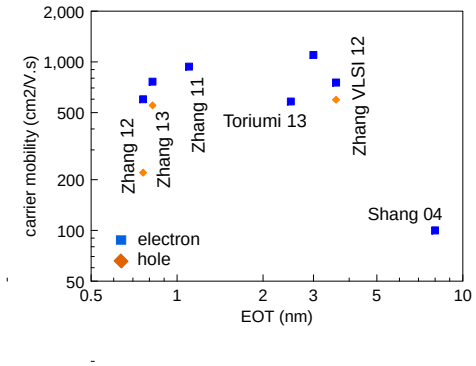


Fig 86