Aluminium oxide prepared by UV/ozone exposure for low-voltage organic thin-film transistors

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We have developed a gate dielectric for low-voltage organic thin-film transistors based on an

inorganic/organic bi-layer with a total thickness of up to ~ 20 nm. The inorganic layer is

aluminium oxide formed by UV/ozone treatment of aluminium layers. The organic layer is 1-

octylphosphonic acid. The preparation of aluminium oxide (AlO<sub>x</sub>) was studied with respect

to the threshold voltage of p-channel thin-film transistors based on thermally evaporated

pentacene. The results demonstrate that the threshold voltage decreases with increasing

UV/ozone exposure time. The threshold voltage varies by 0.7 V and the gate-source leakage

current by a factor of 10 as a function of aluminium oxide preparation. The breakdown

voltages of the bi-layer gate dielectrics vary between 5 and 12 V and the electrical breakdown

field is at least 5 MV/cm for all AlO<sub>x</sub> preparation conditions.

Key words: Organic thin-film transistor, pentacene, alkylphosphonic acid, aluminium oxide

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1

#### 1. Introduction

Flat panel displays and large area electronics based on flexible substrates are of great interest for the next generation electronic devices. Organic thin-film transistors due to their low-temperature processing and compatibility with plastic substrates have become an attractive choice for such devices. Here transistors with low operating voltages and high transconductance are needed for battery-operated applications. Several groups reported low-voltage organic thin-film transistors (OTFTs) by employing various ultra-thin gate dielectrics [1-9]. Here, the main dielectric requirements are low leakage current, high capacitance and breakdown voltage in excess of 5 V.

Organophosphonic acids due to their ability to form dense monolayers on metal oxide surfaces have been implemented previously into OTFTs [2, 5, 6, 9, 10]. AlO<sub>x</sub> can be prepared by sputtering, atomic layer deposition (ALD) or by exposing Al to oxygen plasma. Previous studies have shown that exposure of aluminium to ozone in high vacuum leads to a formation of aluminium oxide films with higher density and smaller 'pore' size when compared to oxygen exposure [11-12]. In our OTFTs the dielectric bi-layer is composed of AlO<sub>x</sub> and a 1-octylphosphonic acid. AlO<sub>x</sub> is prepared, for the first time, by oxidizing Al in a commercial UV/ozone cleaner in ambient atmosphere. AlO<sub>x</sub> preparation is studied with respect to the threshold voltage, gate-source leakage current, and the gate dielectric breakdown field of p-channel OTFTs based on thermally evaporated pentacene. In addition, AlO<sub>x</sub> layers with thicknesses up to  $\sim$  18 nm are studied to control the gate dielectric breakdown voltage in the OTFTs.

## 2. Experimental Procedures

TFTs have a bottom-gate, top source-drain contact structure shown in Fig. 1. The materials used for fabrication are: glass (Eagle 2000) as substrate, a 30-nm-thick aluminium

as gate contact,  $AlO_x$  coated with a 'monolayer' of 1-octylphosphonic acid as the gate dielectric, a 50-nm-thick pentacene as transistor island and a 50-nm-thick gold as source and drain.  $AlO_x$  was prepared by oxidation of the aluminium layers using UV/ozone cleaner enclosed under a Hepa filter in ambient atmosphere. Before the oxidation, part of the gate electrode (away from the transistor island) was coated by a 20-nm-thick gold layer to prevent oxidation in that area. Aside from the  $AlO_x$  preparation the remaining TFT layers, grown under high vacuum in a computer-controlled thermal evaporator (base pressure  $\sim 1x10^{-7}$  mbar), were identical in all sample sets.

Three sets of transistors (A, B, and C) were fabricated with the aim to optimize the preparation of aluminium oxide via UV/ozone exposure. Each set contained 6 samples and the  $AlO_x$  layer was varied within the set. Aside from  $AlO_x$  preparation, the samples within each set were prepared side by side. Each sample contained 4 capacitors (MIM structures) and 12 transistors with channel width of 1 mm and 4 different channel lengths of 30, 50, 70, and 90  $\mu$ m; total of 16 devices. Capacitors were used to measure the capacitance and the breakdown voltage of the gate dielectric bi-layer.

Set A and C were fabricated to investigate the effect of UV/ozone exposure time for fixed dielectric thickness. In set B the  $AlO_x$  thickness was varied while the UV/ozone exposure time was held at 60 minutes. In addition, the  $AlO_x$  thickness of sets A and C correspond to the lowest and the highest thickness in set B, respectively. Consequently, the gate dielectric in set C is about twice as thick as the one in set A.

AlO<sub>x</sub> in set A was fabricated by exposing the aluminium gate to UV/ozone for t = 2, 5, 10, 20, 40 or 60 minutes. Afterwards, a 15-Å-thick layer of aluminium was deposited on top of the created AlO<sub>x</sub> and UV/ozone oxidized for the same time as the gate electrode (see Fig. 2). This was needed to increase the thickness of AlO<sub>x</sub> and raise the breakdown voltage to above 5 V. Additional 15-Å-thick aluminium layers were sequentially deposited and oxidized

to increase further the  $AlO_x$  thickness in sets B and C. The number of 15-Å-thick aluminium layers is n. n=1 for set A and n=6 for set C. In set B n is varied from 1 to 6 while the UV/ozone exposure time t is fixed at 60 minutes. Except  $AlO_x$  all other TFT layers in all three sets were prepared in the same manner.

After fabrication, all samples underwent the same storage, handling and electrical characterization to provide them with identical history. The device measurements were performed with Agilent B1500A semiconductor device analyzer in ambient air. The transistor transfer and output characteristics were measured in a sweep mode. The capacitance and the breakdown voltage of the gate dielectric were measured using the capacitor structures fabricated alongside the TFTs. The capacitance was measured as a function of frequency from 1 kHz to 5 MHz. Capacitance values at 1 MHz were used to calculate the field-effect mobilities. The breakdown voltage is taken as voltage at which the current reaches 100  $\mu$ A even though higher current had to be passed through the MIM structures to cause a non-recoverable effect. All transistors were measured three times before the data was taken. Although the variation in the transistor performance was not studied, the transistors exhibited high yield and similar performance.

## 3. Results

The transfer and output characteristics of TFT with n = 1 and t = 2 mins are shown in Fig. 3. The TFT transfer characteristics for  $V_{ds} = -0.1$  V and -3 V are shown in Fig. 3(a). The drain-source current  $I_{ds}$  as a function of drain-source voltage  $V_{ds}$  for several gate-source voltages  $V_{gs}$  is shown in Fig. 3(b). The off-current is  $\sim 1 \times 10^{-12}$  A and the on-off current ratio is  $\sim 10^6$ . The threshold voltage and field-effect mobility calculated using MOSFET equations in saturation regime are -1.92 V and 0.09 cm<sup>2</sup>/Vs. The inverse subthreshold slope is 106 mV/decade. Even though this transistor represents the least favourable condition of AlO<sub>x</sub>

preparation, its gate-source leakage current  $I_{gs} < 10^{-9}$  A ( $< 4 \times 10^{-7}$  A/cm<sup>2</sup>) for  $V_{ds} = -0.1$  V and  $V_{gs} = -3$  V. The remaining samples exhibit lower  $I_{gs}$ .

Fig. 4 shows the threshold voltages for sets A, B and C. In set A (Fig. 4(a), n=1) the threshold voltage decreases as the UV/ozone exposure time increases from 2 to 60 minutes and this behaviour is independent of the channel length of the transistor. The decrease in the threshold voltage is faster for shorter exposure times and slower after a 20-minute UV/ozone exposure. Fig. 4(b) (set B, t = 60 minutes) gives the threshold voltages as a function of AlO<sub>x</sub> thickness for different channel lengths. Initially there is a slight decrease in the threshold voltage from  $\sim$  -1.45 V to  $\sim$  -1.35 V as the AlO<sub>x</sub> thickness increases and it remains unchanged for AlO<sub>x</sub> thickness higher than  $\sim 110$  Å (n=2). Transistors with different channel lengths show similar behaviour. Fig. 4(c) shows the threshold voltages for thicker  $AlO_x$  layers (n=6) as a function of UV/ozone exposure time. (Note that the scale on x-axis is reversed.) Here the UV/ozone exposure time has similar effect on the threshold voltage as for transistors with thinner AlO<sub>x</sub> shown in Fig. 4(a). However, the data points are shifted downward by  $\sim 0.2 \text{ V}$ . The right-most data points in Fig. 4(a) and the left-most data points in Fig. 4(b) correspond to the same samples prepared at different times. The same applies to the right-most data points in Fig. 4(b) and the left-most data points in Fig. 4(c). This indicates good reproducibility of our fabrication process. When calculating the mean and the standard deviation of the threshold voltages obtained for different channel lengths of the same transistors, the standard deviation of  $\pm$  0.03 V is obtained for data in Figs. 4(a) and 4(b), and this value increases to  $\sim$  $\pm$  0.08 V for short UV/ozone exposure time and n=6 (Fig. 4(c)). To summarize, the threshold voltage varies between  $\sim$  -1.2 V and  $\sim$  -1.9 V as a function of the AlO<sub>x</sub> preparation.

Fig. 5 shows the gate dielectric breakdown voltage of the three sets of samples. The breakdown voltage does not change much with increasing UV/ozone exposure time, although it reaches slightly higher values for longer UV/ozone times (see Figs. 5(a) and 5(c)).

Consequently, the 20-minute UV/ozone exposure leads to improved gate dielectric. Fig. 5(b) shows a gradual increase in the breakdown voltage with increasing  $AlO_x$  thickness. As expected, the breakdown voltage rises from  $\sim$ 5 V to  $\sim$ 12 V when the  $AlO_x$  thickness increases from 93 to 194 Å. In all cases the electric breakdown field is at least 5 MV/cm.

## 4. Discussion

The primary factor that controls the threshold voltage in the OTFTs is the UV/ozone exposure time during the  $AlO_x$  preparation. Here, the longer exposure time leads to OTFTs with lower threshold voltage and slightly higher dielectric breakdown voltage. The thickness of  $AlO_x$  has only minor effect on the threshold voltage of OTFTs. Comparing the data in Fig. 4(a) (set A) and Fig. 4(c) (set C) one can see that the UV/ozone exposure time has similar effect on the threshold voltage even though the  $AlO_x$  thickness in sets A and C is quite different.

The dielectric breakdown voltage is not very sensitive to the UV/ozone exposure time, while the threshold voltage varies strongly with the exposure time. This indicates that while the gate dielectrics prepared with different exposure times exhibit similar catastrophic electrical failure, their properties with respect to built-in or injected charge are quite different. Consequently, UV/ozone exposure times shorter than 20 minutes lead to inferior oxide formation. This can be seen from higher threshold voltages (Fig. 4), slightly lower breakdown voltages (Fig. 5(c)), and larger standard deviation in the threshold voltages (see above).

The threshold voltage of our transistors ranges from  $\sim$  -1.2 V to  $\sim$  -1.9 V which is somewhat higher than values published by the others [6]. This might be result of an unoptimized growth of 1-octylphosponic acid. Additional work is underway to study the

material properties of AlO<sub>x</sub> prepared via UV/ozone oxidation and to improve the transistor performance.

#### 5. Conclusions

We developed new inorganic/organic bi-layer gate dielectric with a total thickness of up to  $\sim 20$  nm for low-voltage organic thin-film transistors. The inorganic layer is aluminium oxide (AlO<sub>x</sub>) formed by UV/ozone treatment of aluminium layers. The organic layer is  $\sim 10$ -Å-thick 1-octylphosphonic acid. The preparation of AlO<sub>x</sub> was studied with respect to the threshold voltage, gate-source leakage current, and the gate dielectric breakdown field of p-channel thin-film transistors based on thermally evaporated pentacene. The results demonstrate that the threshold voltage decreases with increasing UV/ozone exposure time and AlO<sub>x</sub> thickness and varies by  $\sim 0.7$  V depending on the AlO<sub>x</sub> preparation. Transistors exhibit threshold voltages between  $\sim -1.2$  and  $\sim -1.9$  V and the gate-source leakage currents between  $10^{-10}$  and  $10^{-9}$  A ( $4x10^{-8}$  and  $4x10^{-7}$  A/cm²) for drain-source voltage of -0.1 V and gate-source voltage of -3 V. As the thickness of the gate dielectric increases, the breakdown voltage raises from  $\sim 5$  to  $\sim 12$  V. Regardless of AlO<sub>x</sub> preparation method the gate dielectric breakdown field is at least 5 MV/cm.

# Acknowledgement

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# Figure captions:

Figure 1. Cross-section of a thin-film transistor.

Figure 2. UV/ozone treatment procedure for AlO<sub>x</sub> formation.

Figure 3. Transfer (a) and output (b) characteristics for transistor with n = 1 and UV/ozone exposure time of 2 min.

Figure 4. Threshold voltage as a function of  $AlO_x$  preparation for sets A (a), B (b) and C (c). Note the reversed x-axis in (c). The channel width is 1mm. The ovals link transistors prepared at different times following the same fabrication procedure.

Figure 5. Gate dielectric breakdown voltage for sets A (a), B (b) and C (c). Note the reversed x-axis in (c). The ovals link capacitors prepared at different times following the same fabrication procedure. Each data point represents a mean of four capacitor measurements. The standard deviations are  $\sim \pm 0.2$  V and are not visible on the graph.

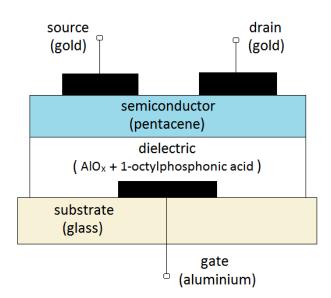
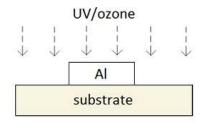
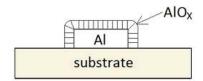


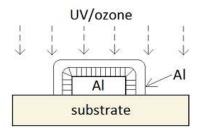
Fig. 1.



a) expose Al gate to UV/ozone



b) formation of  $\,AIO_{X}\,$  on the surface of  $AI\,$ 



c) deposition of 15 Å of Al (n=1) and UV/ozone exposure

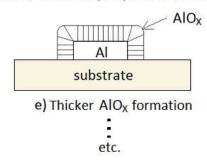


Fig. 2.

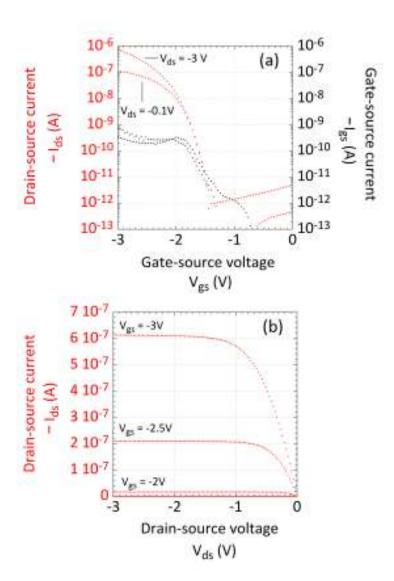


Fig. 3.

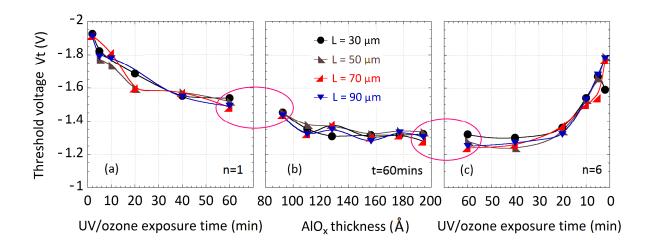


Fig. 4.

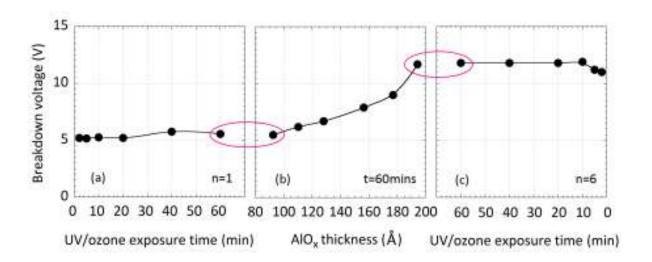


Fig. 5.