



High capacity organic memory structures based on PVP as the insulating layer

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Abstract

The electrical behaviour of organic memory structures based on gold nanoparticles (AuNPs) and poly 4-vinylphenol as the gate dielectric are reported in this work. Metal–insulator–semiconductor (MIS) and thin film transistor structures were used to fabricate the control and memory devices. The drain and source electrodes were fabricated by evaporating 50 nm gold, and the gate electrode was made from 50 nm-evaporated aluminium on a clean glass substrate. Thin films of AuNPs embedded within the insulating layer were used as the floating gate. All memory devices exhibited clear hysteresis in their electrical characteristics [capacitance–voltage ($C-V$) for MIS structures as well as output and transfer characteristics for transistors]. Both structures were shown to produce reliable and large memory windows by virtue of high capacity. The hysteresis in the output and transfer characteristics and shifts in the threshold voltage of the transfer characteristics as well as flat-band voltage shift in the MIS structures were attributed to the charging and discharging of the AuNPs floating gate. Memory window of 38 V was achieved by scanning the applied voltage of the MIS structure between 40 and -40 V. Similarly, a memory window of 27 V was achieved for the TFT-based memory structure. Under an appropriate gate bias of 1 s pulses, the floating gate is charged and discharged, resulting in significant threshold voltage shifts. Pulses of as low as 5 V resulted in a clear write and erase states.

1 Introduction

Inorganic gate insulators such as SiO_2 are prone to crack under the stress caused by bending of substrates. Due to the demand for portable electronic devices, polymer gate insulators became more suitable for fabricating organic thin film transistors (OTFTs) on plastic substrates. Garnier et al. reported first all-organic transistors with a polyester gate insulator [1]. Afterwards, OTFTs received a great interest due to their many unique advantages, such as low cost solution process, light weight, flexible large area electronics applications, and solution process ability [2–6]. The main limitations associate with traditional OTFTs and memory

devices are high operating voltage, low mobility, poor interface between the insulating layer and the organic semiconductor and high contact resistance. For that reason it is important to consider these parameters in the design and fabrication of organic devices. Hence, for the applications that require high current output, such as switching of organic light-emitting diodes, OTFTs are still not the suitable candidates [7]. Since the field-induced current is proportional to the field-induced charge density and carrier mobility, one way to overcome this problem is to use high-dielectric-constant gate insulators [8, 9], which can enhance the field-induced carrier density. Also, the morphology of the organic semiconductors at the interface with dielectric layers plays a crucial role in the performance of the devices [10]. The morphology of the evaporated pentacene is dependent on the surface energy of the substrate which is grown on. Because of simple processing via spin-coating or casting, and ready tuning of the surface chemical properties [11], polymeric dielectrics have recently been employed as OTFT gate insulators that afford superior performance in pentacene-based OTFTs versus those fabricated with SiO_2 insulators [12]. The low surface energy of poly4-vinylphenol (PVP) was reported by other researchers to be the most suitable as an

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organic dielectric for the growth of pentacene thin film [13]. This is due to the three dimensional growth and larger grain size of pentacene when deposited on thin layer of PVP [14, 15].

Other applications associated with portable electronics such as organic solar cells [16], organic thin film transistors (OTFTs) [17] and light emitting displays [18] have been evaluated in the last two decades. Organic memory devices play an important part in plastic and flexible electronic applications [19], which lead to extensive research in this field. Organic memory devices based on charge storage in bistable switching [20–22], metal–insulator–semiconductor structures (MIS) [23–26], and organic thin film memory transistors (OTFMTs) [27–29] have been reported in recent years. The main structure to achieve fast and high capacity memory is the floating gate-based memory devices; where a thin film of a floating gate serves as the charge storage element in a transistor or MIS structure [29, 30].

Building on our earlier research which demonstrated the use of nanoparticles in organic memory structures [30, 31], we report on the use of PVP thin film as the insulating layer in OTFMTs. We employ the performance of non-volatile memory effects of gold nanoparticles (AuNPs) based structures. Simple and low-cost self-assembly technique was used for the deposition of AuNPs as the charge storage element. Achieving a large memory window, which gives an indication of the potential for high-density charge storage, was the major feature of this work.

2 Experimental

All the materials used were purchased from Sigma-Aldrich. The schematic diagram for the structure of Al/PVP/AuNPs/PVP/pentacene/Au memory device is shown in Fig. 1. The preparation of the gold nanoparticles (AuNPs) solution has been described previously [31]. The device was fabricated by thermally evaporating 70 nm thickness of an Al gate electrode through a shadow mask onto a clean glass substrate. 25% (wt) of poly 4-vinyl phenol (PVP) solution in

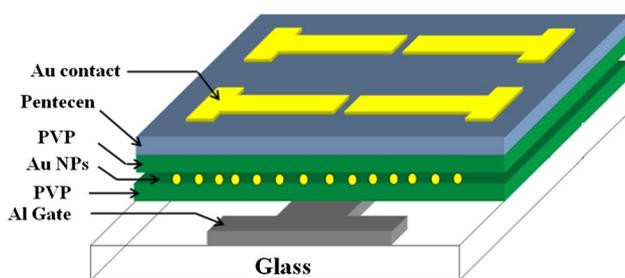


Fig. 1 Schematic diagram of Al/PVP/AuNPs/PVP/pentacene/Au memory structure

isopropanol (IPA) was spin coated on top of the gate electrode to a thickness of about 350 nm and cured at 80 °C for 10 min to form a uniform layer. The floating gate, AuNPs, was deposited using the self-assembly technique as described previously [31]. In brief, the glass substrates were placed in a dilute solution of (3-aminopropyl)-trimethoxysilane (APTMS) (0.1 ml of APTMS in 1 ml methanol) for about 4 h before rinsing with methanol. The substrates were subsequently immersed in the Au solution for 20 min and were rinsed with water. Prior to deposition of the pentacene semiconducting layer, another thin film of PVP was deposited onto the floating gate. Pentacene was thermally evaporated at a rate of 0.03 nm s⁻¹, through a shadow mask to a thickness of 50 nm. Following the deposition of pentacene, the source and drain contacts were defined by thermal evaporation of 50 nm of Au through a shadow mask after about 7 days of the pentacene evaporation. The channel width (*W*) and length (*L*) were 2670 μm and 198 μm, respectively. Control devices without Au nanoparticles were also fabricated for comparison. Double sweep capacitance voltage (*C*–*V*) measurements were carried out using a LCR Bridge (HP4192) at 100 kHz and a typical 2 V s⁻¹ scan rate to investigate the memory behaviour of the specimens produced. Double sweep current (*I*) versus voltage (*V*) characteristics of the transistors were recorded at room temperature (21 ± 2 °C) using a Keithley 4140B picoammeter.

3 Results and discussion

As the surface morphology of the organic semiconductor at the interface with dielectric layers play a crucial role in the performance of organic devices, the topographies of the organic thin films have been investigated to establish the required evaporation parameters that lead to fabricate high-performance pentacene-based devices. AFM images were used to extract the surface morphology of the deposited pentacene film as a function of PVP for different thicknesses. Figure 2 shows the AFM image of the 50 nm pentacene film evaporated with deposition rate of 0.03 nm s⁻¹ on 350 nm of PVP dielectric layers. The figure shows a clear polycrystalline structures of pentacene with large, uniform and condensed grains. The figure shows the morphology with scan sizes of (a) 5 μm, and (b) 2 μm. The average grain size of pentacene was estimated to be in the range of 1.46 μm². The large grain sizes of the organic semiconductor is an important parameter for higher mobility and allows higher current when used as the active layer in organic transistors. In contrast, smaller and completely separated grains were observed when pentacene was evaporated on thinner layer of PVP. Such films resulted in very poor channel conductivity and almost no drain source current even at very high gate

Fig. 2 AFM images of deposited pentacene film on PVP with scan area size of **a** 5 μm and **b** 2 μm

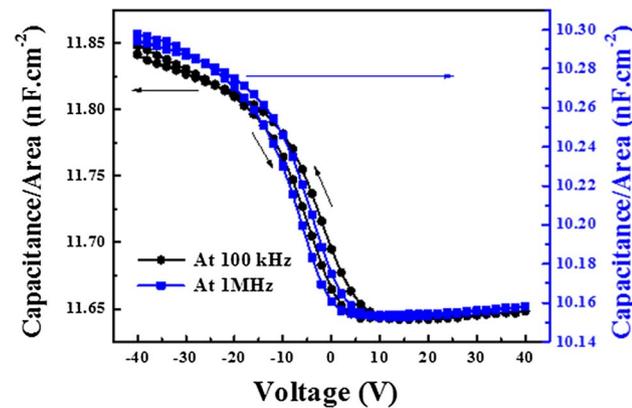
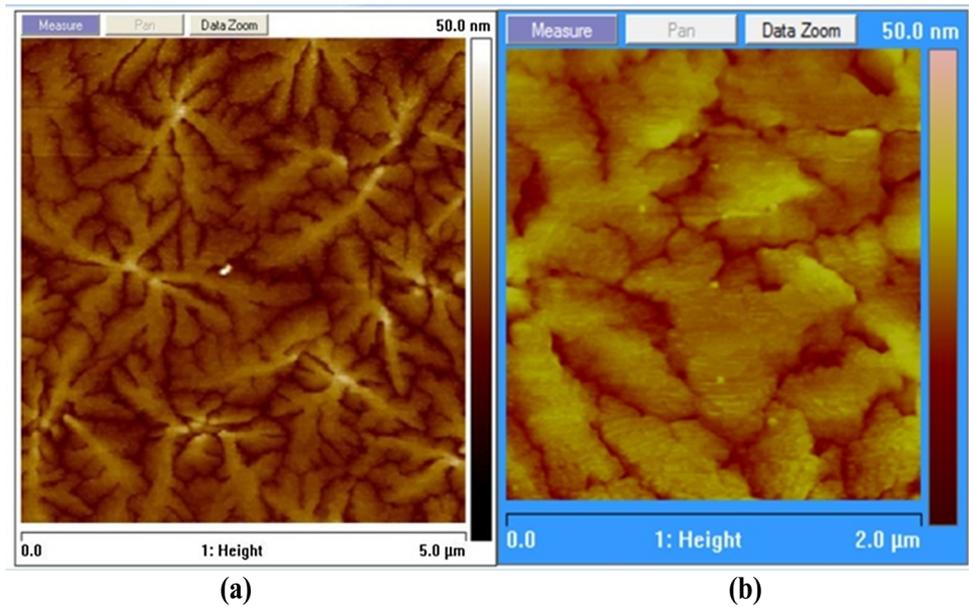


Fig. 3 C - V characteristic curves of double voltage sweep ± 40 V for Al/PVP/pentacene/Au structure

voltages. Therefore, all devices described in this work were based on 350 nm thick PVP insulating layers.

The C - V characteristics for the control MIS structure is shown in Fig. 3. The measurements were performed at low and high frequencies (100 kHz and 1 MHz) for comparison. In each measurement, the double scan started from a negative gate voltage, swept towards inversion region, and then back to negative voltages. The C - V curve for the control device with a reference structure of Al/PVP/pentacene/Au reveals the typical characteristics of an MIS structure based on a p-type semiconductor, with a flat-band voltage (V_{fb}) of about -16 V (with no effect of the measurement frequency on the value of flat-band voltage) and full semiconductor depletion at about 7 V.

Furthermore, the slope lines of the curves in the depletion region occurred between about -20 and 5 V, which indicates

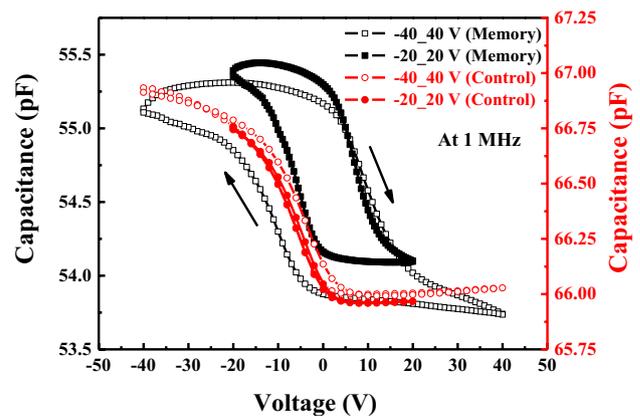


Fig. 4 C - V characteristic curves of double voltage sweep ± 20 V and ± 40 V for Al/PVP/AuNPs/PVP/pentacene/Au MIS memory structures at 1 MHz

a higher interface state density, may exist at PVP/pentacene interface. At the frequency measurement of 1 MHz, negligible hysteresis was evident at the voltage sweep range of ± 40 V. The capacitance in accumulation for this device was 66.8 pF and the thickness of the insulator was estimated to be 350 nm. The doping concentration (N_a) of pentacene was estimated to be $1.3 \times 10^{17} \text{ cm}^{-3}$.

The additional layers of AuNPs within the insulating layer to form an Al/PVP/AuNPs/PVP/pentacene/Au structure produced a very small change in the flat-band voltage as shown in Fig. 4. Furthermore, on reversing the direction of the voltage scan, significant hysteresis and shift in the flat-band voltage were observed in the C - V curve with a large memory window, which is indicative of the charge storage in the AuNPs layer. For comparison, Fig. 4

represents the C – V characteristics for the control and memory devices using double voltages sweep of ± 20 V and ± 40 V with 1 V s^{-1} scan rate, starting from accumulation to deep depletion and back to accumulation at 1 MHz. The area of this memory device was $6.5 \times 10^{-3} \text{ cm}^2$.

The flat-band voltage shifted to a more positive value after applying accumulation voltages, resulting in a clockwise hysteresis as electrons originating from the Al gate become trapped in the AuNPs layer. The hysteresis in the C – V curve at 1 MHz showed a memory window ΔV of about 18 and 38 V at voltage sweeps ± 20 V and ± 40 V, respectively, indicating a clear increase of stored charges as the applied voltage was increased. The value of capacitance of this memory device was less than of the control device, as depicted in Fig. 4. Another important feature was that the hysteresis curves were centred close to 0 V, which is an important advantage for the memory devices, as it indicates that the devices may operate at lower voltages. The thickness of the insulating layer was almost doubled due to the second PVP layer deposited on top of the AuNPs film to complete their confinement. The presence of AuNPs did not change the PVP dielectric properties such as permittivity. The amount of charge stored (Q) in the AuNPs can be estimated from the capacitance in the accumulation region C_i , which give a value of 8.9×10^{-9} , $8.5 \times 10^{-9} \text{ F cm}^{-2}$, and the change in flat-band voltage (ΔV_{FB}) was 18.5 and 39 V for ± 20 and ± 40 V sweep range, respectively. Accordingly, the number of charge carriers stored was estimated to be $2.07 \times 10^{12} \text{ cm}^{-2}$. As shown in Fig. 4, if a voltage less than -30 V is applied to the gate of the memory structure, the device will be in the high accumulation capacitance and thus perform the write operation of the ON state. On the other hand if a voltage of higher than 20 V is applied (deep depletion region) the erase operation will perform and the device turn to OFF state. Applying a voltage between -30 V and 20 V represents the reading voltage range at which the capacitance value indicates if the device in the ON or OFF state.

The performance of nonvolatile organic thin film memory transistor (OTFMT) is also investigated. Figure 5 shows the plots of the electrical characterization (a) output and (b) transfer characteristics of PVP-based OTFT. In each measurement, forward and reverse voltage scans are performed. The output characteristic exhibits linear behaviour at low V_{DS} , and the saturation behaviour in this device is observed at high V_{DS} and low V_{GS} values (V_{GS} from 0 to ~ -30 V, as shown in Fig. 5a). Figure 5b shows the transfer characteristic of the device, measured at $V_{\text{DS}} = -25$ V. The plots are given in the form of both $(I_{\text{DS}})^{1/2}$ and $\log(I_{\text{DS}})$ as a function of V_{GS} . Negligible hysteresis is evident on reversing the bias scan direction; this may be related to a relatively clean interface between the PVP and the pentacene. The field-effect mobility, on/off current ratio and

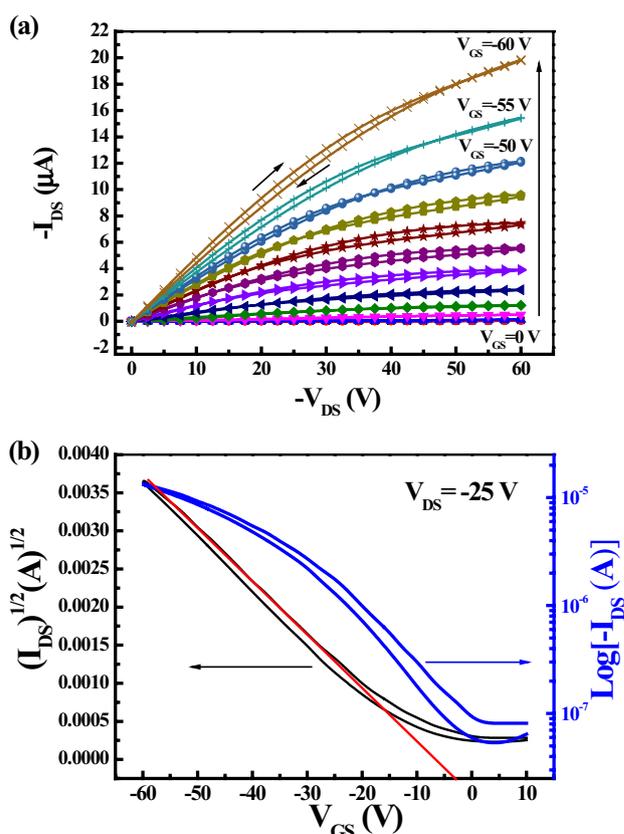


Fig. 5 The a output and b transfer characteristics of PVP-based OTFT

threshold voltage for this device were $0.65 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, 2.66×10^2 and -7 V respectively.

Figure 6 shows the characteristics of OTFMT for devices using AuNPs as the trapping layer, and the characteristics of the OTFT control device associated with the memory structure (blue colour in Fig. 6). Both forward and reverse scans are shown in each measurement, at voltage scan rate of 1 V s^{-1} . Figure 6a shows the output characteristics of the memory and control devices which exhibited good linear behaviour at low V_{DS} values as well as good saturation region at high V_{DS} with a gate voltage of -40 V. The transfer characteristic for the memory (initial curve, before programming pulses were applied) and control devices is shown in Fig. 6b with $V_{\text{DS}} = -10$ V. The OTFT devices exhibited negligible hysteresis in both characteristics, while a large memory window is evident on reversing the voltage scan direction of OTFMT. The output characteristic shows hysteresis window of $\Delta V = 23$ V, similar behaviour was observed for the transfer characteristics with $\Delta V = 27$ V. The hysteresis is the result of the charging and discharging of the AuNPs floating gate with the a defined applied voltages; when a high negative bias is applied to the gate, electrons will be injected from the gate into the floating gate through the

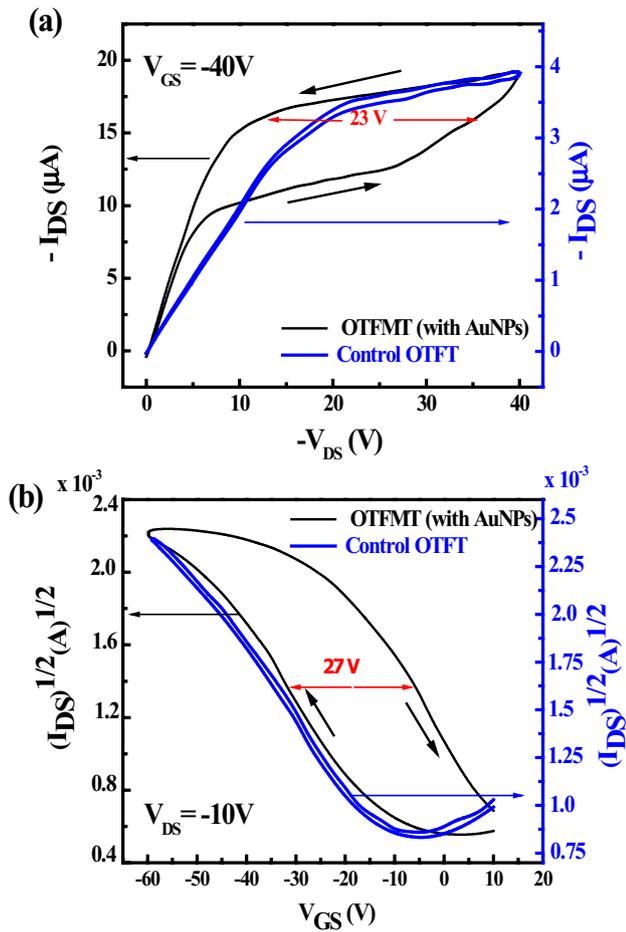


Fig. 6 **a** The output and **b** transfer characteristics of the PVP-based OTFT (control device) and OTFMT device. (Color figure online)

lower insulating layer, charging up the AuNPs floating gate and programming the memory device. On the other hand, when a high positive voltage is applied to the gate, electrons are ejected from the floating gate through the bottom insulating layer (erase process).

The field-effect mobility, μ , of the prepared memory device is calculated to be in the region of $0.048 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. A lower mobility value is recorded for OTFMTs than that in OTFT devices ($\mu = 0.65 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$); this clearly indicates that AuNPs floating gate has influenced the current flow in the transistor channel resulting in lower mobility due to the trapped charge carriers in the floating gate [31]. The amount of charge stored in the gold nanoparticles Q is approximately $1.2 \times 10^{12} \text{ cm}^{-2}$ as the value of $C_i = 8.5 \times 10^{-9} \text{ F cm}^{-2}$ and $\Delta V_T = 23 \text{ V}$. The magnitude of charge storage has similar values to those stored in the MIS memory structures as described earlier from Fig. 4.

The charging effect by the application of negative and positive bias pulses to the gate are investigated and shown in Fig. 7. The memory operation was characterized by

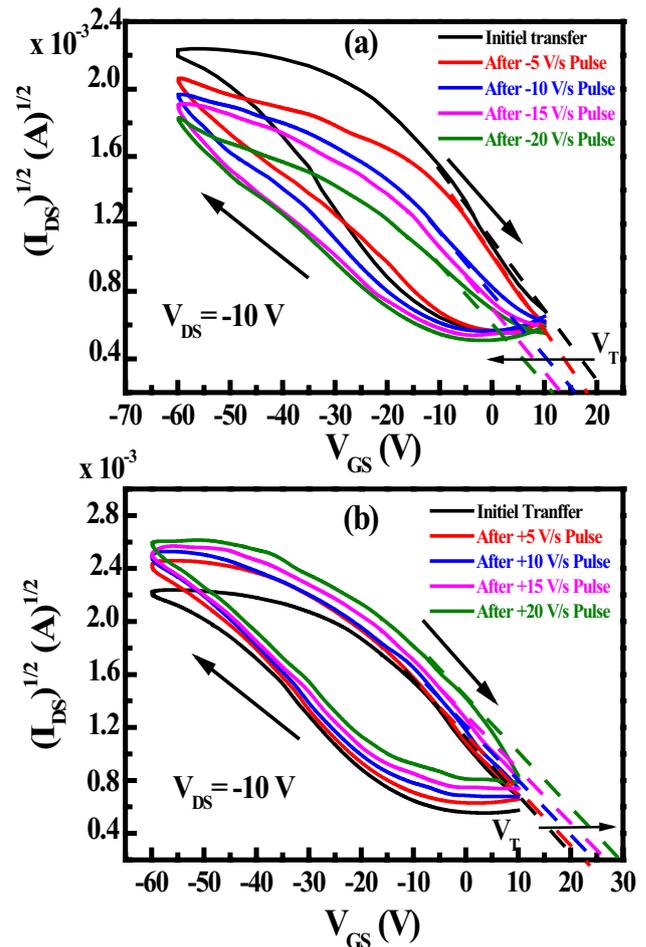


Fig. 7 The effect of **a** negative and **b** positive pulses on transfer characteristics for PVP-based OTFMT

measuring the threshold voltage shift after positive and negative voltage pulses were applied to the gate electrode. The magnitude of the voltage pulses were increased for each step but the pulse duration was kept at 1 s with V_{DS} maintained at 0 V. A clear shift to higher negative threshold voltages is observed for the application of negative pulses (write state) as shown in Fig. 7a, whereas positive shifts of threshold voltages is observed due to the application of positive pulses (erase) as shown in Fig. 7b.

The transfer characteristics of the prepared device were measured after each application of the voltage pulse to calculate the shift in the threshold voltage compared to the unstressed devices. Figure 8a shows the programming pulses (write/erase), where the threshold voltage shifts as the result of the applied negative and positive pulses. There was V_T shift of around 3 V after the application of 5 V bias pulses for 1 s as shown in Fig. 8a. Therefore, clear charging and discharging of the charge carriers occurred in the bulk and/or interfaces of the PVP gate dielectric layer. The shift in

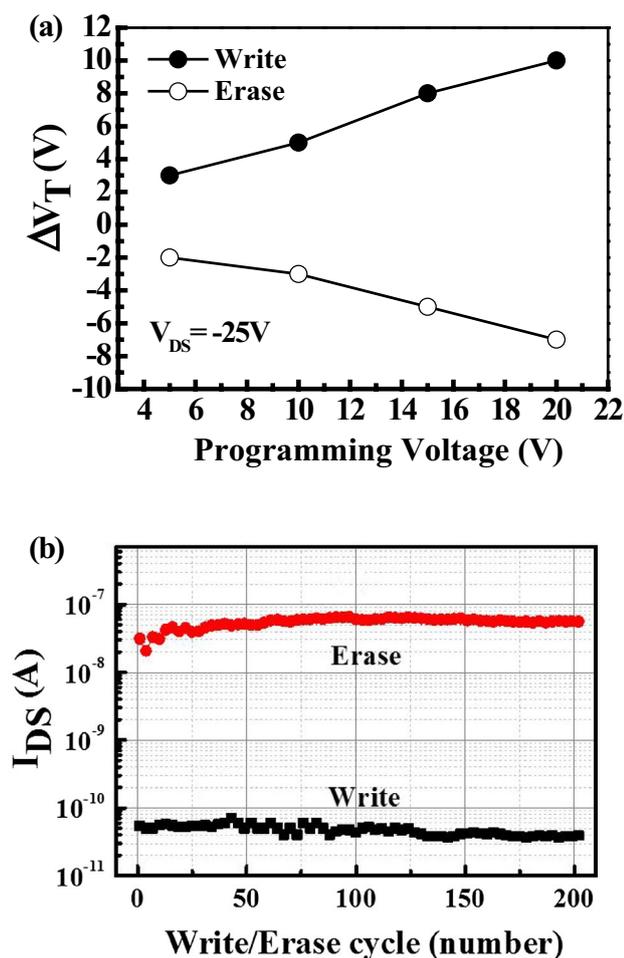


Fig. 8 **a** Programming characteristics and **b** retention current for the PVP-based OTFMT

threshold voltage increases with the increase in the applied voltage pulses. Clear memory window behaviour was shown for voltage pulses of 5 V, as shown in Fig. 8a. Such operating voltages are lower than reported values for similar configurations [32, 33], and for voltages applied to OFET memory devices built on silicon wafers [34]. The write/erase processes were defined as the states associated with the electrons being trapped or de trapped after the application of the negative or positive gate biases [32].

To evaluate the endurance properties of the OTFMTs, the nonvolatile behaviour was investigated by monitoring the drain–source current after the application of voltage pulses for write and erase states. The write/erase operations were repeated with continuous application of bias pulses of ± 20 V for 1 s. After a certain number of write/erase cycles the reading process was carried out to monitor the change in drain current. There are three write/erase cycles in the first period with an initial decay of 60 s for each cycle, and then the drain current is measured by an applied reading bias of -10 V. After a retention time of about 60 min, the

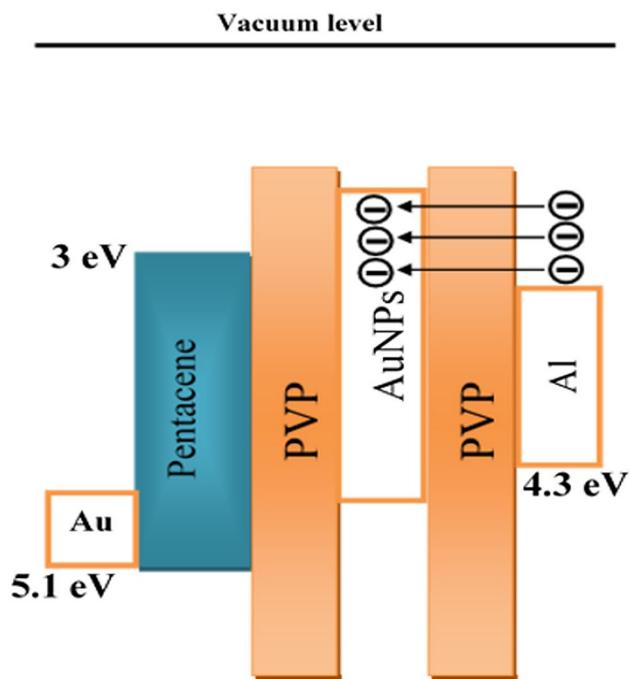


Fig. 9 Schematic diagram of the energy bands for the OTFMT

write/erase operations were repeated (two cycles, and were followed with a reading process). This process was repeated for over 200 cycles and the I_{DS} value of the memory transistor was measured accordingly. Figure 8b shows the values of the I_{DS} as a function of cycles. It is clear that the current did not change dramatically after more than 200 cycles and it is easy to distinguish if the device in write or erase state. The average current recorded for the write and erase states are 5.5×10^{-11} A and 5×10^{-8} A, respectively.

The energy band diagram of the Al/PVP/AuNPs/PVP/pentacene/Au structure were considered for investigation. Figure 9 represents the relative energy diagrams for the materials used in the fabrication of the memory device, where the work functions for Al and Au are 4.3 and 5.1 eV, respectively [12]. The highest-occupied molecular orbital (HOMO) and the lowest-unoccupied molecular orbital (LUMO) levels of pentacene are -5 and -3 eV [12], respectively. The charging process shown in Fig. 9 for a negative bias applied to the gate electrode. Electrons from the Al gate injected through the PVP and captured by the AuNPs memory stack. The capture of electrons leads to lower negative voltage required to turn the transistor ON which means lower negative threshold voltage.

4 Conclusions

Organic memory devices based on AuNPs as charge storage elements are fabricated and characterised, and compared to the control structure (without AuNPs). In this work we have demonstrated that PVP can be employed as a reliable insulator in organic transistors and memory devices. The electrical parameters of the OTFMT device which were investigated in this study are 5 V, $0.048 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, -5 V , 22 V , 0.27×10^3 , 23 V and $1.2 \times 10^{12} \text{ cm}^{-2}$ for charging pulse, mobility, forward threshold voltage (V_{TF}), reverse threshold voltage (V_{TR}), On/Off ratio, memory window and charge capacity (Q) respectively. The floating gate may be charged and discharged resulting in a clear shift in the threshold voltage of the transistors, and flat-band voltage of the MIS structure, by applying appropriate negative or positive voltages pulses. Data retention properties for the memory devices were extracted from the extrapolation of the measured data retention characteristics, which showed the stored information was maintained for long time and the hysteresis may be used as the basis of a stable memory at room temperature. The data retention and endurance measurements confirmed that the pentacene based OTFMTs devices exhibited mechanical stability as well as good electrical reliability. Furthermore, these data retention and endurance measurements confirmed the non-volatile memory properties for prepared device.

The results augur well for the development of organic electronic circuits working at low operating voltages.

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