THE DESIGN AND IMPLEMENTATION OF LOW-POWER CMOS RADIO RECEIVERS

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To all of our teachers, and to our parents, who were the best teachers of them all.

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Foreword

It is hardly a profound observation to note that we remain in the midst of a wireless revolution. In 1998 alone, over 150 million cell phones were sold worldwide, representing an astonishing 50% increase over the previous year. Maintaining such a remarkable growth rate requires constant innovation to decrease cost while increasing performance and functionality.

Traditionally, wireless products have depended on a mixture of semiconductor technologies, spanning GaAs, bipolar and BiCMOS, just to name a few. A question that has been hotly debated is whether CMOS could ever be suitable for RF applications. However, given the acknowledged inferiority of CMOS transistors relative to those in other candidate technologies, it has been argued by many that "CMOS RF" is an oxymoron, an endeavor best left cloistered in the ivory towers of academia.

In rebuttal, there are several compelling reasons to consider CMOS for wireless applications. Aside from the exponential device and density improvements delivered regularly by Moore's law, only CMOS offers a technology path for integrating RF and digital elements, potentially leading to exceptionally compact and low-cost devices. To enable this achievement, several thorny issues need to be resolved. Among these are the problem of poor passive components, broadband noise in MOSFETs, and phase noise in oscillators made with CMOS. Beyond the component level, there is also the important question of whether there are different architectural choices that one would make if CMOS were used, given the different constraints.

The work described in this book, based on Dr. Shaeffer's doctoral research at Stanford, is a significant first step toward answering many of these questions. This single-chip GPS receiver actually outperforms existing implementations in other technologies, while consuming less power. Furthermore, it is more highly integrated. As is made apparent in the chapters to come, this performance is made possible by a careful choice of architecture, and a detailed study of how to approach performance limits consistently. Important advances in understanding

how to design low-noise amplifiers (LNAs) and wide dynamic range filters in CMOS form the core contributions of this work. Just as important are the scaling properties elucidated by this research, for it makes it clear that both RF and digital performance will improve together, assuring that CMOS will become an important medium in which to realize RF circuits and systems.

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Finally, Dr. Shaeffer would like to express his gratitude for the steadfast support of his wife, Deborah Shaeffer, who patiently endured the many hours of preparation that went into this book.

Introduction

Derek K. Shaeffer

Wireless communications research has experienced a remarkable renaissance in the last decade. The advent of cellular telephony has driven much of the recent research activity, but substantial efforts have also focused on other wireless applications, such as cordless telephones and, more recently, the Global Positioning System.

The primary goal of this book is to explore techniques for implementing wireless receivers in an inexpensive complementary metal-oxide-semiconductor (CMOS) technology. Although the techniques developed apply somewhat generally across many classes of receivers, the specific focus of this work is on the Global Positioning System (GPS). Because GPS provides a convenient vehicle for examining CMOS receivers, a brief overview of the GPS system and its implications for consumer electronics is in order.

The GPS system comprises 24 satellites in low earth orbit that continuously broadcast their position and local time [4]. Through satellite range measurements, a receiver can determine its absolute position and time to within about 100m anywhere on Earth, as long as four satellites are within view. The deployment of this satellite network was completed in 1994 and, as a result, consumer markets for GPS navigation capabilities are beginning to blossom. Examples include automotive or maritime navigation, intelligent hand-off algorithms in cellular telephony, and cellular emergency (911) services, to name a few.

Of particular interest in the context of this book are embedded GPS applications where a GPS receiver is just one component of a larger system. Widespread proliferation of embedded GPS capability will require receivers that are compact, cheap and low-power. For such goals, the benefits conveyed by integration are self-evident: minimization of the number of off-chip components (particularly the number of expensive passive filters), improved form factor, reduced cost and ease of design.

For further cost reduction, it is interesting to consider implementation in a CMOS technology. Due to the huge capital investment in CMOS, it is only natural to consider whether the technology's shortcomings can be mitigated, making it attractive in an arena that historically has been dominated by more expensive silicon bipolar and GaAs MESFET technologies.

Meeting the goal of receiver integration in an inferior technology requires innovation in architectures, circuits and device modeling. Collectively, the scope of these problems is broad, but a successful approach will bring clear benefits for consumer electronics. And so, these considerations motivate the present research into highly integrated CMOS GPS receivers that forms the subject of this book.

The following chapters delve into the problems of radio receiver design in detail. The ultimate goal is the design and implementation of a 115mW CMOS GPS receiver in a **0.5-μm** CMOS process. The techniques developed along the way are, however, broadly applicable to other wireless systems.

Chapter 1 begins with an overview of radio receiver architectures by presenting fundamental concepts through the vehicle of historical examples. Then in Chapter 2, the subjects of noise, distortion and frequency planning are presented, with special attention paid to cascaded systems. In addition, a review of the current state of the art in CMOS receiver research establishes a context for the present work. In Chapter 3, the relevant technical details of the GPS system are presented along with a brief survey of common GPS receiver architectures. Then, applying the concepts developed in Chapter 1, we introduce a new architecture that takes advantage of details of the GPS signal spectrum to achieve a high level of integration.

Chapter 4 tackles the subject of CMOS low-noise amplifiers in great detail. This includes a survey of recent work and the development of a power-constrained noise figure optimization procedure for gaining the best performance for a stated power budget. Proceeding down the receiver chain, Chapter 5 discusses frequency mixers and focuses attention on the double-balanced CMOS voltage mixer that provides high linearity, low noise figure and extremely low power consumption. Chapter 6 follows with an investigation of active filters. Because the active filter is a dynamic range bottleneck in many receivers, this chapter focuses on how to design filter transconductor elements that maximize dynamic range with a given power consumption. In particular, we develop a figure of merit that permits a comparison of various transconductors, leading ultimately to a very power-efficient filter implementation.

To put these theoretical developments into practice, Chapter 7 presents the implementation of an experimental CMOS GPS receiver in a **0.5μm** process. The experimental results demonstrate a high level of performance and integration that is comparable to or better than existing implementations in more expensive technologies, thereby confirming the value of the techniques pre-

sented in earlier chapters. Finally, Chapter 8 concludes with a summary and some suggestions for future work.

For readers who survive the first eight chapters, several appendices present expanded treatment of certain subjects. Appendix A explores the topic of noise correlations in amplitude-limited gaussian noise channels. Appendix B presents a noise figure analysis of the MOSFET device using the classical technique. Appendix C presents some experimental results on two low-noise amplifiers: a single-ended amplifier and a differential amplifier. Finally, Appendix D describes the measurement techniques used to gather the experimental data reported in Chapter 7.