
**SILICON-ON-INSULATOR
TECHNOLOGY:
Materials To VLSI**

THE KLUWER INTERNATIONAL SERIES IN ENGINEERING AND COMPUTER SCIENCE

VLSI, COMPUTER ARCHITECTURE AND DIGITAL SIGNAL PROCESSING

Consulting Editor
Jonathan Allen

Latest Titles

- BiCMOS Technology and Applications*, A. R. Alvarez, Editor
ISBN: 0-7923-9033-4
- Analog VLSI Implementation of Neural Systems*, C. Mead, M. Ismail (Editors),
ISBN: 0-7923-9040-7
- The MIPS-X RISC Microprocessor*, P. Chow. ISBN: 0-7923-9045-8
- Nonlinear Digital Filters: Principles and Applications*, I. Pitas, A.N.
Venetsanopoulos, ISBN: 0-7923-9049-0
- Algorithmic and Register-Transfer Level Synthesis: The System Architect's
Workbench*, D.E. Thomas, E.D. Lagnese, R.A. Walker, J.A. Nestor, J.V. Ragan,
R.L. Blackburn, ISBN: 0-7923-9053-9
- VLSI Design for Manufacturing: Yield Enhancement*, S.W. Director, W. Maly,
A.J. Strojwas, ISBN: 0-7923-9053-7
- Testing and Reliable Design of CMOS Circuits*, N.K. Jha, S. Kundu,
ISBN: 0-7923-9056-3
- Hierarchical Modeling for VLSI Circuit Testing*, D. Bhattacharya, J.P.
Hayes, ISBN: 0-7923-9058-X
- Steady-State Methods for Simulating Analog and Microwave Circuits*,
K. Kundert, A. Sangiovanni-Vincentelli, J. White,
ISBN: 0-7923-9069-5
- Introduction to Analog VLSI Design Automation*, M. Ismail, J. Franca,
ISBN: 0-7923-9102-0
- Gallium Arsenide Digital Circuits*, O. Wing, ISBN: 0-7923-9081-4
- Principles of VLSI System Planning*, A.M. Dewey ISBN: 0-7923-9102
- Mixed-Mode Simulation*, R. Saleh, A.R. Newton, ISBN: 0-7923-9107-1
- Automatic Programming Applied to VLSI CAD Software: A Case Study*,
D. Setliff, R.A. Rutenbar, ISBN: 0-7923-9112-8
- Models for Large Integrated Circuits*, P. Dewilde, Z.Q. Ning
ISBN: 0-7923-9115-2
- Hardware Design and Simulation in VAL/VHDL*, L.M. Augustin, D.C. Luckham,
B.A. Gennart, Y. Huh, A.G. Stanculescu ISBN: 0-7923-9087-3
- Subband Image Coding*, J. Woods, editor, ISBN: 0-7923-9093-8
- Low-Noise Wide-Band Amplifiers in Bipolar and CMOS Technologies*, Z.Y. Chang,
W.M.C. Sansen, ISBN: 0-7923-9096-2
- Iterative Identification and Restoration Images*, R. L. Lagendijk, J. Biemond
ISBN: 0-7923-9097-0
- VLSI Design of Neural Networks*, U. Ramacher, U. Ruckert
ISBN: 0-7923-9127-6
- Synchronization Design for Digital Systems*, T. H. Meng ISBN: 0-7923-9128-4
- Hardware Annealing in Analog VLSI Neurocomputing*, B. W. Lee, B. J. Sheu
ISBN: 0-7923-9132-2
- Neural Networks and Speech Processing*, D. P. Morgan, C.L. Scofield
ISBN: 0-7923-9144-6

SILICON-ON-INSULATOR TECHNOLOGY: Materials To VLSI

by

Jean-Pierre Colinge
IMEC, Belgium



SPRINGER SCIENCE+BUSINESS MEDIA, LLC

Library of Congress Cataloging-in-Publication Data

Colinge, Jean-Pierre.

Silicon-on-insulator technology : materials to VLSI / by Jean
-Pierre Colinge.

p. cm. — (The Kluwer international series in engineering and
computer science ; SECS 132. VLSI, computer architecture, and
digital signal processing)

Includes bibliographical references and index.

ISBN 978-1-4757-2123-2

ISBN 978-1-4757-2121-8 (eBook)

DOI 10.1007/978-1-4757-2121-8

1. Semiconductors. 2. Silicon-on-insulator technology.
3. Integrated circuits—Very large scale integration—Materials.
I. Title. II. Series: Kluwer international series in engineering
and computer science ; SECS 132. III. Series: Kluwer international
series in engineering and computer science. VLSI, computer
architecture, and digital signal processing.

TK7871.85.C578 1991

621.381'52—dc20

90-29327

CIP

Copyright ©1991 by Springer Science+Business Media New York

Originally published by Kluwer Academic Publishers in 1991

Softcover reprint of the hardcover 1st edition 1991

All rights reserved. No part of this publication may be reproduced, stored in a retrieval system or transmitted in any form or by any means, mechanical, photo-copying, recording, or otherwise, without the prior written permission of the publisher, Springer Science+Business Media, LLC .

Printed on acid-free paper.

Contents

Preface	ix
Acknowledgements	xi
CHAPTER 1 - Introduction.....	1
CHAPTER 2 - SOI Materials.....	7
2.1. Heteroepitaxial techniques.....	7
2.1.1. Silicon-on-sapphire.....	8
2.1.2. Cubic zirconia.....	11
2.1.3. Silicon-on-spinel.....	11
2.1.4. Epitaxial calcium fluoride.....	11
2.1.5. Other heteroepitaxial SOI materials.....	12
2.1.6. Problems of heteroepitaxial SOI.....	12
2.2. Laser recrystallization.....	13
2.2.1. Types of lasers used	13
2.2.2. Seeding	14
2.2.3. Encapsulation.....	15
2.2.4. Beam shaping.....	16
2.2.5. Silicon film patterning	19
2.3. E-beam recrystallization.....	19
2.3.1. Scanning techniques	20
2.3.2. Seeding and wafer heating	21
2.4. Zone-melting recrystallization.....	21
2.4.1. Zone-melting recrystallization mechanisms.....	23
2.4.1.1. Melting front.....	23
2.4.1.2. Solidification front.....	25
2.4.2. Role of the encapsulation.....	28
2.4.3. Mass transport.....	29
2.4.4. Impurities in the ZMR film	30
2.5. Homoepitaxial techniques.....	32
2.5.1. Epitaxial lateral overgrowth.....	32
2.5.2. Lateral solid-phase epitaxy.....	34
2.6. FIPOS.....	34
2.7. SIMOX	38
2.7.1. A brief history of SIMOX.....	39
2.7.2. Oxygen implantation.....	40
2.7.2.1. Oxygen dose.....	40
2.7.2.2. Implant temperature.....	42
2.7.3. Annealing parameters.....	43
2.7.4. Multiple implants.....	46
2.7.5. Low-energy implantation.....	46
2.7.6. Material quality.....	47

2.8. SIMNI and SIMON	4 8
2.8.1. SIMNI.....	4 8
2.8.2. SIMON	4 9
2.9. Wafer bonding and etch-back.....	4 9
2.9.1. Mechanisms of bonding.....	5 0
2.9.2. Etch-back techniques	5 2
2.10. What material for what application?.....	5 3
CHAPTER 3 - SOI Materials Characterization.....	5 5
3.1. Film thickness measurement.....	5 6
3.1.1. Spectroscopic reflectometry.....	5 6
3.1.2. Spectroscopic ellipsometry.....	6 2
3.1.3. Electrical thickness measurement.....	6 5
3.2. Crystal quality.....	6 6
3.2.1. Crystal orientation.....	6 6
3.2.2. Degree of crystallinity.....	6 8
3.2.3. Crystal defects.....	7 1
3.2.3.1. (Sub)grain boundaries.....	7 3
3.2.3.2. Dislocations.....	7 4
3.3. Silicon film contamination	7 4
3.3.1. Carbon contamination	7 5
3.3.2. Oxygen contamination.....	7 5
3.4. Carrier lifetime and surface recombination.....	7 6
3.4.1. Surface photovoltage.....	7 6
3.4.2. Lifetime measurement in devices.....	7 8
3.4.2.1. Generation lifetime & surface generation....	7 8
3.4.2.2. Recombination lifetime.....	8 4
3.5. Silicon-oxide interfaces.....	8 5
3.5.1. Capacitance measurements.....	8 5
3.5.2. Charge pumping.....	8 7
CHAPTER 4 - SOI CMOS Technology.....	9 1
4.1. Comparison between bulk and SOI processing.....	9 1
4.2. Isolation techniques.....	9 4
4.3. Doping profiles.....	9 8
4.4. Source and drain silicidation	10 1
4.5. SOI MOSFET design.....	10 2
4.6. SOI-bulk CMOS design comparison.....	10 4

CHAPTER 5 - The SOI MOSFET	107
5.1. Introduction.....	107
5.2. Distinction between thick- and thin-film devices.....	109
5.3. I-V Characteristics.....	112
5.3.1. Threshold voltage.....	112
5.3.2. Body effect.....	118
5.3.3. Short-channel effects.....	120
5.3.4. Output characteristics.....	124
5.4. Transconductance and mobility.....	129
5.4.1 Transconductance.....	129
5.4.2. Mobility.....	130
5.5. Subthreshold slope.....	132
5.6. Impact ionization and high-field effects.....	139
5.6.1. Kink effect.....	139
5.6.2. Hot-electron degradation.....	143
5.7. Parasitic bipolar effects.....	145
5.7.1. Anomalous subthreshold slope.....	145
5.7.2. Reduced drain breakdown voltage.....	147
5.8. Accumulation-mode p-channel MOSFET.....	149
CHAPTER 6 - Other SOI Devices.....	159
6.1. Non-conventional devices adapted from bulk.....	159
6.1.1. COMFET.....	160
6.1.2. High-voltage lateral MOSFET.....	161
6.1.3. PIN photodiode.....	162
6.1.4. JFET.....	163
6.2. Novel SOI devices.....	164
6.2.1. Lubistor.....	164
6.2.2. Bipolar-MOS device.....	166
6.2.3. Double-gate MOSFET.....	169
6.2.4. Bipolar transistors.....	172
6.2.5. Optical modulator.....	174
CHAPTER 7 - The SOI MOSFET Operating in a Harsh Environment.....	177
7.1. Radiation environment.....	177
7.1.1. SEU.....	178
7.1.2. Total dose.....	180
7.1.3. Dose-rate.....	184
7.2. High-temperature operation.....	185
7.2.1. Leakage currents.....	185
7.2.2. Threshold voltage.....	186
7.3. Low-temperature operation.....	189
7.3.1. Threshold voltage.....	189
7.3.2. Kink effect.....	189
7.3.3. Subthreshold slope.....	190
7.3.4. Mobility.....	190

CHAPTER 8 - SOI Circuits	191
8.1. Rad-hard and high-temperature circuits.....	191
8.2. VLSI and high-speed CMOS circuits.....	193
8.3. Three-dimensional integrated circuits.....	197
BIBLIOGRAPHY	203
INDEX.....	225

Preface

Silicon-on-Insulator (SOI) technology has been around for over a decade, and yet, there is no book describing its multiple facets and possibilities. In ten years of extensive research efforts, SOI technology has made dramatic progress from the first laser recrystallization experiments to CMOS circuits operating at multi-gigahertz frequencies, withstanding high temperatures or surviving several hundred megarads of radiation. At first SOI technology was only considered as a possible replacement for SOS in some niche applications. It has, however, been discovered since then that thin-film SOI MOSFETs have excellent scaling properties which make them extremely attractive for deep-submicron ULSI applications. The commercial availability of SOI substrates, the good fabrication yield obtained in SIMOX 64k SRAMs, and the demonstration of functional three-dimensional integrated circuits are all indicators of a level of maturity reached by Silicon-on-Insulator technology which cannot be questioned any longer. In this Book, we will try to bridge the gap which exists between the specialized SOI literature and the classical textbooks describing bulk device physics, processing and applications.

The SOI community has been extremely productive in the recent years, and a large amount of papers have been published over SOI materials, devices and circuits. It is, unfortunately, not practical to take all these contributions into account, and a selection had to be made in order to present the most significant results of this research effort in a clear and concise manner. Time is, of course, another limitation. Communications published after the summer of 1990 are, therefore, not included in this Book, with a few exceptions.

The material covered by this bulk is divided in eight Chapters, which are summarized below:

CHAPTER 1: INTRODUCTION briefly describes some obvious advantages of SOI technology, such as the absence of latchup in CMOS structures and the reduction of parasitic source and drain capacitances.

CHAPTER 2: SOI MATERIALS lists the different approaches for producing SOI materials. The basic mechanisms behind the fabrication of thin silicon films on an insulating substrate using epitaxy, melting and recrystallization, implantation or bonding are described. This Chapter also addresses the issues of material quality. The application fields for the different materials are described.

CHAPTER 3: SOI MATERIALS CHARACTERIZATION describes different techniques which have been developed to characterize the physical and electrical properties of Silicon-on-Insulator materials. Indeed, while some "universal" characterization techniques such as SIMS and TEM can, of course, be used to assess the quality SOI materials, some techniques have been developed especially to assess the SOI crystal quality and its interface properties, and to measure the film thickness and the lifetime in Silicon-on-Insulator materials.

CHAPTER 4: SOI CMOS TECHNOLOGY deals with the basics of SOI CMOS processing. Thin-film and thicker-film SOI CMOS processes are compared with bulk CMOS processing. Some process steps which are particular to SOI as well as different MOSFET structures are described.

CHAPTER 5: THE SOI MOSFET deals with the physics of the SOI MOSFET. The electrical characteristics (threshold voltage, body effect and output characteristics) of thick- and thin-film MOSFETs are derived and compared to those of bulk devices. The subthreshold slope and the transconductance of SOI transistors are analyzed in detail. The effects caused by the parasitical bipolar transistor are reviewed.

CHAPTER 6: OTHER SOI DEVICES describes other types of SOI devices (double-gate transistors, bipolar transistors, high-voltage devices, JFETs, optical modulators, ...)

CHAPTER 7: THE SOI MOSFET OPERATING IN A HARSH ENVIRONMENT describes the performances of SOI devices operating in a harsh environment (high temperature, radiations, ...)

And, finally, **CHAPTER 8: SOI CIRCUITS** reviews the performances of modern SOI circuits, such as high-speed CMOS, VLSI, rad-hard and three-dimensional integrated circuits.

Acknowledgements

I would like to express my appreciation to many colleagues who have supported my SOI activity over the years, especially when SOI was considered by most people as nothing but an exotic research topic: Drs. M. Lobet, P. Verlinden and F. Van de Wiele from the Université Catholique de Louvain (UCL), Drs. D. Bensahel, G. Bomchil, E. Demoulin, M. Haond and D.P. Vu from the Centre National d'Etude des Télécommunications (CNET), Drs. S.Y. Chiang, C. Drowley, T. Kamins and J. Moll from Hewlett-Packard, and Drs. C. Claeys, G. Declerck, M. Ghannam, R. De Keersmaecker, H. Maes, R. Mertens and R. Van Overstraeten from the Interuniversitair Micro-Elektronica Centrum (IMEC).

I would like to thank the individuals who helped me collecting information, even unpublished, about SOI technology, and/or who reviewed parts of the manuscript: Drs. A.J. Auberton-Hervé, G. Celler, S. Cristoloveanu, A. De Veirman, E. Dupont-Nivet, J.G. Fossum, M. Haond, P.L.F. Hemment, J.L. Leray, J. Margail, P. Mertens, J.C. Sturm, P. Swart, J. Vanhellemont, D.P. Vu, G. Willems and D. Wouters.

Finally, I would especially like to thank Drs. J.C. Alderman and G.E. Davis for proofreading the whole manuscript and making useful suggestions to improve the content of this Book.

*Ce livre est dédié
à mon épouse Carine,
à nos parents,
et à notre fils Colin-Pierre*